

# The ALICE low-mass silicon tracker



**ALICE**

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On behalf of the ALICE ITS

- ▶ Introduction
- ▶ ITS pointing resolution performance
- ▶ Focus on the SPD components and material budget
- ▶ Towards the ITS upgrade

# The ALICE experiment



## Dedicated heavy ion experiment at LHC

- ▶ Study of the behavior of strongly interacting matter under extreme conditions of high energy density and temperature

## Proton-Proton collisions

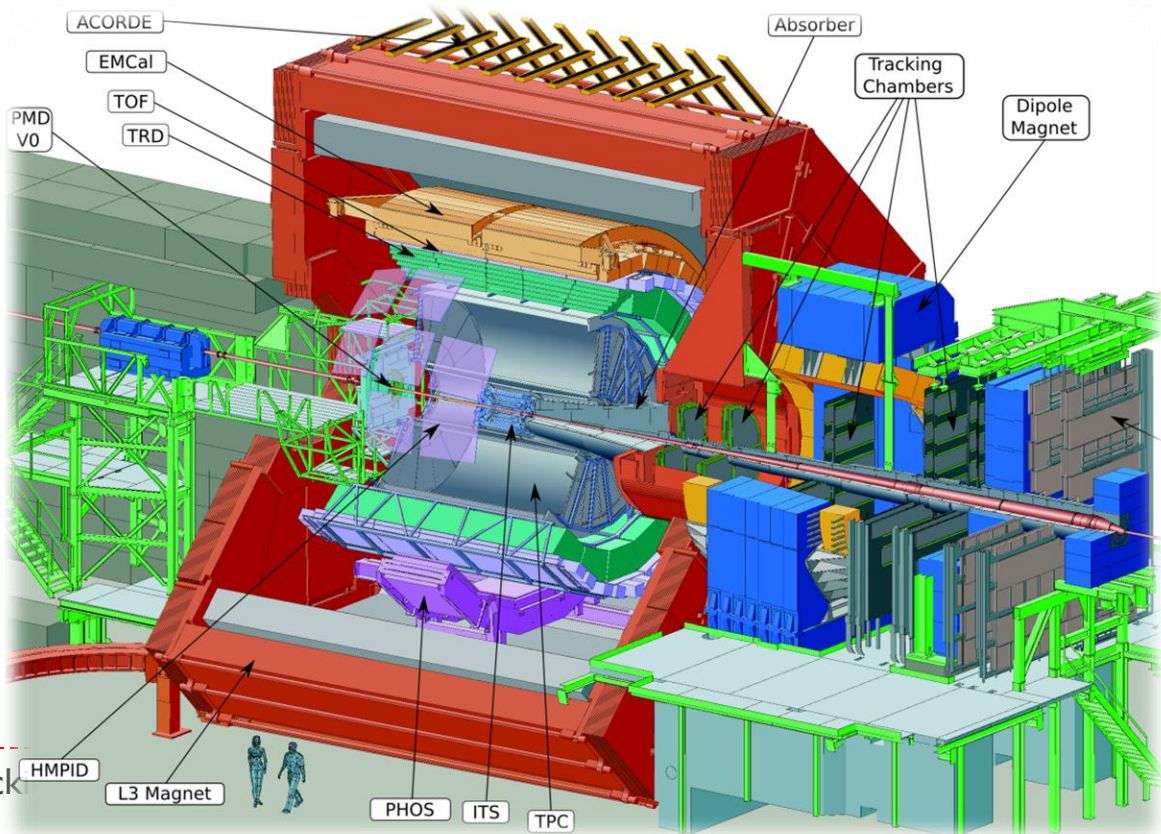
- ▶ Reference data for heavy-ion program
- ▶ Genuine physics (momentum cutoff  $< 100 \text{ MeV}/c$ , excellent PID, efficient minimum bias trigger)

## Barrel Tracking requirements ( $|\eta| < 0.9$ )

- ▶ Robust tracking for heavy ion environment
  - ▶ Mainly 3D hits and up to 150 points along the tracks
- ▶ Wide transverse momentum range (100 MeV/c – 100 GeV/c)
  - ▶ Low material budget (13% X0 up to the end of TPC)
  - ▶ Large lever arm to guarantee good tracking resolution at high pt

## PID requirements over the large momentum range

- ▶ Combined PID based on several techniques:  $dE/dx$ , TOF, transition and Cherenkov radiation



# The ALICE Inner Tracking System



## The ITS role in ALICE

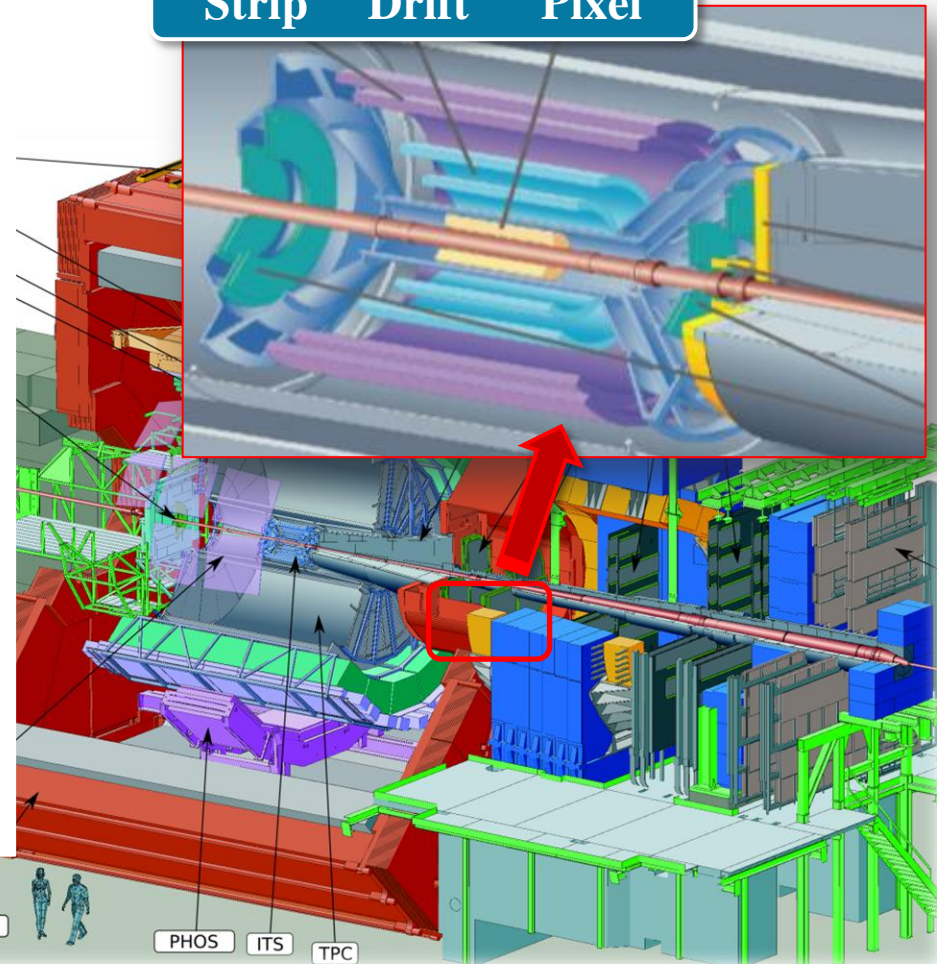
- ▶ Secondary vertex reconstruction (c, b decays)
  - ▶ Good track impact parameter resolution ( $< 60 \mu\text{m}$  ( $r\phi$ ) for  $p_t > 1 \text{ GeV}/c$  in Pb-Pb)
- ▶ Improve primary vertex reconstruction and momentum resolution
- ▶ Tracking and PID of low  $p_t$  particles
- ▶ Prompt L0 trigger capability ( $< 800 \text{ ns}$ )
- ▶ Measurements of charged particle pseudorapidity distribution
  - ▶ First Physics measurement both in p-p and Pb-Pb

## Detector requirements

- ▶ Two dimension detectors to handle high particle density
- ▶ Good spatial precision
- ▶ High efficiency
- ▶ High granularity ( $\approx$  few % occupancy)
- ▶ Minimize distance of innermost layer from beam axis (mean radius  $\approx 3.9 \text{ cm}$ )
- ▶ Limited material budget
- ▶ Analogue information in 4 layers (Drift and Strip) for particle identification in  $1/\beta^2$  region via  $dE/dx$

**ITS: 3 different silicon detector technologies**

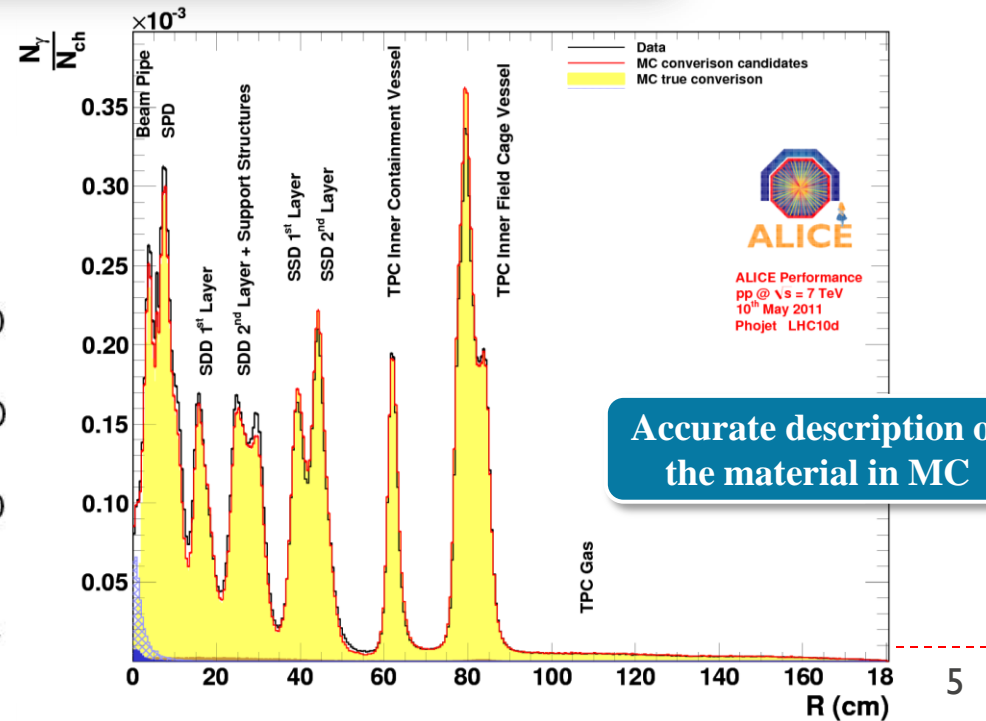
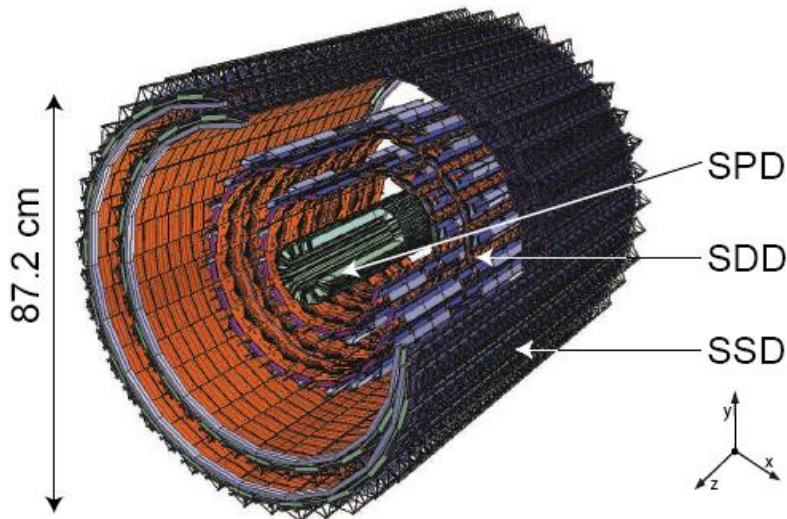
**Strip Drift Pixel**





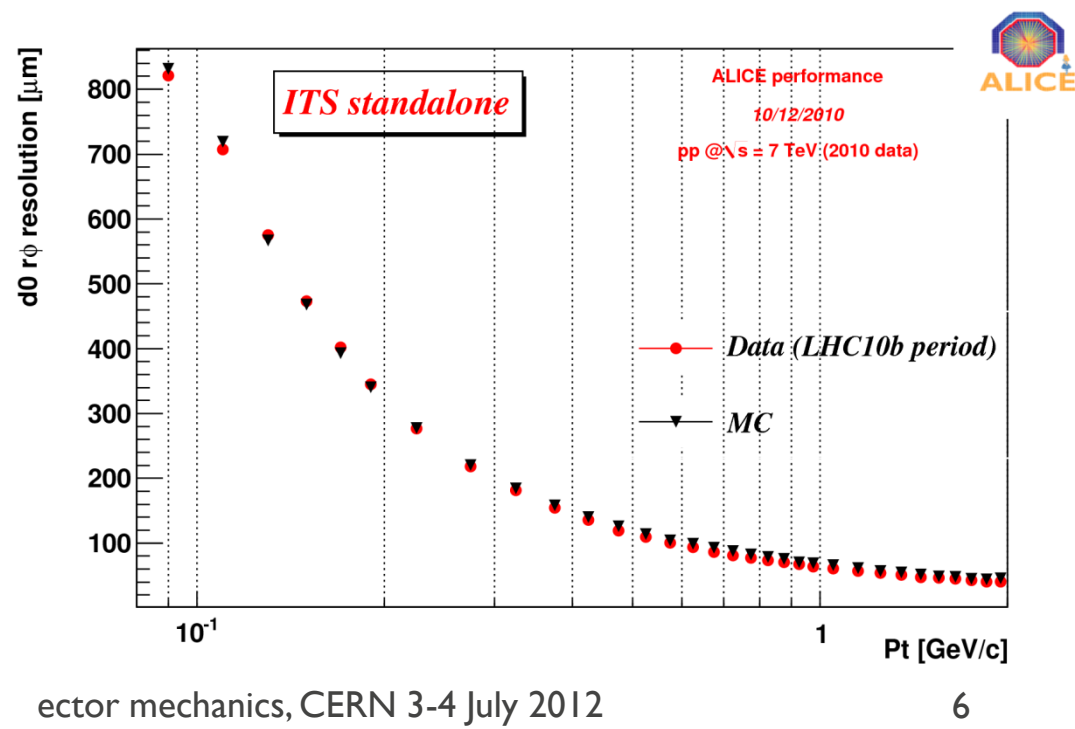
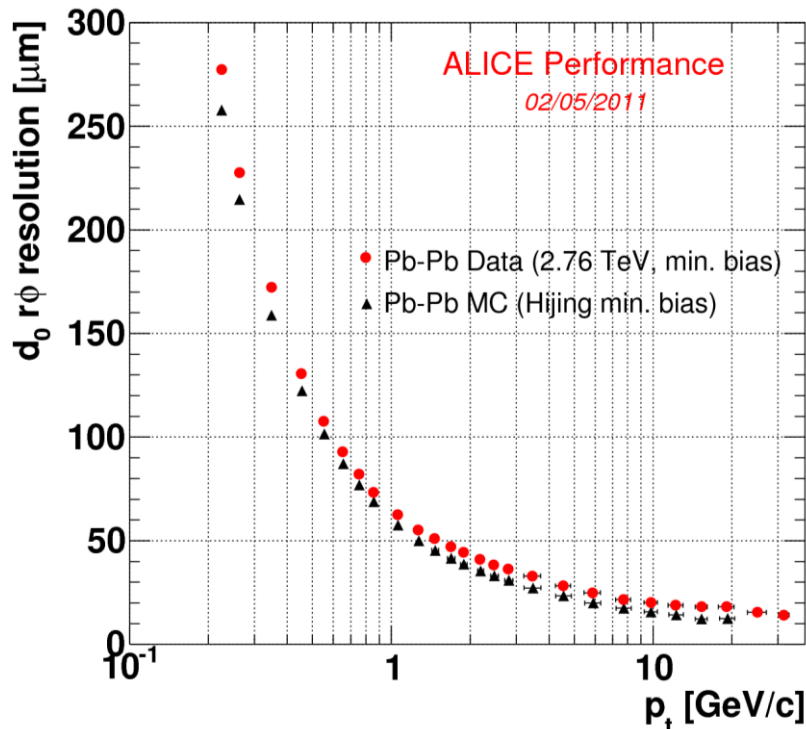
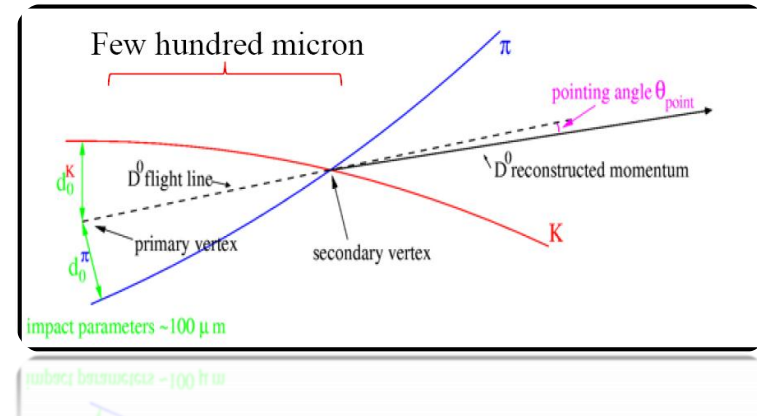
# ITS parameters

| Layer | Det. | Radius (cm) | Length (cm) | Surface (m <sup>2</sup> ) | Chan. | Spatial precision (mm) |     | Cell (μm <sup>2</sup> ) | Max occupancy central PbPb (%) | Material Budget (% X <sub>0</sub> ) | Power dissipation (W) |         |
|-------|------|-------------|-------------|---------------------------|-------|------------------------|-----|-------------------------|--------------------------------|-------------------------------------|-----------------------|---------|
|       |      |             |             |                           |       | rφ                     | z   |                         |                                |                                     | barrel                | end-cap |
| 1     | SPD  | 3.9         | 28.2        | 0.21                      | 9.8M  | 12                     | 100 | 50x425                  | 2.1                            | 1.14                                | 1.35k                 | 30      |
| 2     |      | 7.6         | 28.2        |                           |       |                        |     |                         |                                |                                     |                       |         |
| 3     | SDD  | 15.0        | 44.4        | 1.31                      | 133 K | 35                     | 25  | 202x294                 | 2.5                            | 1.13                                | 1.06k                 | 1.75k   |
| 4     |      | 23.9        | 59.4        |                           |       |                        |     |                         |                                |                                     |                       |         |
| 5     | SSD  | 38.0        | 86.2        | 5.0                       | 2.6M  | 20                     | 830 | 95x40000                | 4.0                            | 0.83                                | 850                   | 1.15k   |
| 6     |      | 43.0        | 97.8        |                           |       |                        |     |                         |                                |                                     |                       |         |



# Transverse impact parameter

- ▶ A key plot to quote the tracker performance in terms of track and vertex reconstruction is the transverse impact parameter in the bending plane:  $d_0(r\phi)$ 
  - ▶ Distance between the track projection and the vertex position reconstruction in the bending plane
- ▶ The material budget mainly affect the performance at low  $p_t$  (multiple scattering)
- ▶ The point resolution of each layers drives the asymptotic performance



# Some considerations

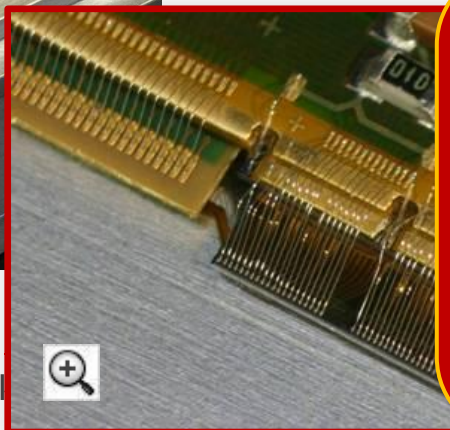
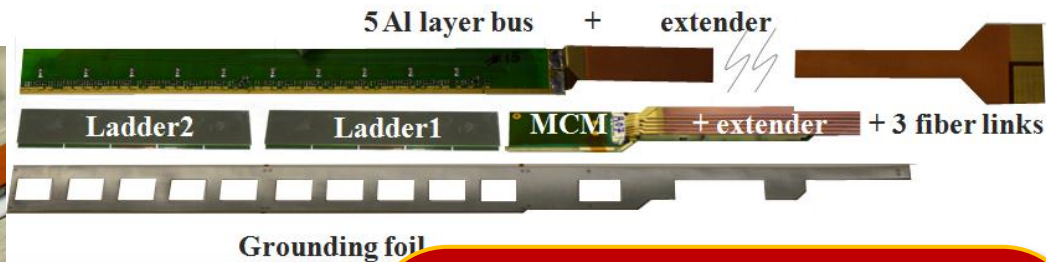
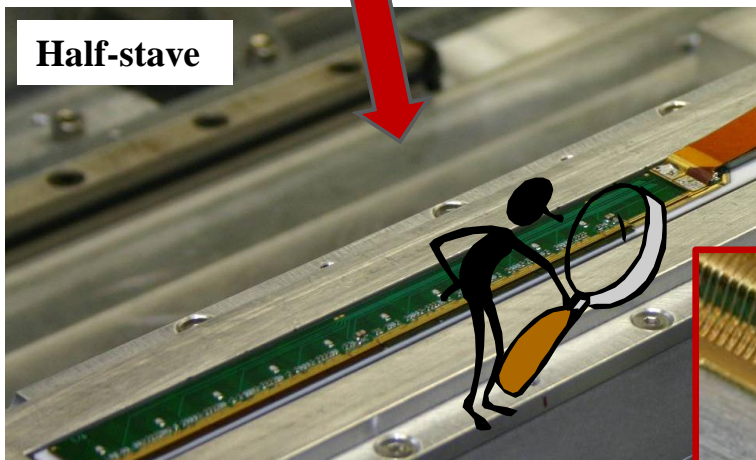
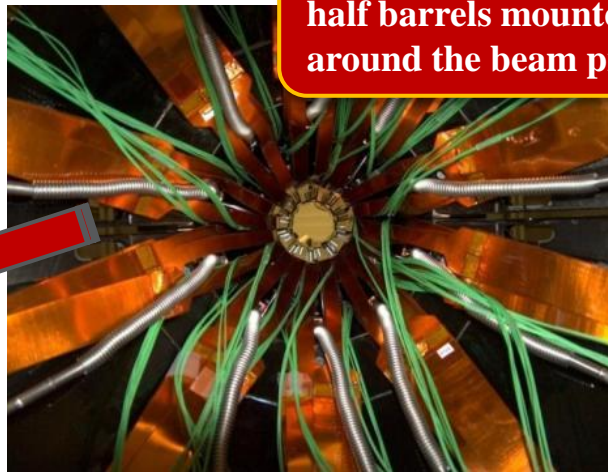
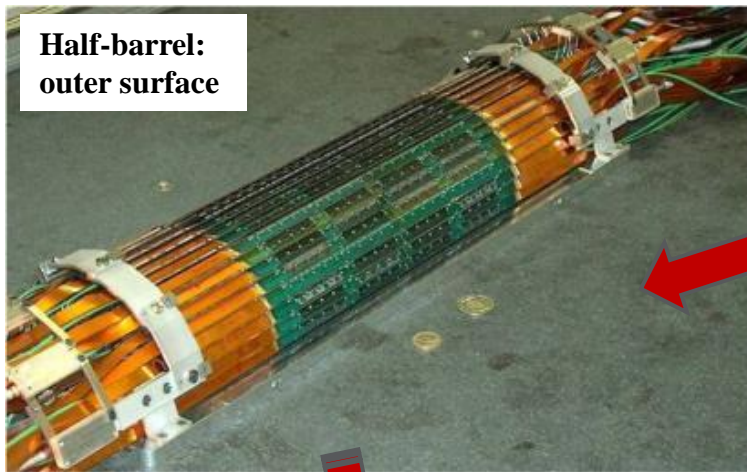


- ▶ The key requirements to obtain good tracking performance are:
  - ▶ Small channel dimension
  - ▶ Low material budget
  - ▶ First layer as close as possible to the interaction point
  
- ▶ From now on I will show how these requirements have driven the design of the silicon pixel detector in ALICE
  - ▶ Channel dimension:  $50 \mu\text{m}$  ( $r\phi$ ) x  $425 \mu\text{m}$  ( $z$ )
  - ▶ Material budget: 1.14 % of  $X_0$
  - ▶ Mean sensor radial position of the first layer = 39 mm
    - ▶ Beam pipe outer radius = 29.8 mm



# Silicon Pixel Detector (SPD)

2 layers of pixels grouped in 2 half barrels mounted face to face around the beam pipe

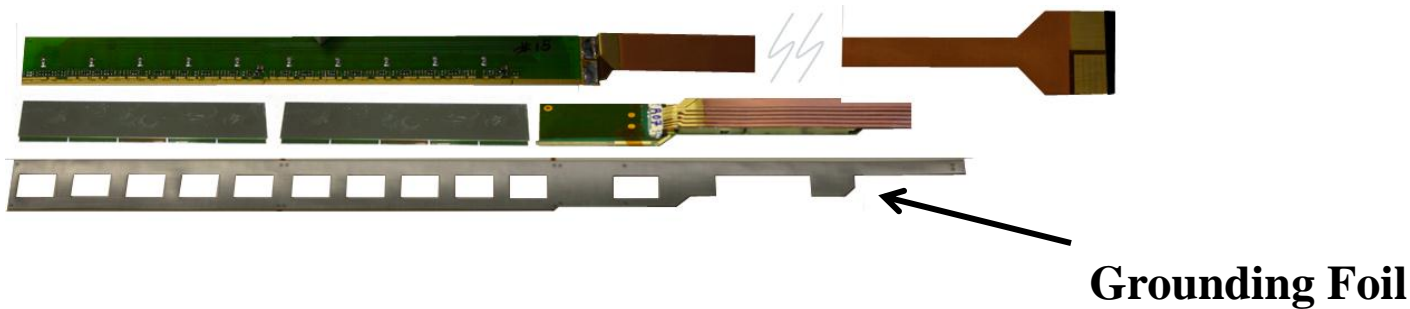


- ✓ Total surface:  $\sim 0.24\text{m}^2$
- ✓ Power consumption  $\sim 1.4\text{kW}$
- ✓ Evaporative cooling  $\text{C}_4\text{F}_{10}$
- ✓ Operating at room temperature
- ✓ Fast two-dimensional readout ( $256\mu\text{s}$ )
- ✓ High efficiency ( $> 99\%$ )
- ✓ L0 trigger capability
- ✓ Material budget per layer =  $1.14\% X_0$

| Layer | Radius (cm) | # half-staves | Ladders/half-stave | # ladders |
|-------|-------------|---------------|--------------------|-----------|
| 1     | 3.9         | 40            | 2                  | 80        |
| 2     | 7.6         | 80            | 2                  | 160       |

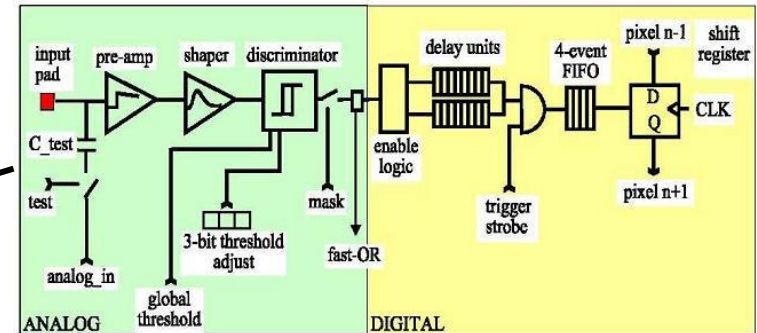
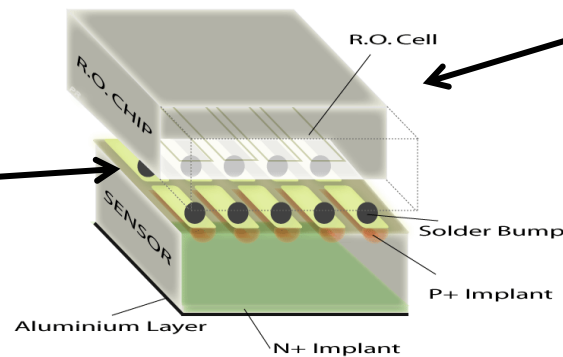
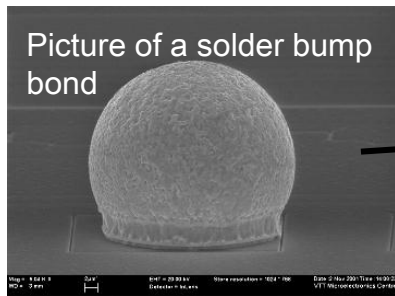
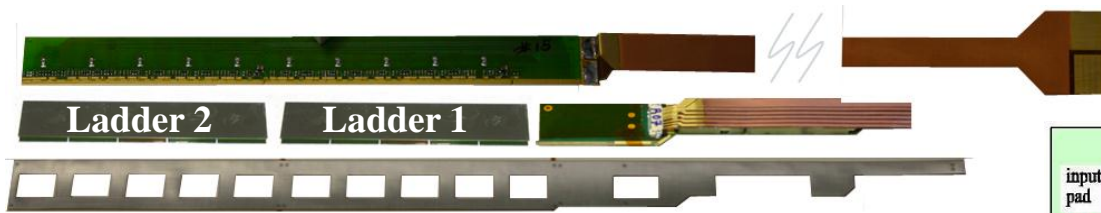


# Half – stave components



- ▶ Grounding foil: Aluminum-polyimide foil (25 + 50  $\mu\text{m}$  thick)
  - ▶ Reference ground for the half-stave
  - ▶ The 11 openings are needed to improve the thermal coupling between the electronics and cooling duct via thermal grease
- ▶  $X/X_0 = 0.03 \%$

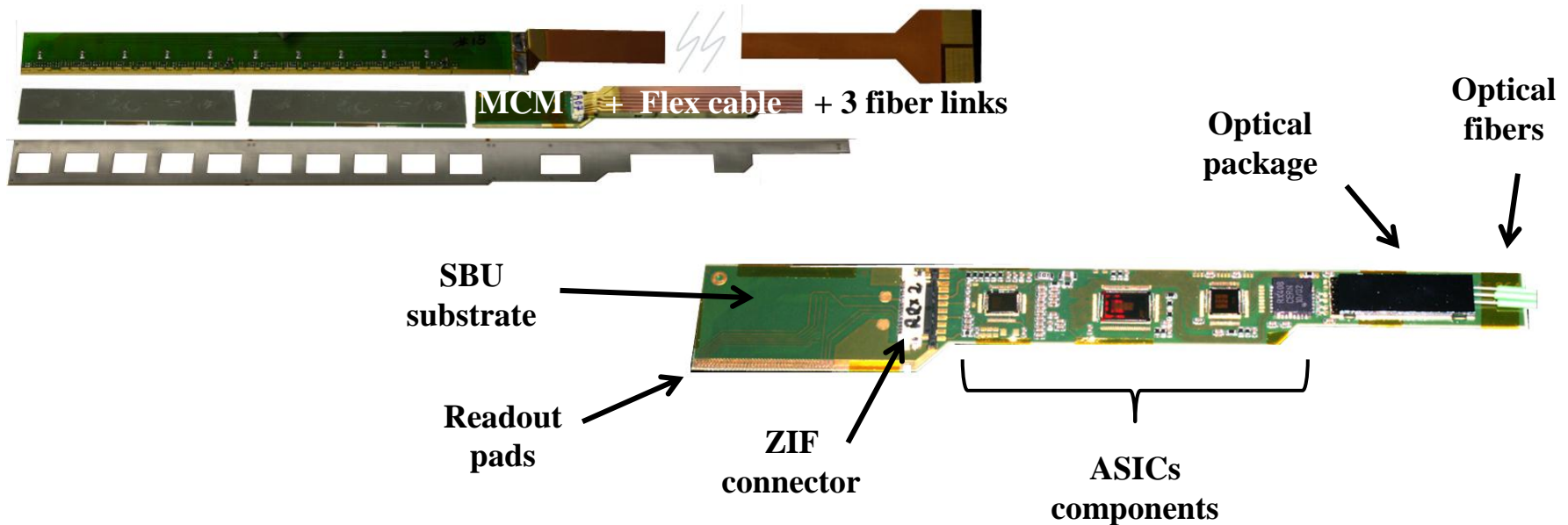
# Half – stave components



## FEE chip

- ▶ Ladder: Sensor + FEE chip (200 + 150  $\mu\text{m}$  thick)
  - ▶ A p+n silicon sensor matrix with 40960 pixels arranged in 256 rows and 160 columns
  - ▶ Pixel cell: 50  $\mu\text{m}$  (r $\phi$ ) x 425  $\mu\text{m}$  (z)
  - ▶ 5 FEE chips Flip-chip bonded to the sensor through Sn-Pb bumps
- ▶  $X/X_0 = 0.38 \%$

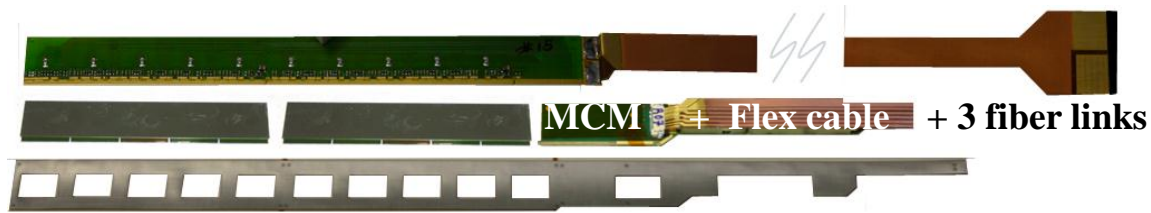
# Half – stave components



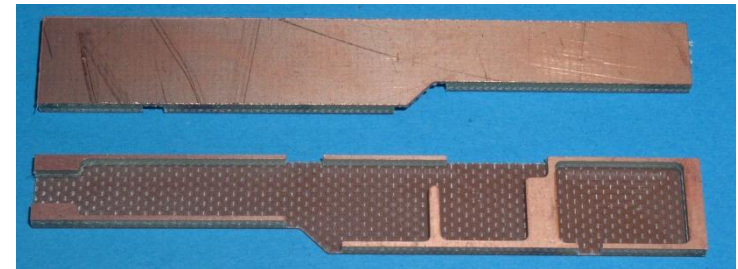
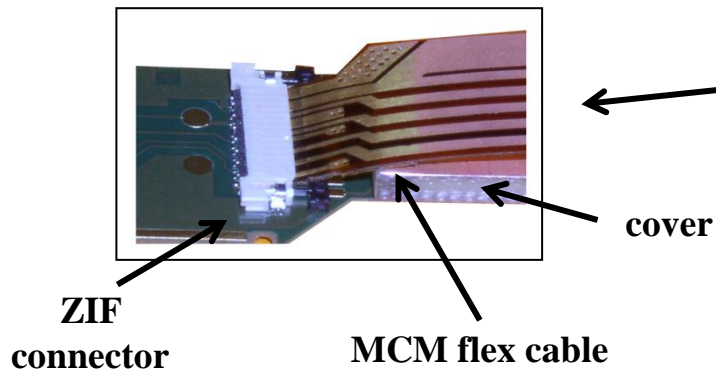
## ▶ Multi Chip Module (MCM)

- ▶ 5-metal-layer SBU substrate (Polyimide – copper)  $\approx 350 \mu\text{m}$  thick
- ▶ Four ASICs produced in standard  $0.25 \mu\text{m}$  CMOS technology with radiation hardness layout techniques
  - ▶ Analog Pilot, Digital Pilot, Giga-bit optical link (GOL) and RX40 to convert the optical link into electrical signals
- ▶ A custom developed optical package 1.2 mm thick (STMicroelectronics) with three single-mode 1310nm optical fibers to communicate with the counting room

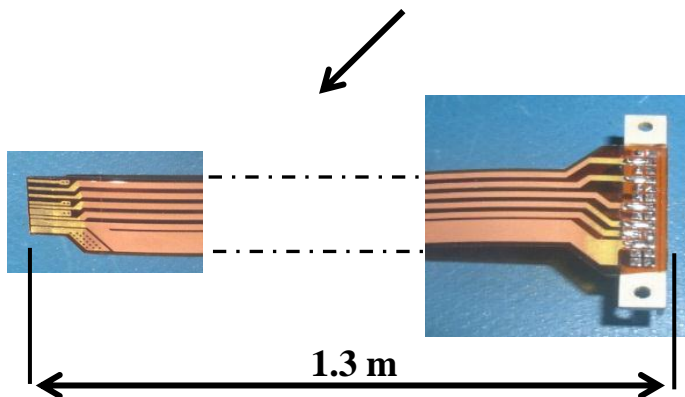
# Half – stave components



- ❑ These components are outside the barrel acceptance
- ❑ They were optimized anyway to reduce disturbance at high rapidity and to allow the detector integration



Cover to protect the electrical components (FR4, 300µm thick) glued after the qualification test

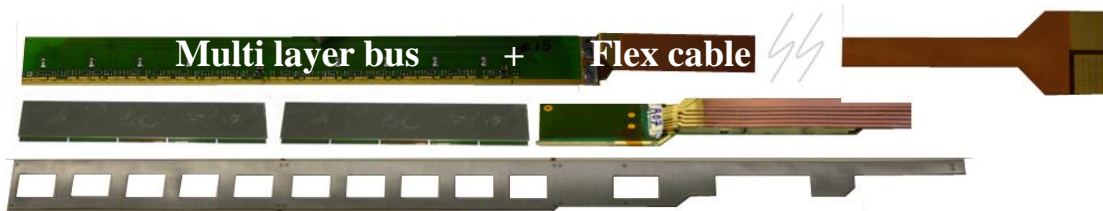


## MCM flex cable

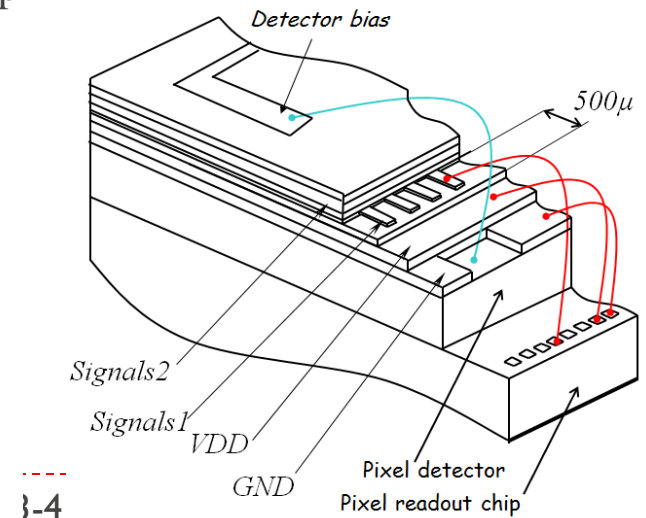
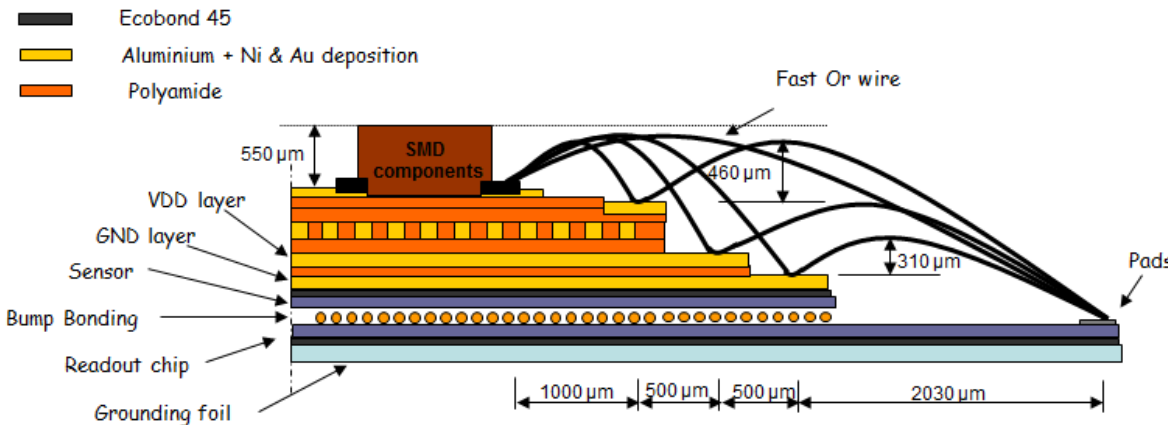
- ▶ Single layer polyimide/copper flex cable (200 µm thick)
- ▶ It provides power (2.5V / 0.5A), sense, bias and the detector temperature (used in the interlock)
- ▶ 1.3 m long to reach the first patch panel



# Half – stave components

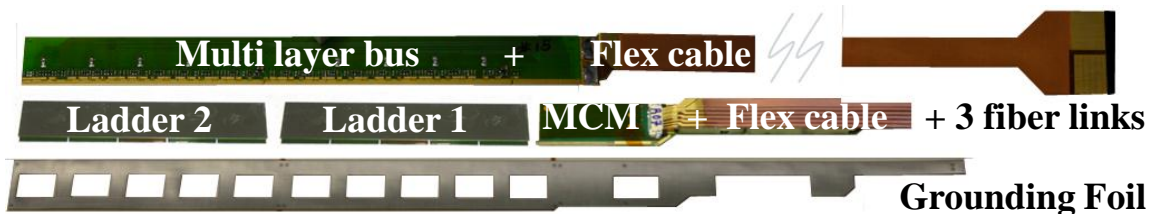


- ▶ 5-layer polyimide/aluminum (280  $\mu\text{m}$  thick) bus to connect front-end chips and MCM
  - ▶ The aluminum was used to reduce the impact on the material budget
    - ▶ Almost 30% of reduction replacing Cu with Al
  - ▶ The bus distributes power/ground to the FEE chips (two 50  $\mu\text{m}$  thick Al-layers)
  - ▶ The other three layers are used to carry data/control lines
  - ▶ The step side is needed to allow access to the different planes for the interconnection bonds
  - ▶ Decoupling capacitors and PT1000 are integrated on the top
- ▶ Overall X/X0 = 0.48 %



}-4

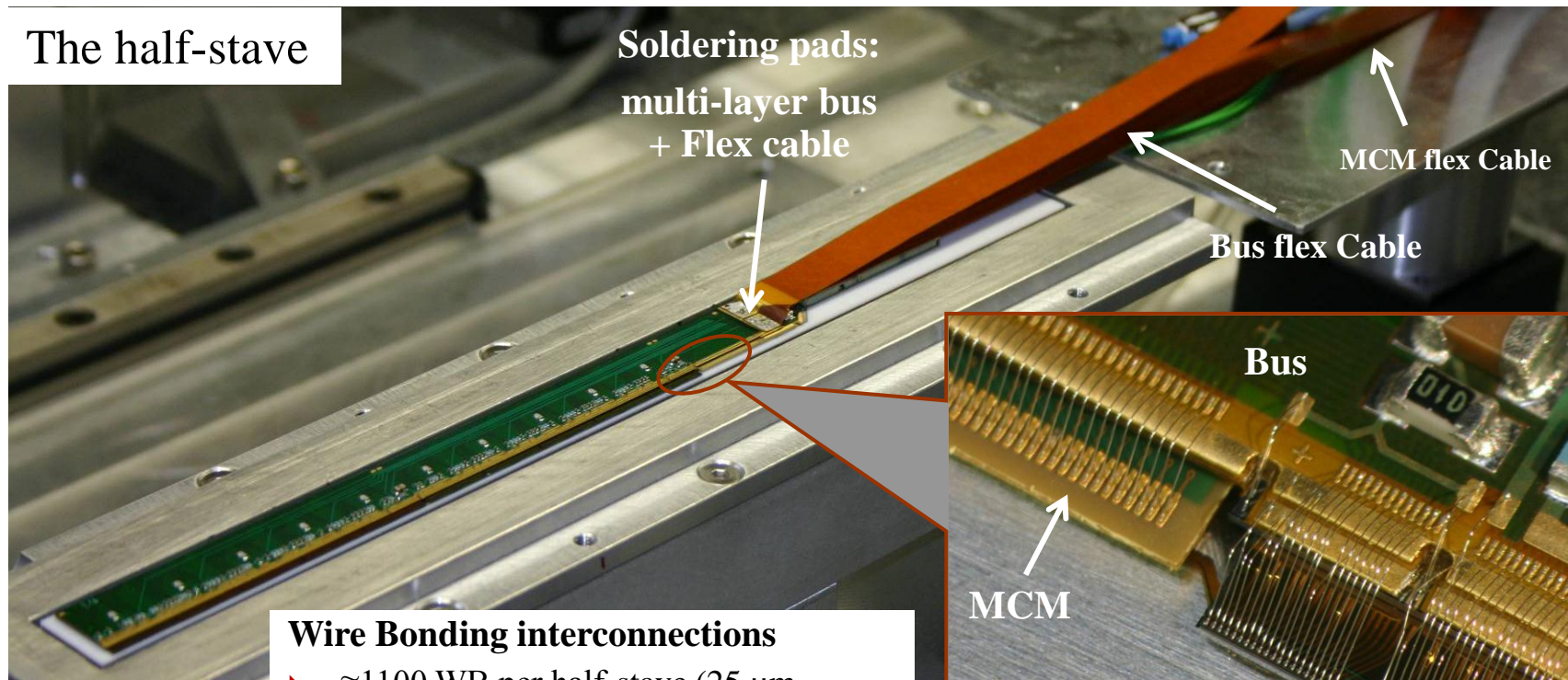
# Half – stave components



## Bus flex cable

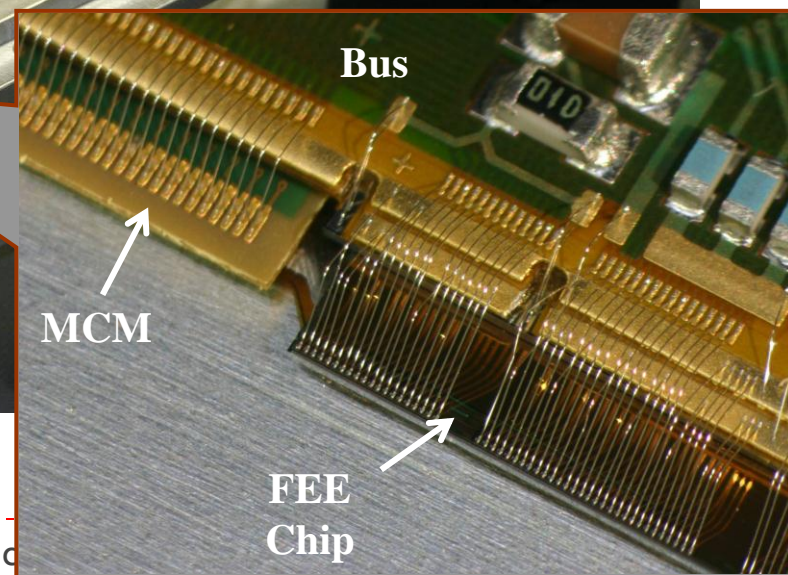
- ▶ Double layer polyimide/copper flex cable (250  $\mu\text{m}$  thick)
- ▶ It provides the power to the FEE chips (1.85V / 5A)

## The half-stave



## Wire Bonding interconnections

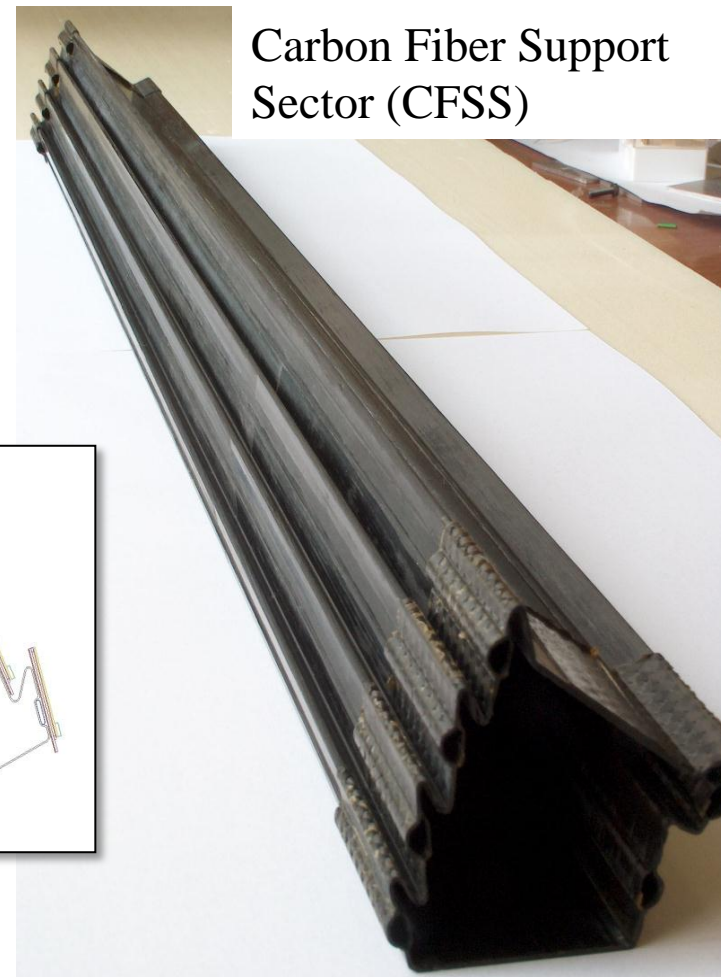
- ▶  $\approx 1100$  WB per half-stave (25  $\mu\text{m}$  diameter)
- ▶ 32 data lines and 71 lines for control, test and power in each chip



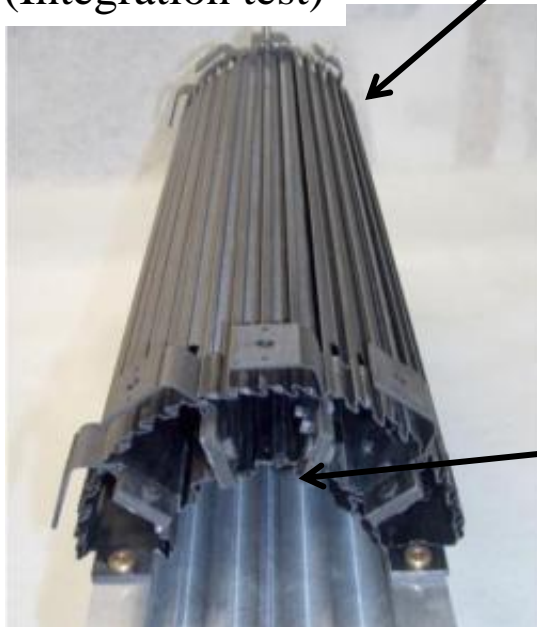
# Sector components

## ▶ Carbon fiber support structure

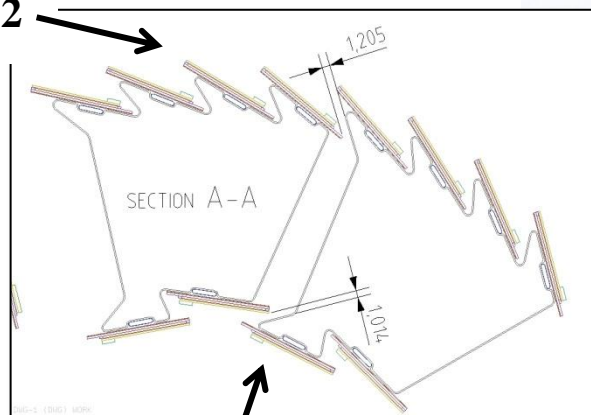
- ▶ 1/10 of the 2-layer barrel structure
- ▶ Two layers of unidirectional high-modulus carbon fiber tapes 100 $\mu$ m thick
- ▶ The central part is 200 $\mu$ m thick while ends are thicker (600 $\mu$ m) to allow the precise positioning and fixing
- ▶ The special design allows to accommodate the cooling pipes and to overlap the half-staves in  $r\phi$ .
- ▶ The global and local deformations of the CFSS are of the order of 1  $\mu$ m



Bare half-barrel  
(Integration test)



Layer 2



Layer 1

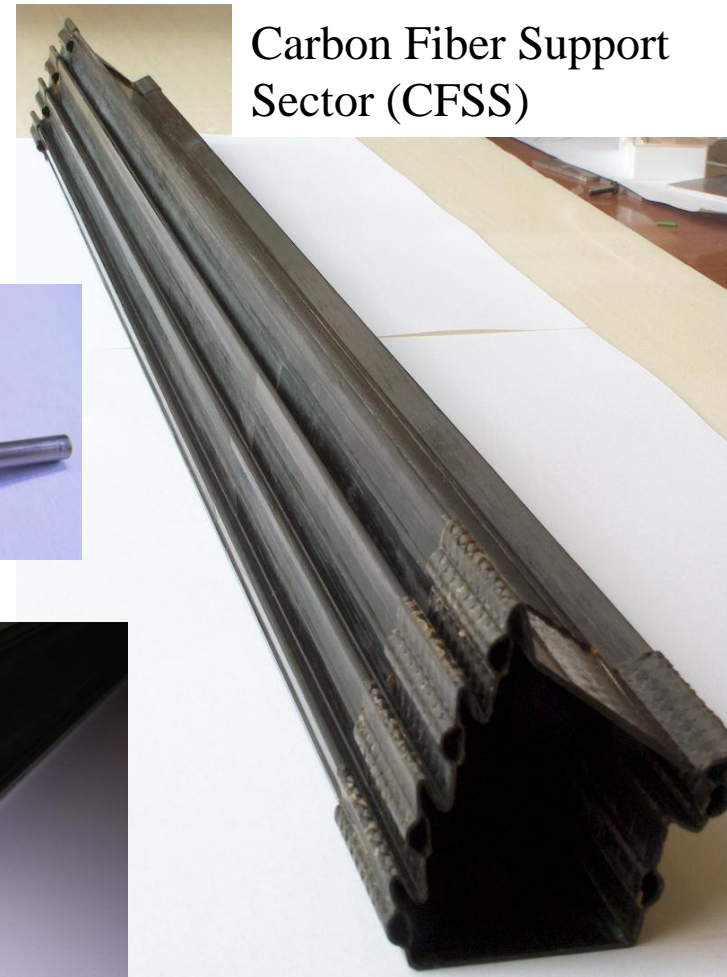
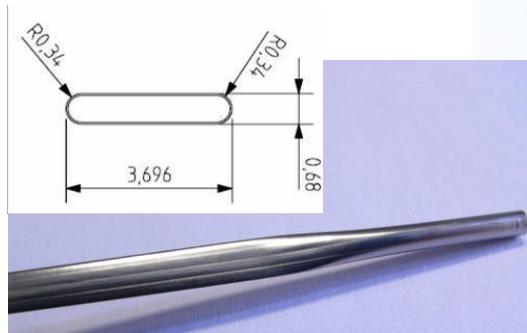
(close to the beam pipe)



# Sector components

## 6 Cooling pipes / sector (2 for layer 1 and 4 for layer 2)

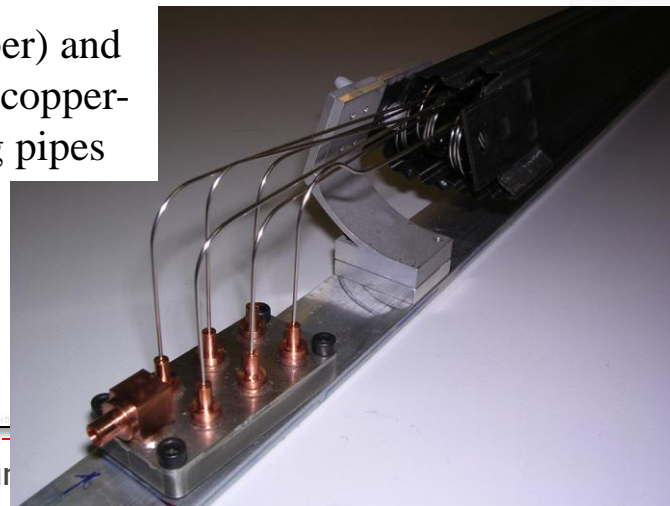
- ▶ Phynox pipes with 3mm diameter and 40 $\mu$ m wall
- ▶ Squeezed to 0.6 mm (inner size) to enlarge the thermal coupling surface
- ▶ Embedded to the CFSS



Carbon Fiber Support Sector (CFSS)

Manifold (steel), fittings (copper) and 6 capillaries (0.85 mm OD) in copper-nickel alloy to feed the cooling pipes

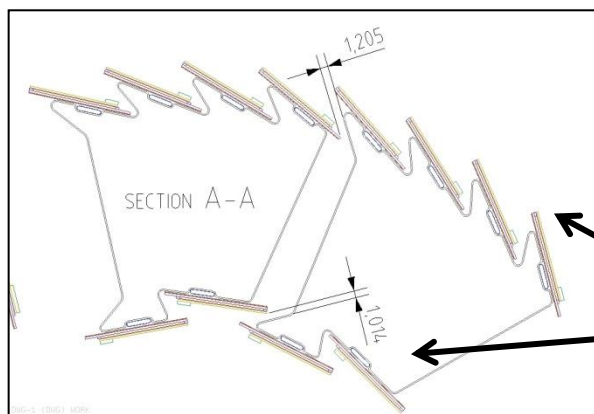
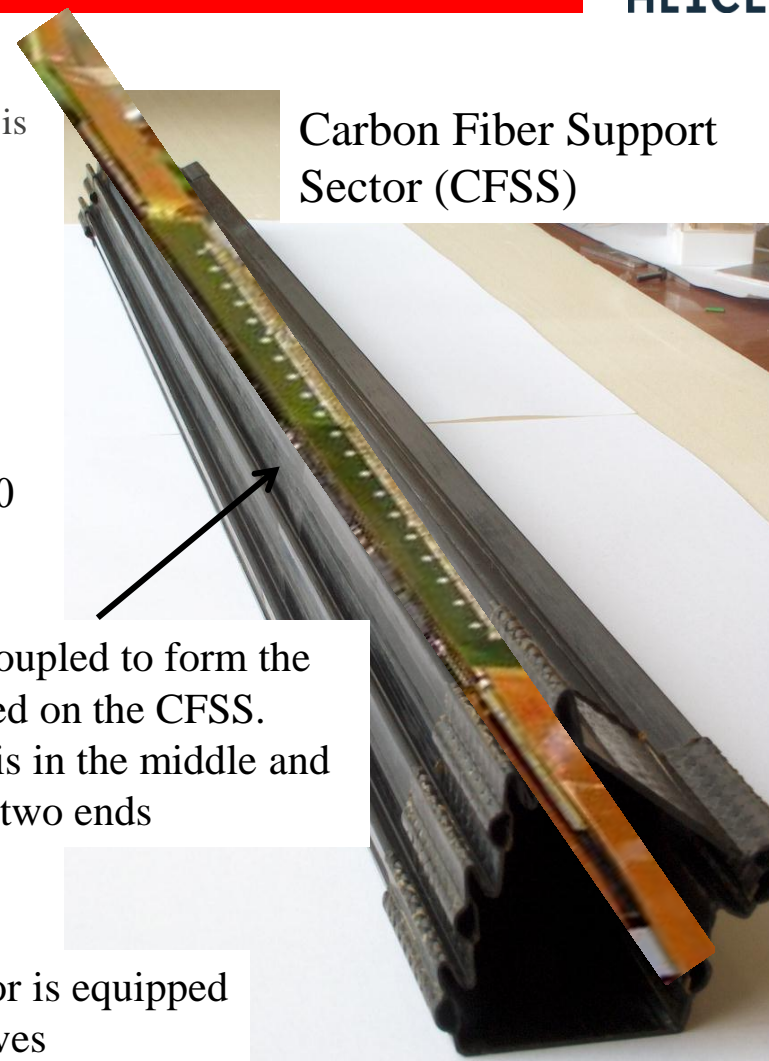
**outside the barrel acceptance**





# Sector components

- ▶ The Cooling is based on evaporative system with C4F10
  - ▶ Thermal contact between the cooling pipe and the FEE chips is performed with thermal grease (AOS 52029)
  - ▶ HS mechanical fixing to the CFSS with UV glue (NEA 123)
- ▶ Sector power dissipation  $\approx 135$  W
  - ▶ Working temperature  $\approx 30^\circ\text{C}$
  - ▶ Due to the low mass of the SPD a cooling failure causes a temperature rise of  $\approx 1^\circ\text{C/s}$
- ▶ Material budget contribution due to the mechanical support and piping in the central region is  $\approx 0.19\%$  of X0



2 half-staves are coupled to form the stave and are placed on the CFSS. The active region is in the middle and the services at the two ends

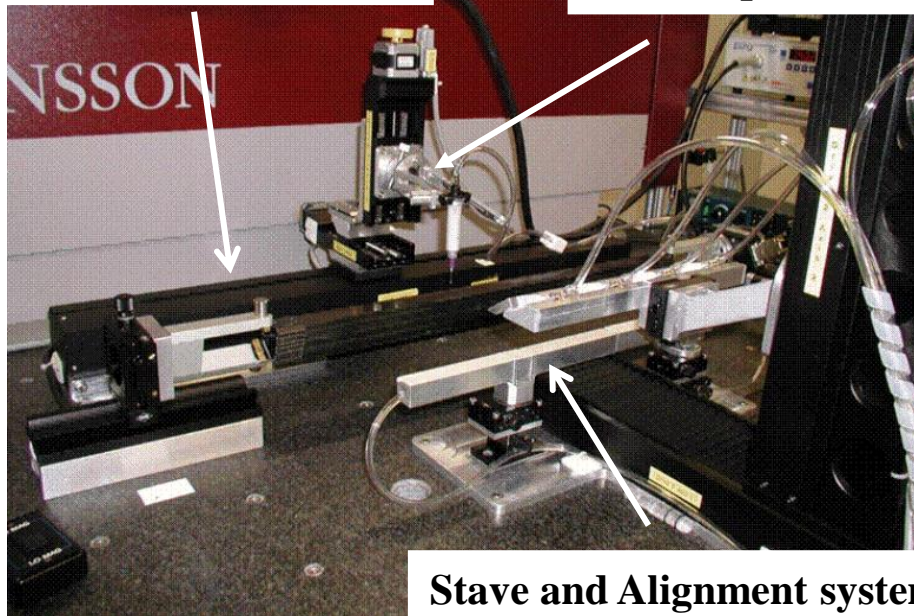
Each sector is equipped with 6 staves

# Sector set up



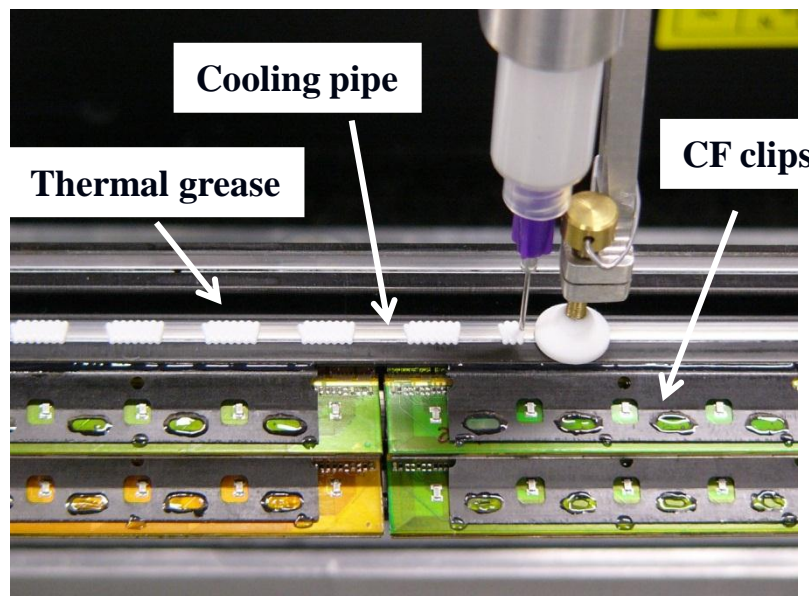
ALICE

Rotating sector support



Glue dispenser tower

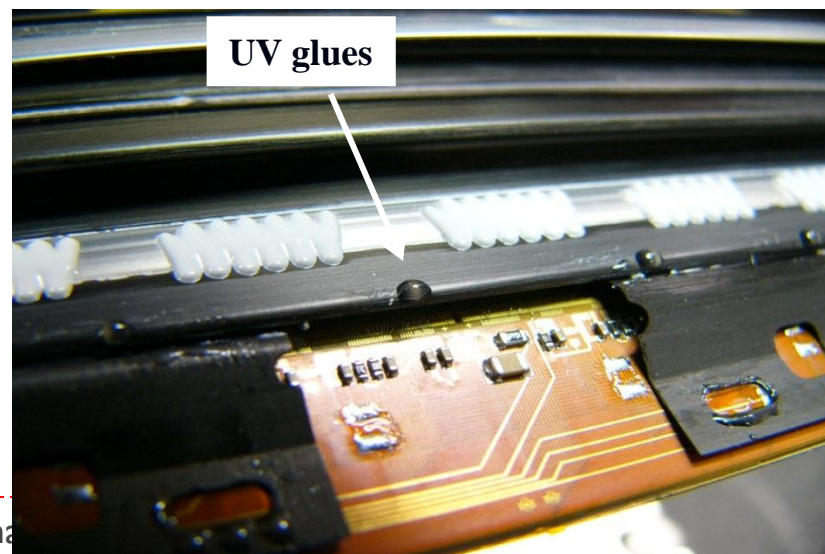
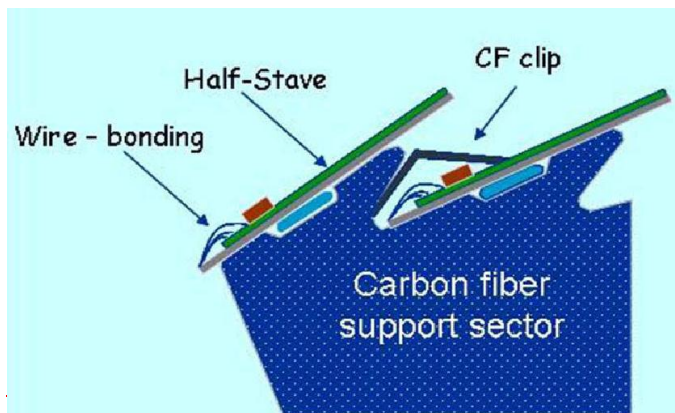
Stave and Alignment system



Cooling pipe

Thermal grease

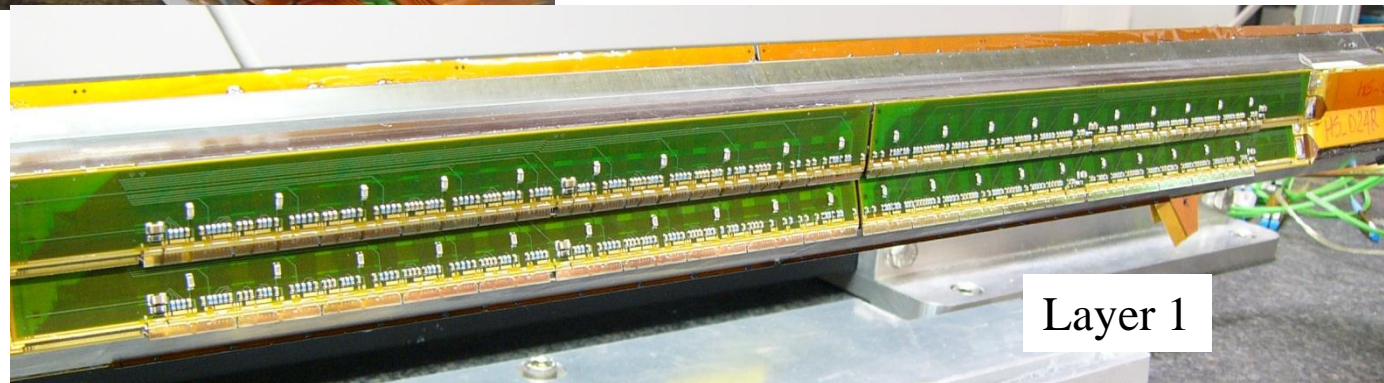
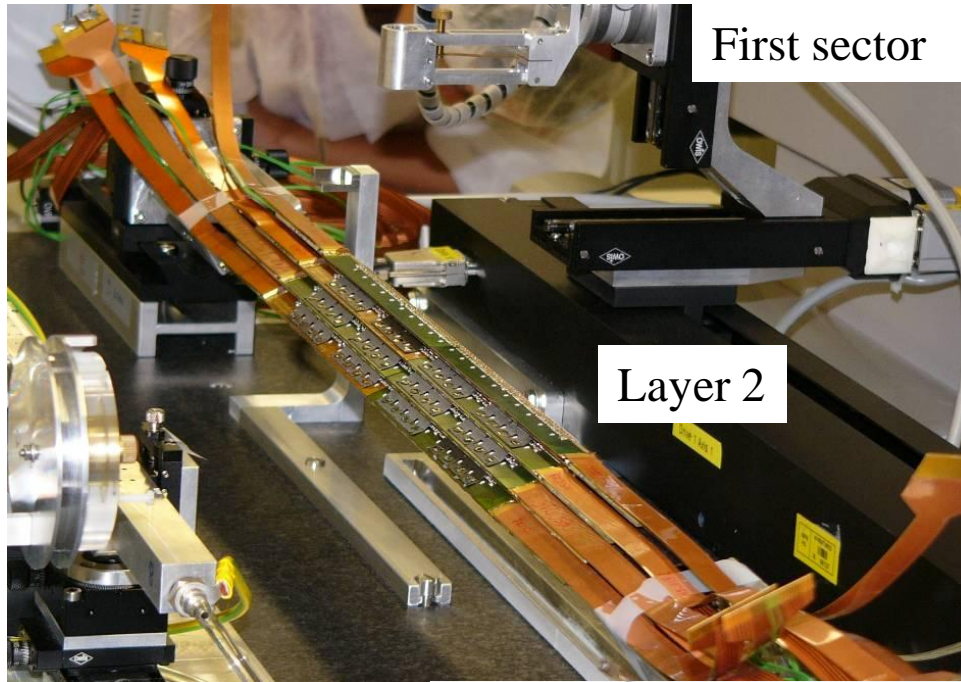
CF clips



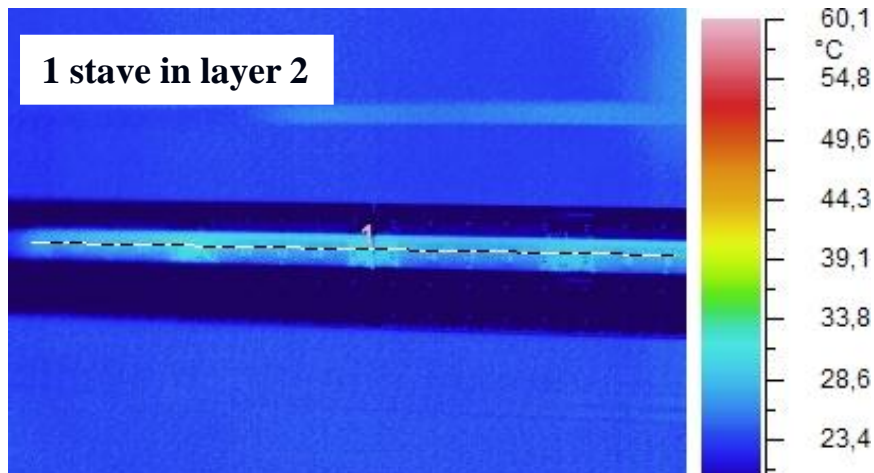
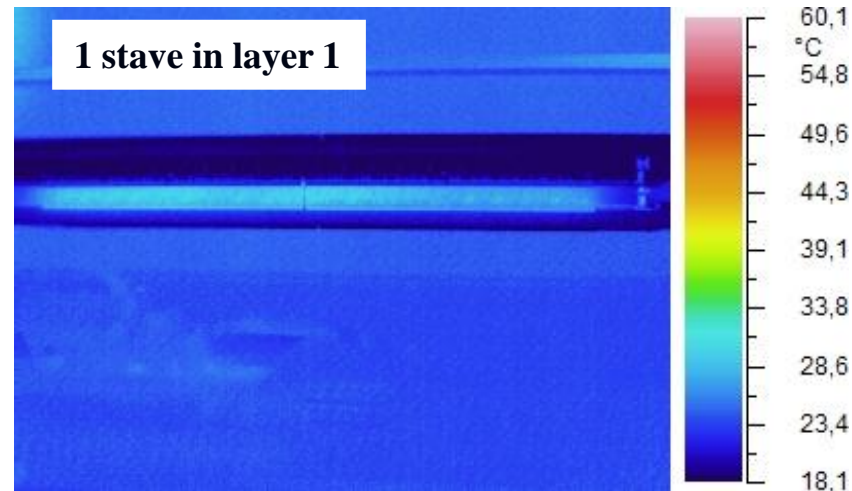
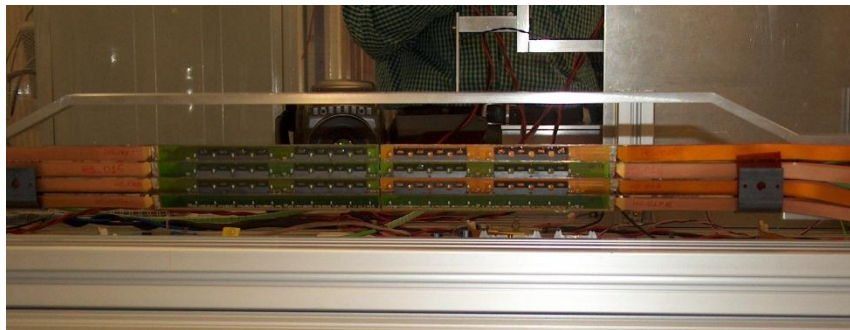
UV glues



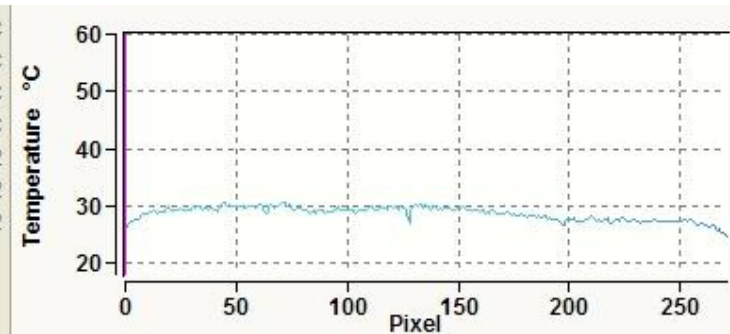
# The first sector fully equipped



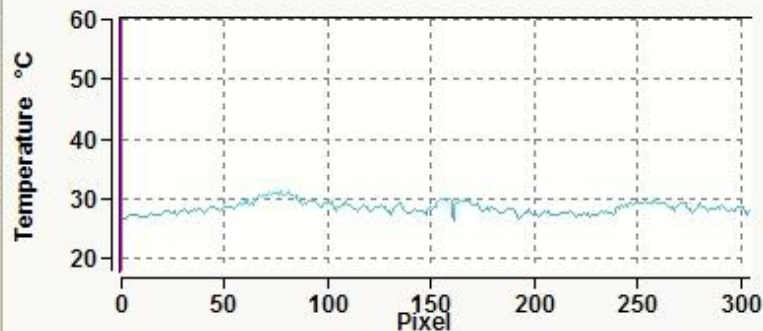
# Cooling thermal qualification



Max : 30,69 °C  
 Avr : 28,60 °C  
 Min : 24,18 °C  
 Temp: 25,95 °C  
 FstP(x/y): 13/92  
 LstP(x/y): 284/92  
 Points : 272



Max : 31,07 °C  
 Avr : 28,45 °C  
 Min : 25,95 °C  
 Temp: 25,95 °C  
 FstP(x/y): 11/110  
 LstP(x/y): 315/116  
 Points : 305

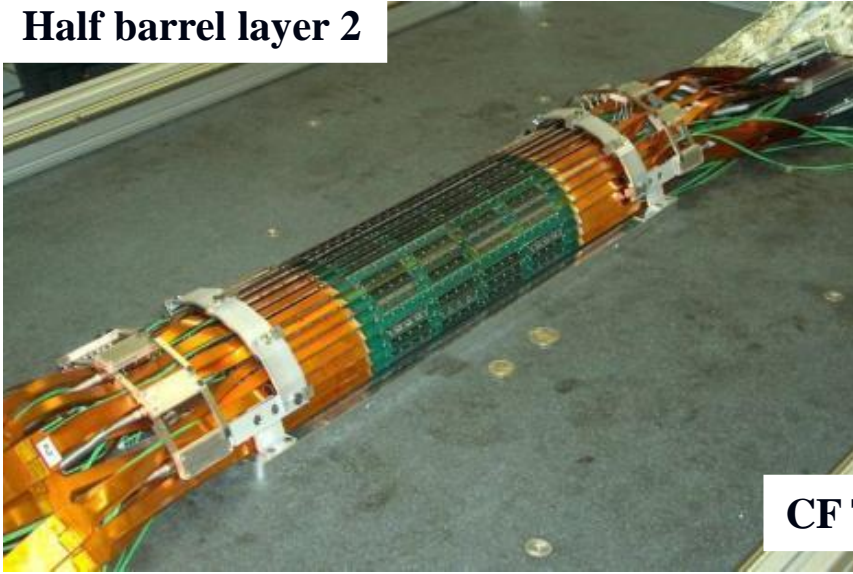


← Stave temperature profile



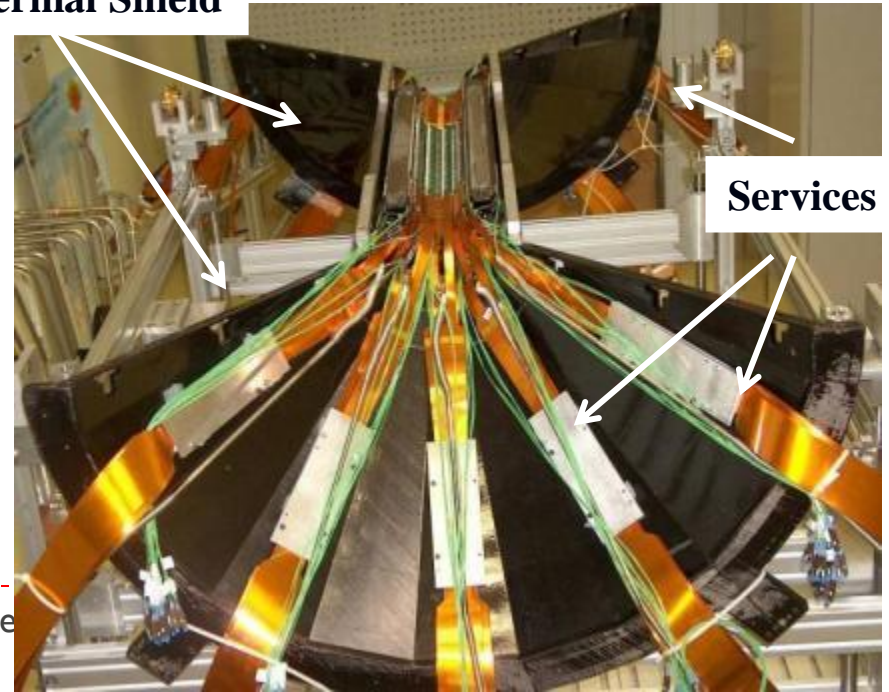
# Half-barrel integration

Half barrel layer 2



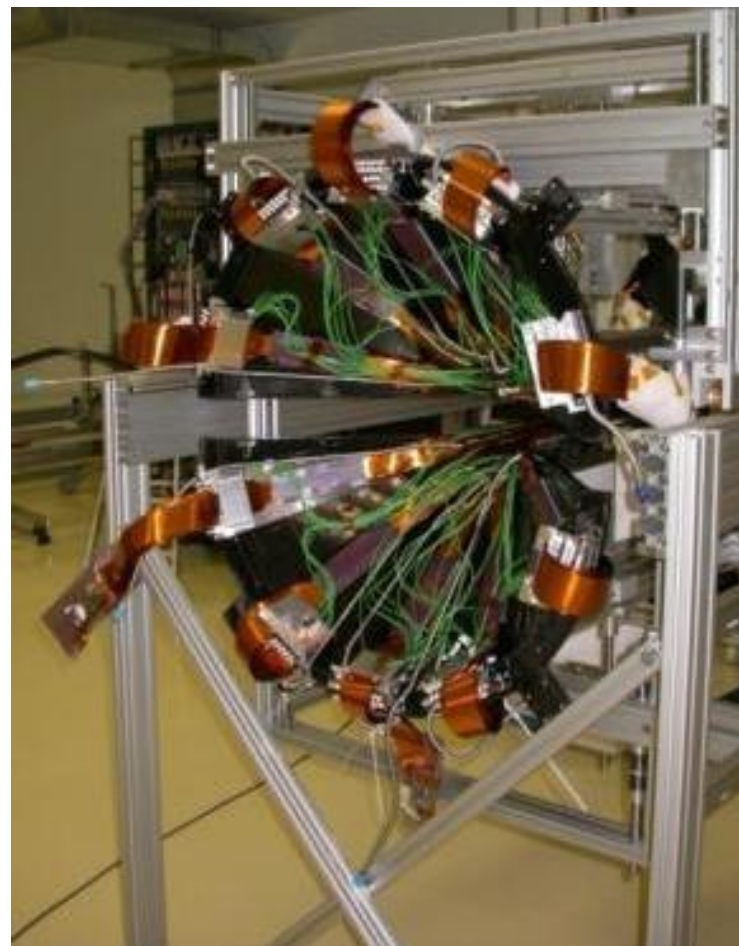
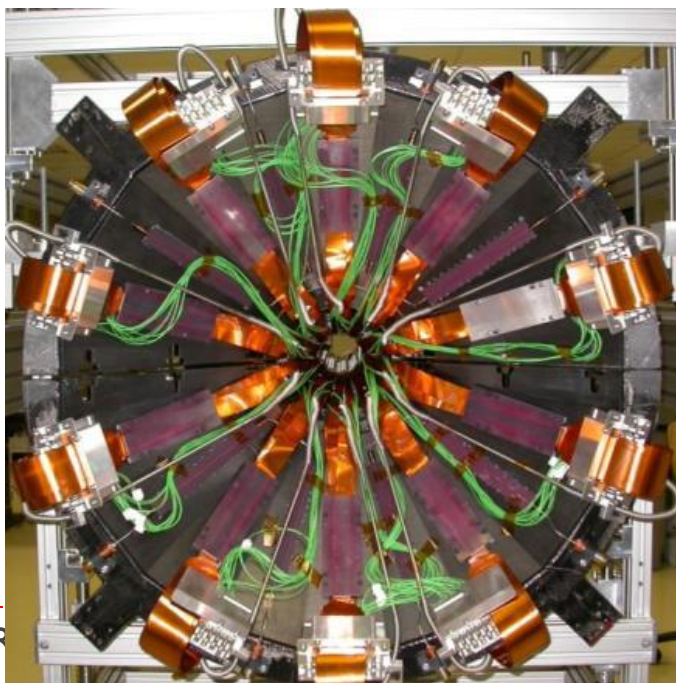
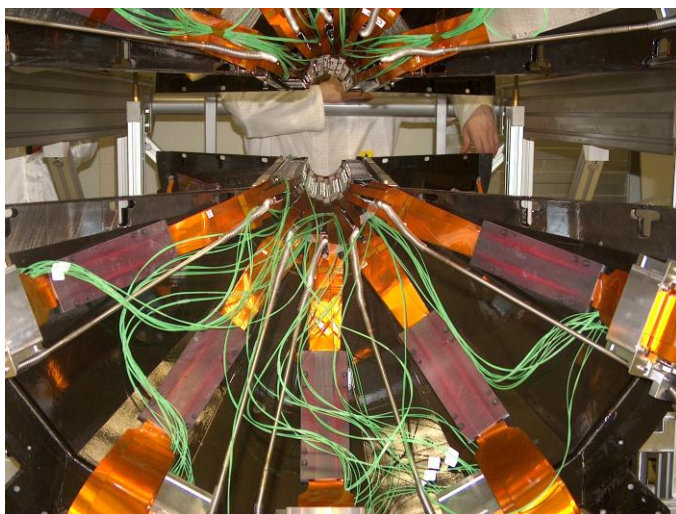
CF Thermal Shield

Half barrel layer 1





# Barrel integration test

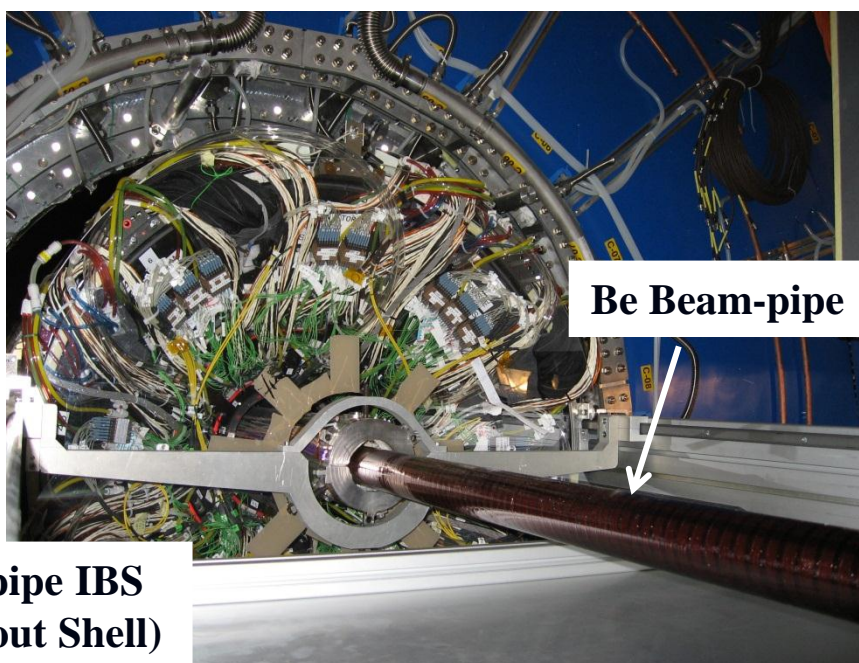




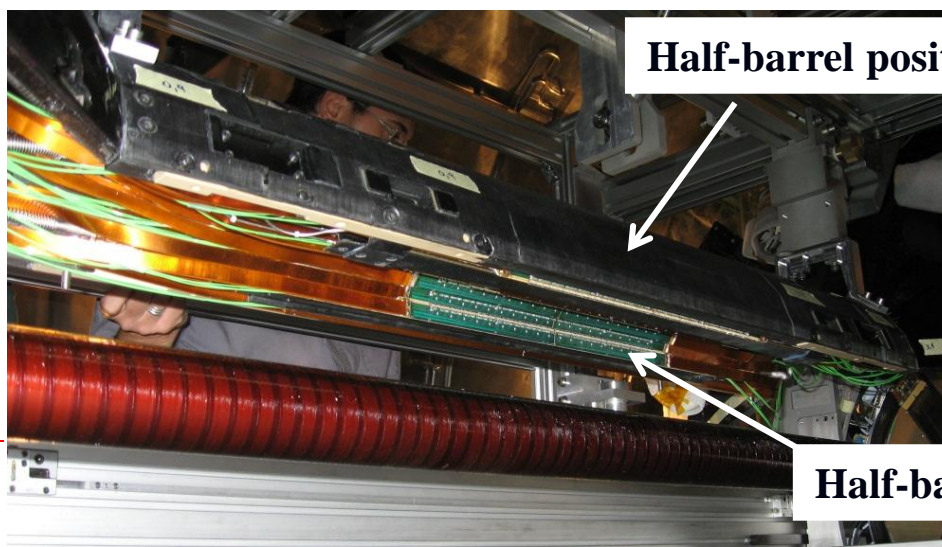
# SPD installation in ALICE



**Removal of the beam-pipe IBS  
(Installation and Bake-out Shell)**



**Be Beam-pipe**

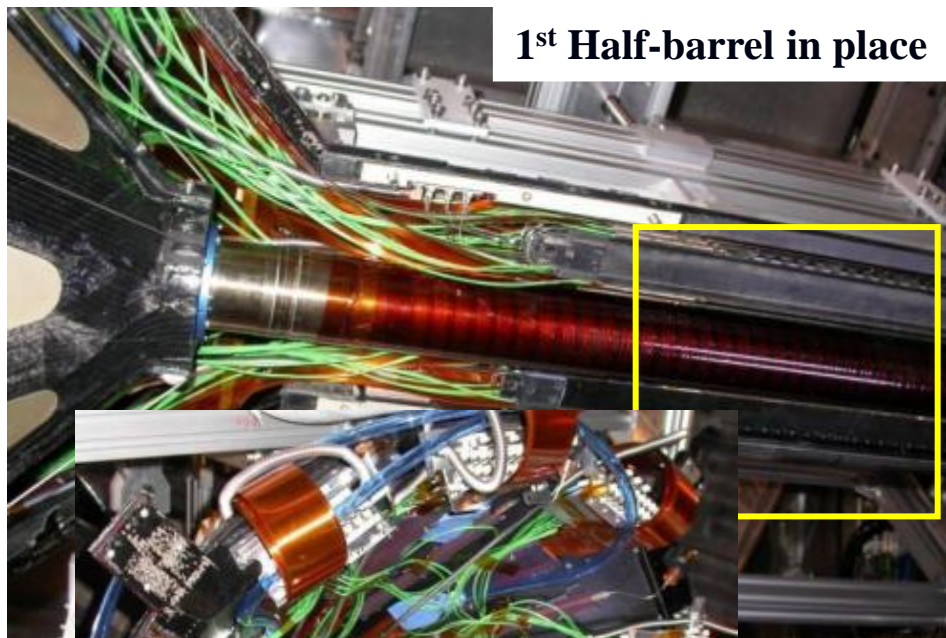


**Half-barrel positioning**

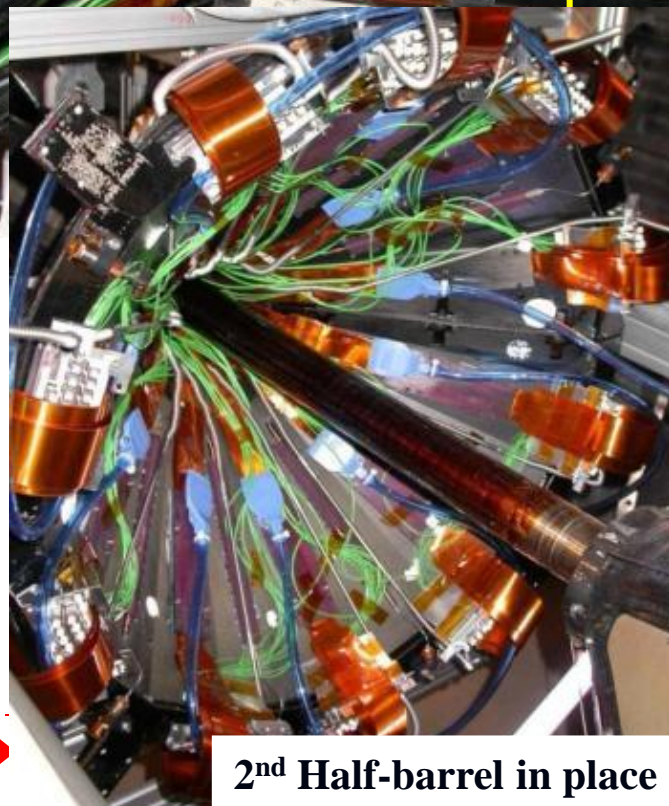
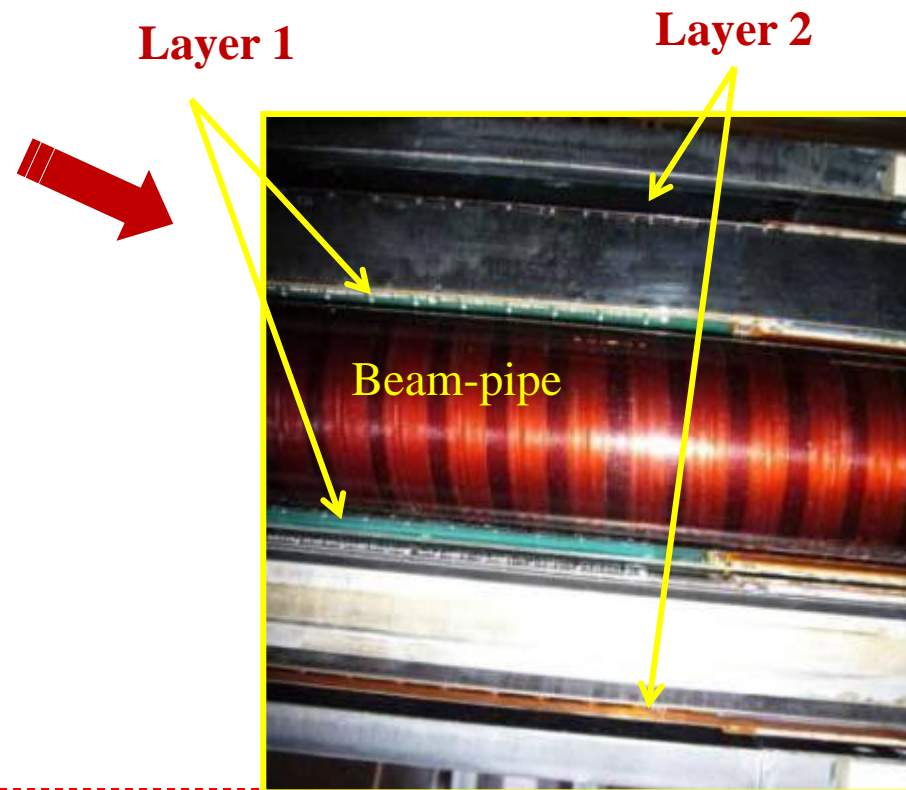
**Half-barrel layer 1**

# SPD installation in ALICE

1<sup>st</sup> Half-barrel in place



SPD Internal mean radius  $\approx 39$  mm  
Beam pipe outer radius = 29.8 mm



2<sup>nd</sup> Half-barrel in place



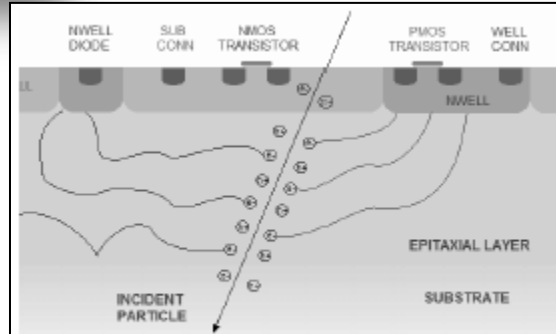
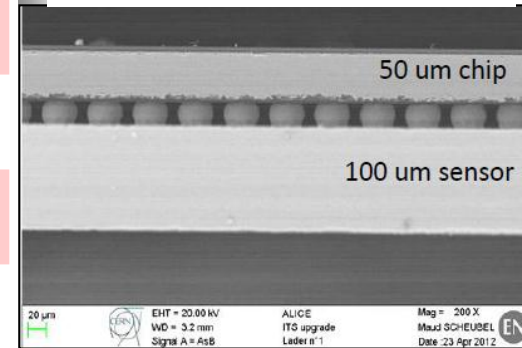
# Material budget summary table

| SPD Component                         | Some details   | Thickness (μm) | X/X0 (%)    | Contribution to the total X/X0 (%) |
|---------------------------------------|--|----------------|-------------|------------------------------------|
| <b>Silicon</b>                        | Sensor + FEE + interconnection                       | 350            | 0.38        | 33                                 |
| <b>Electrical bus</b>                 | 5 Al/polyimide layers + SMD components               | 280            | 0.48        | 42                                 |
| <b>Mechanical support and cooling</b> | Carbon fiber + tube                                  | 200            | 0.19        | 17                                 |
| <b>Others</b>                         | Glue (assembly / thermal contact) and grounding foil |                | 0.09        | 8                                  |
| <b>Total</b>                          |  |                | <b>1.14</b> | <b>100</b>                         |

# Towards the upgraded pixel layers

| SPD Component                  | Some details   | Thickness (μm) | X/X0 (%)    | Contribution to the total X/X0 (%) |
|--------------------------------|--|----------------|-------------|------------------------------------|
| Silicon                        | Sensor + FEE + interconnection                       | 350            | 0.38        | 33                                 |
| Electrical bus                 | 5 Al/polyimide layers + SMD components               | 280            | 0.48        | 42                                 |
| Mechanical support and cooling | Carbon fiber + tube                                  | 200            | 0.19        | 17                                 |
| Others                         | Glue (assembly / thermal contact) and grounding foil |                | 0.09        | 8                                  |
| <b>Total</b>                   |  |                | <b>1.14</b> | <b>100</b>                         |

Hybrid thinned to 150 μm (0.16 % of X0)

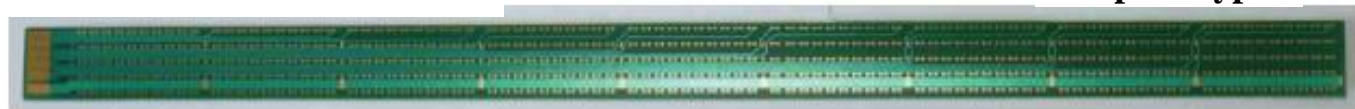


Monolithic thinned to 50 μm (0.053 % of X0)

See C. Gargiulo's talk

Electrical Bus:  
double Al/polyimide layer  
(0.075 % of X0)

1<sup>st</sup> prototype

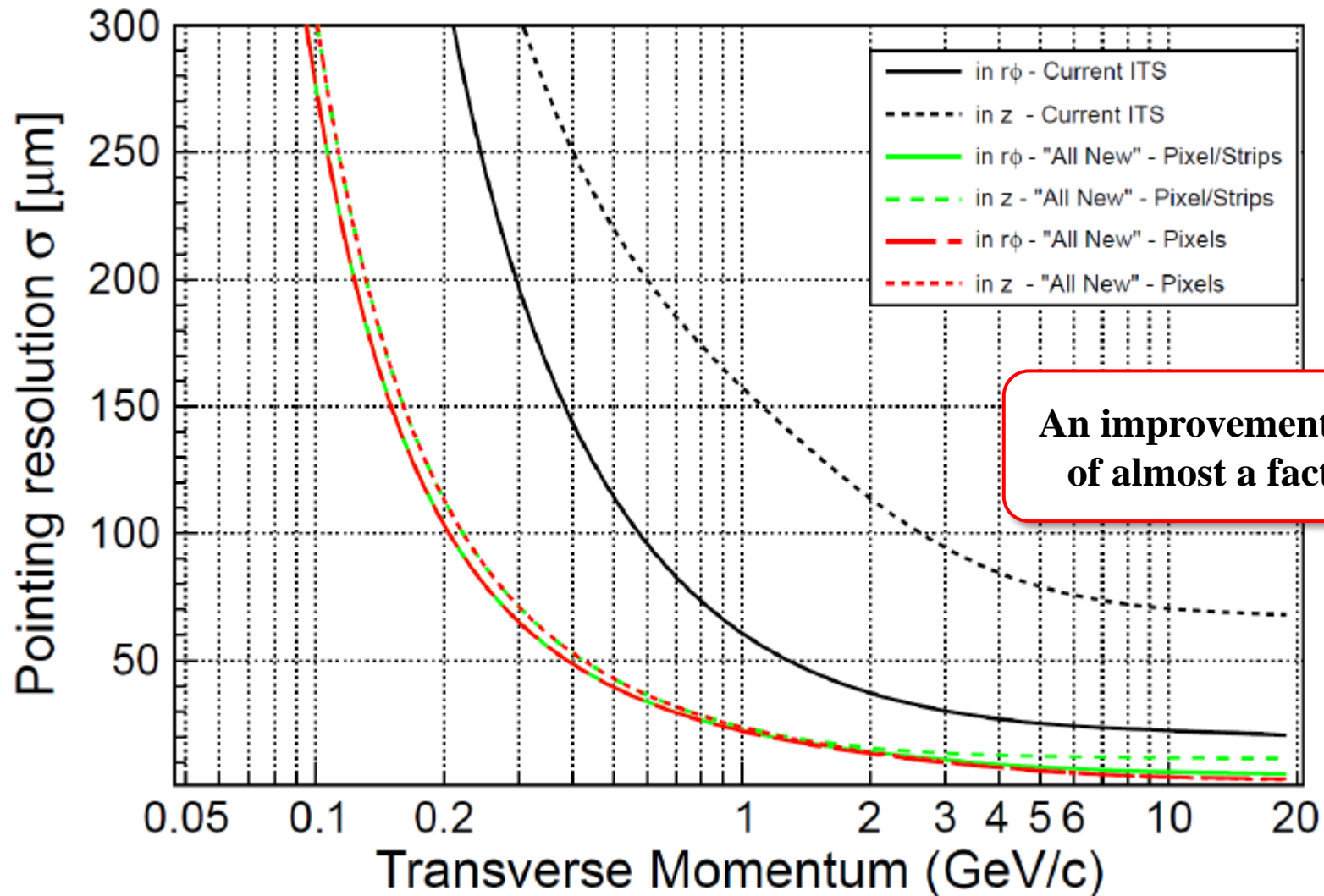


# Back to the previous considerations



- ▶ The key requirements to obtain good tracking performance are:
  - ▶ Small channel dimension
  - ▶ Low material budget
  - ▶ First layer as close as possible to the interaction point
  
- ▶ The silicon pixel detector in ALICE
  - ▶ Channel dimension:  $50 \mu\text{m}$  ( $r\phi$ ) x  $425 \mu\text{m}$  ( $z$ )
  - ▶ Material budget: 1.14 % of  $X_0$
  - ▶ Mean sensor position of the first layer = 39 mm
    - ▶ Beam pipe outer radius = 29.8 mm
  
- ▶ Target for the first layers of the upgraded ITS
  - ▶ Channels dimension:  $20 \mu\text{m}$  x  $20 \mu\text{m}$  (monolithic option)
  - ▶ Material budget: 0.3% of  $X_0$  (See C. Gargiulo's talk)
  - ▶ First tracking point: 22 mm
    - ▶ This will be possible by reducing the beam-pipe outer radius to 19.8 mm

# Back to the previous considerations





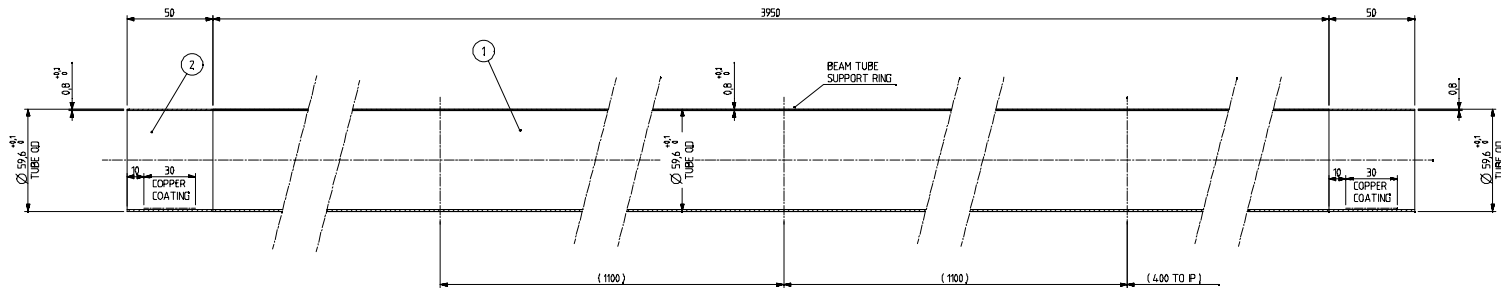
Thanks for your attention



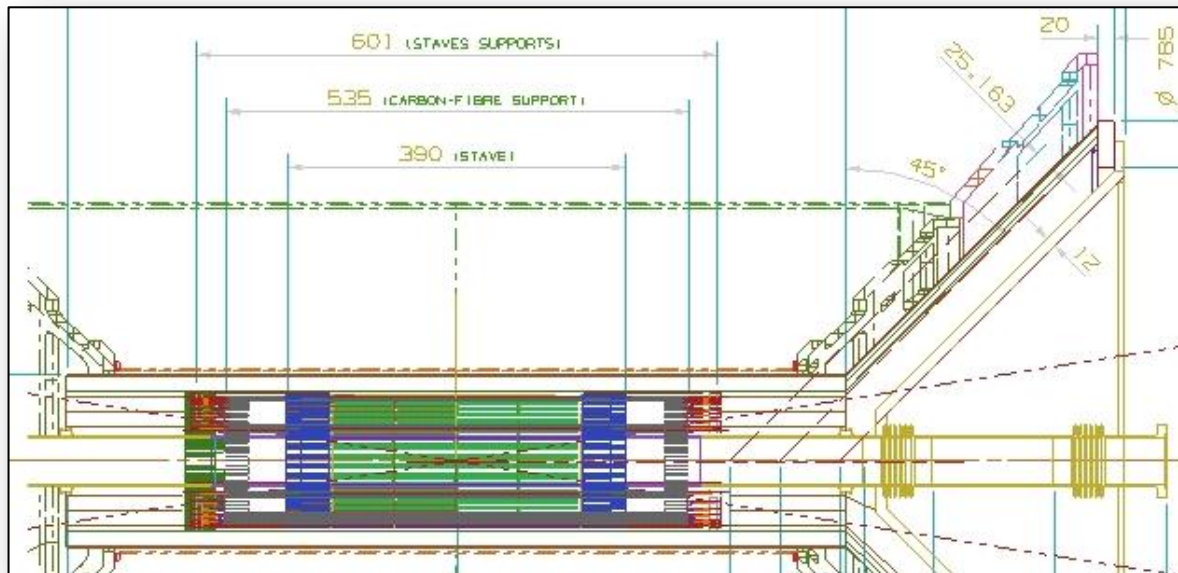
**ALICE**

# Spare





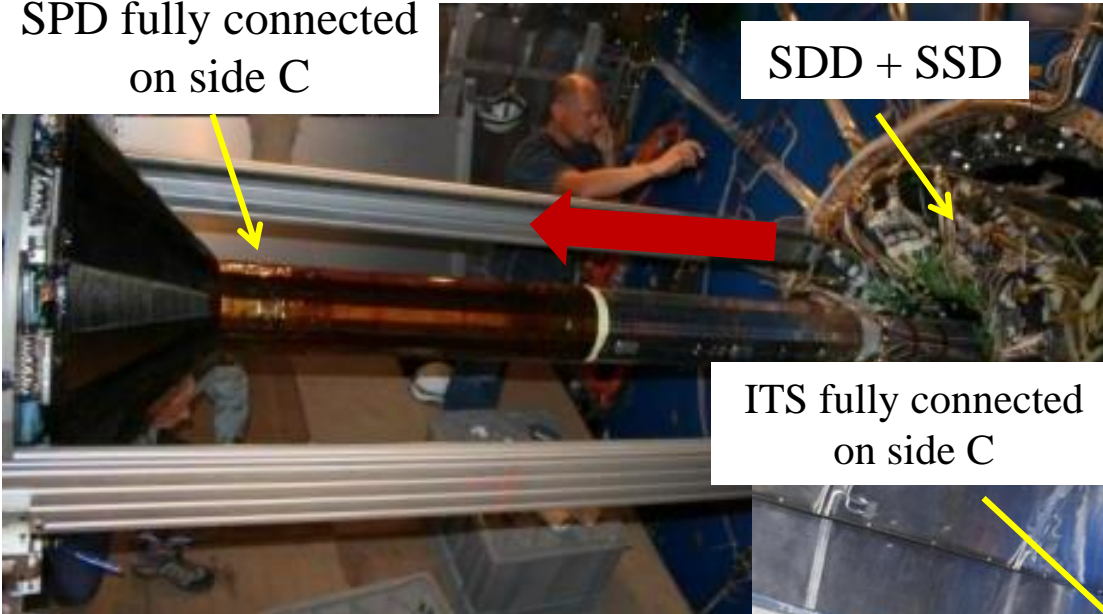
CP/1



|   | current ALICE | ALICE upgrade | ATLAS upgrade | CMS upgrade |
|---|---------------|---------------|---------------|-------------|
| innermost point (mm)                            | 39.0          | 22.0          | 25.7          | 30.0        |
| $x/X_0$ (innermost layer)                       | 1.14%         | 0.3%          | 1.54%         | 1.25%       |
| $d_0$ res. $r\phi$ ( $\mu\text{m}$ ) at 1 GeV/c | 60            | 20            | 65            | 60          |
| hadron ID $p$ range (GeV/c)                     | 0.1–3         | 0.1–3         | –             | –           |

# ITS installation: summer 2007 (phase 2)

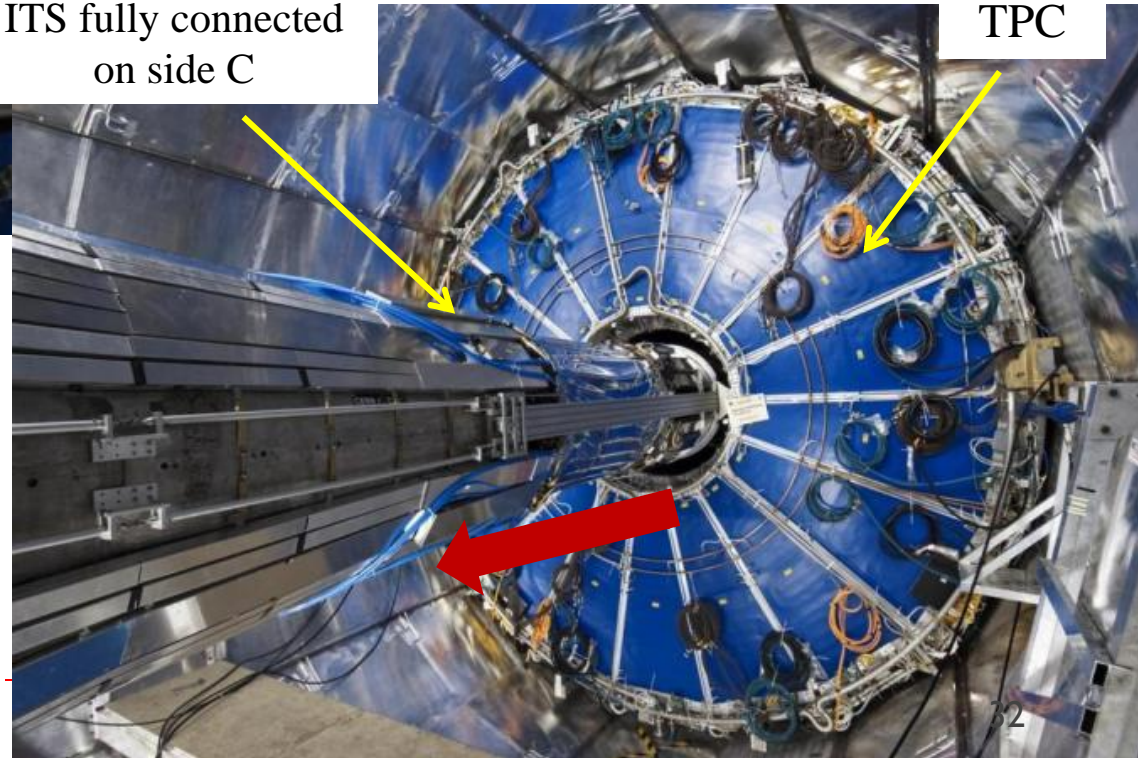
SPD fully connected  
on side C



SDD + SSD

SDD+SSD moved over the  
SPD to form the ITS

ITS fully connected  
on side C



TPC

TPC moved over the ITS