A fast, low-power, multichannel 6-bit ADC ASIC with data serialisation

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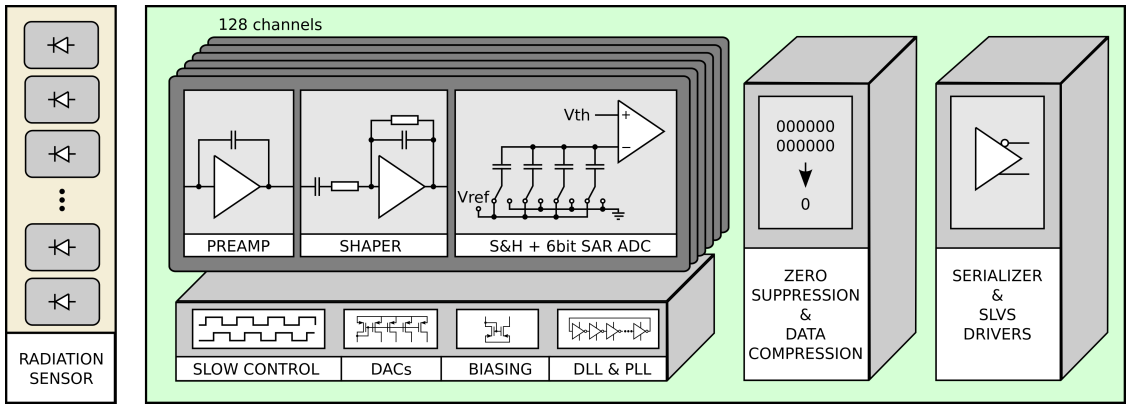
Outline

- Motivation
- Architecture of multichannel ADC ASIC
- Readout modes
- Measurement results
- Summary

Motivation

- Multichannel readout systems comprising front-end and multi-bit digitisation in each channel require:
  - fast, low-power ADC
  - data serialisation and fast data transmission
- Example HEP applications, we are working for:
  - LHCb strip tracker (6-bit ADC)
  - ILC luminosity detector (higher resolution ADC)



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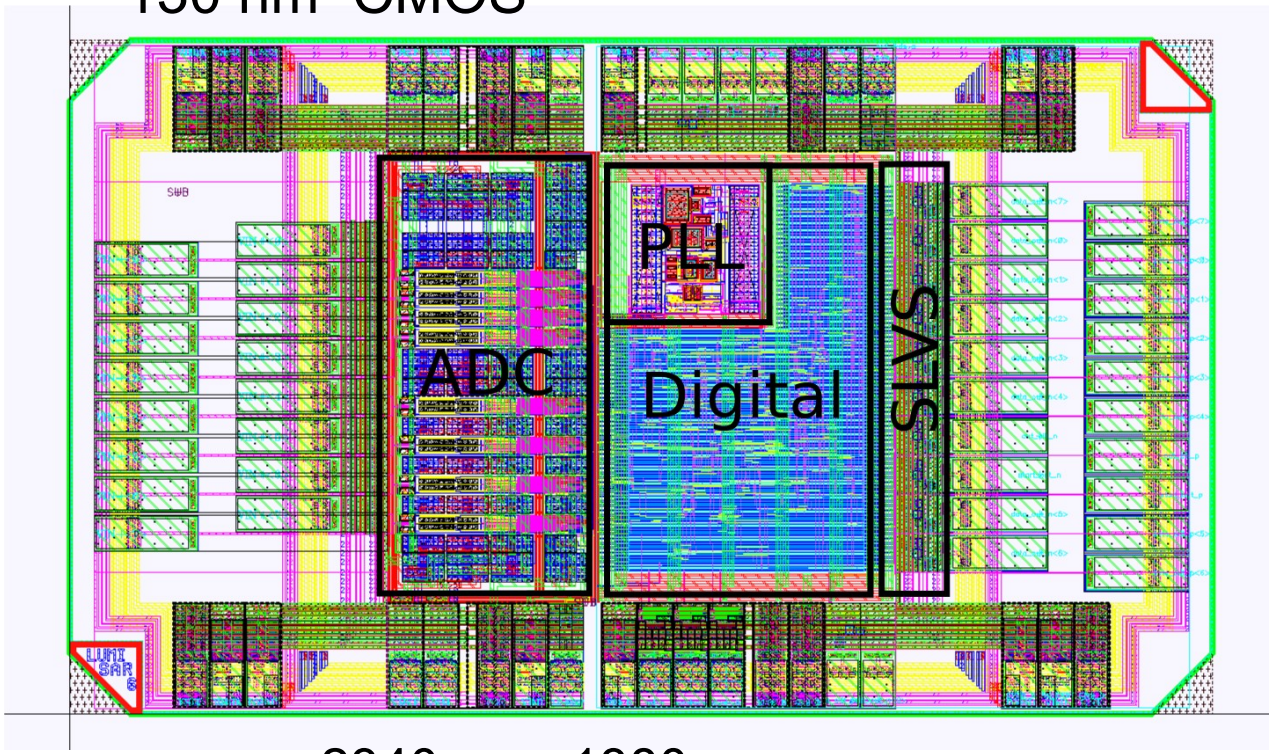
Architecture of multichannel ADC ASIC
Layout diagram

130 nm CMOS

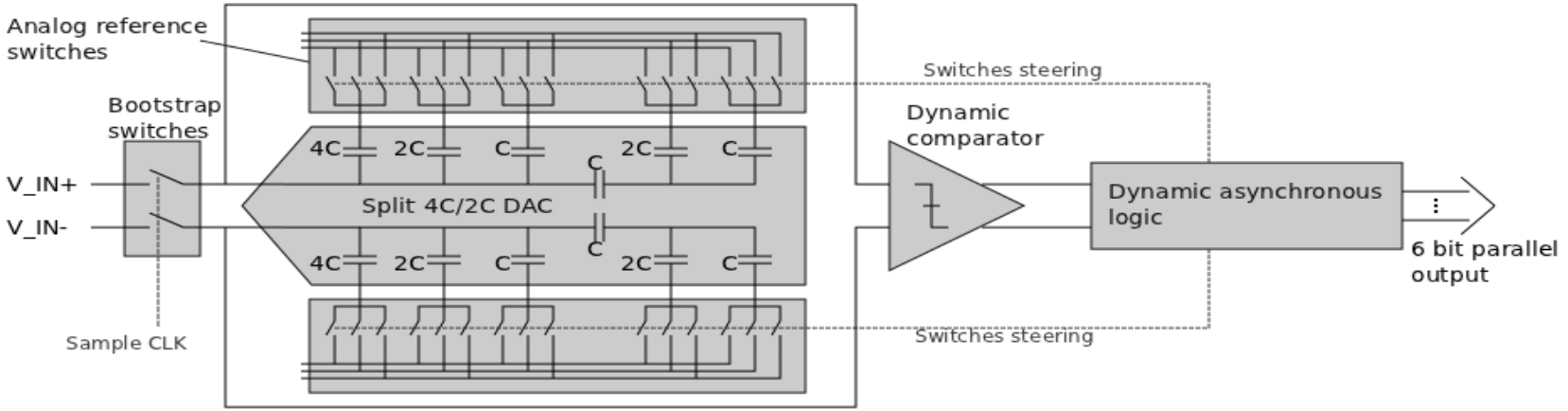


2340um x 1380um

ADC prototype contains:

- 8 channels of 6-bit SAR ADC
- Readout circuitry (multiplexer & serialiser)
- PLL for generation of high frequency readout clock
- SLVS I/O circuitry
- Staggered pads
- Command decoder

SAR ADC architecture, design and results



Architecture of ADC:

- Differential segmented/split DAC with MCS scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

Measured performance:

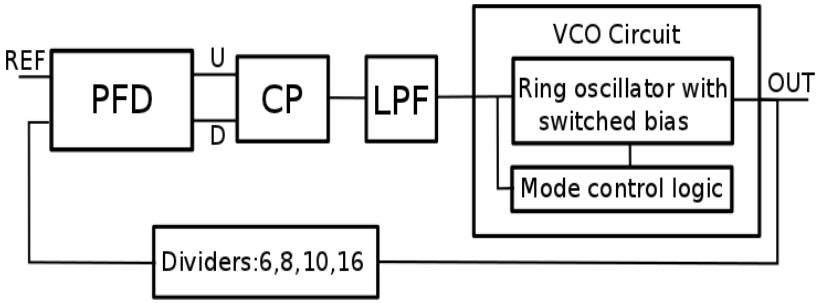
- Resolution, ENOB 6 bits, ~5.85
- Variable sampling frequency up to ~80 MS/s
- Power consumption at 40 MS/s 0.35 mW

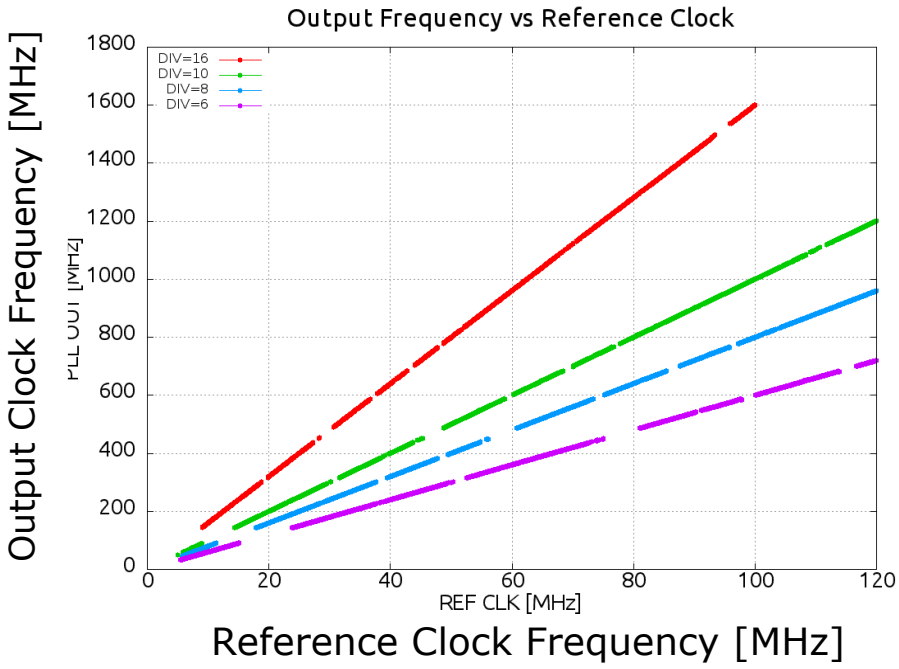
K. Świentek, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, T. Szumlak "SALT – new silicon strip readout chip for the LHCb Upgrade", TWEPP2013 23-27 September 2013, Perugia Italy

PLL architecture, design and results

Main features:

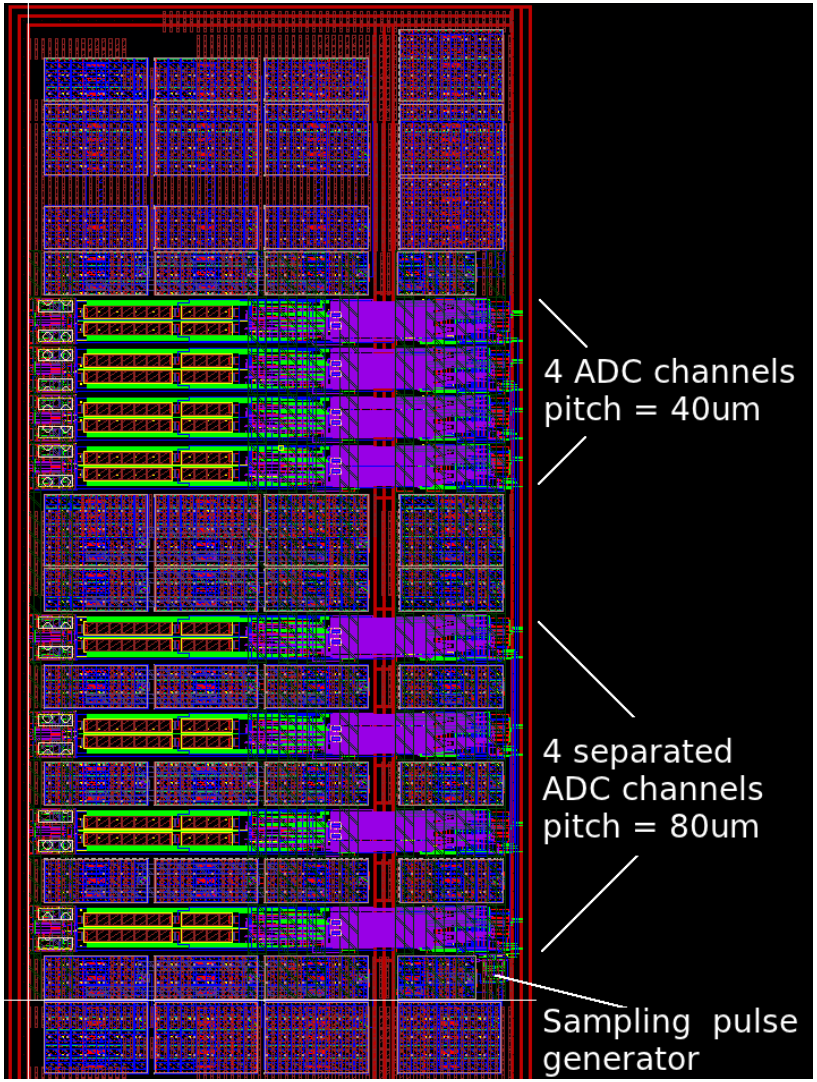
- General purpose PLL block
- Very wide output frequency range: **20MHz – 1.6GHz** (SLVS limit.)
- Gaps in frequency are found in the prototype – to be eliminated...
- 16 VCO modes – automatically (or manually) changed
- Jitter 15-70 ps (to be improved...)
- Power consumption **~0.6mW @ 1GHz**
- Different loop division factors: **6**, **8**, 10, 16
- Size 300um x 300um





M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, "Development of variable frequency, power Phase-Locked Loop (PLL) in 130nm CMOS technology , TWEPP2013 23-27 September 2013, Perugia Italy

Layout of 8 channels of SAR ADC



- ADC channels designed in 2 different pitch values:
  - 40 um (4 channels)
  - 80 um (4 channels)
- Decoupling capacitances in the gaps between channels

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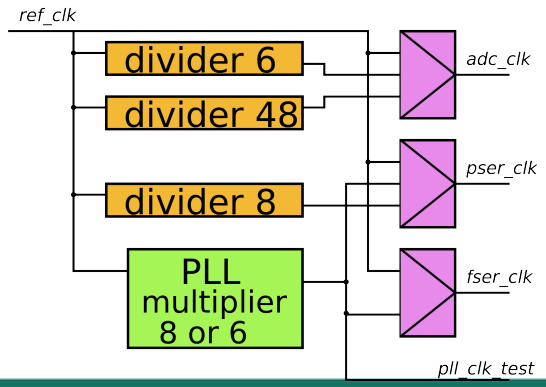
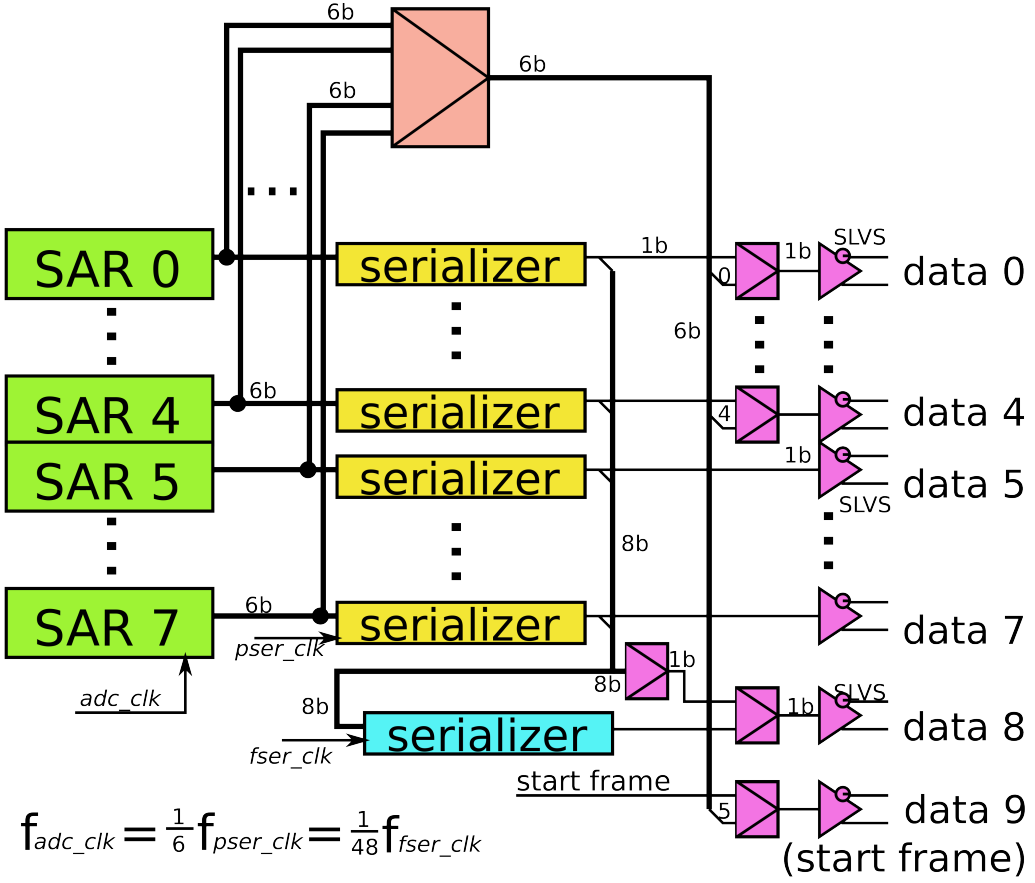
8 channel ADC ASIC
Readout modes - block diagram

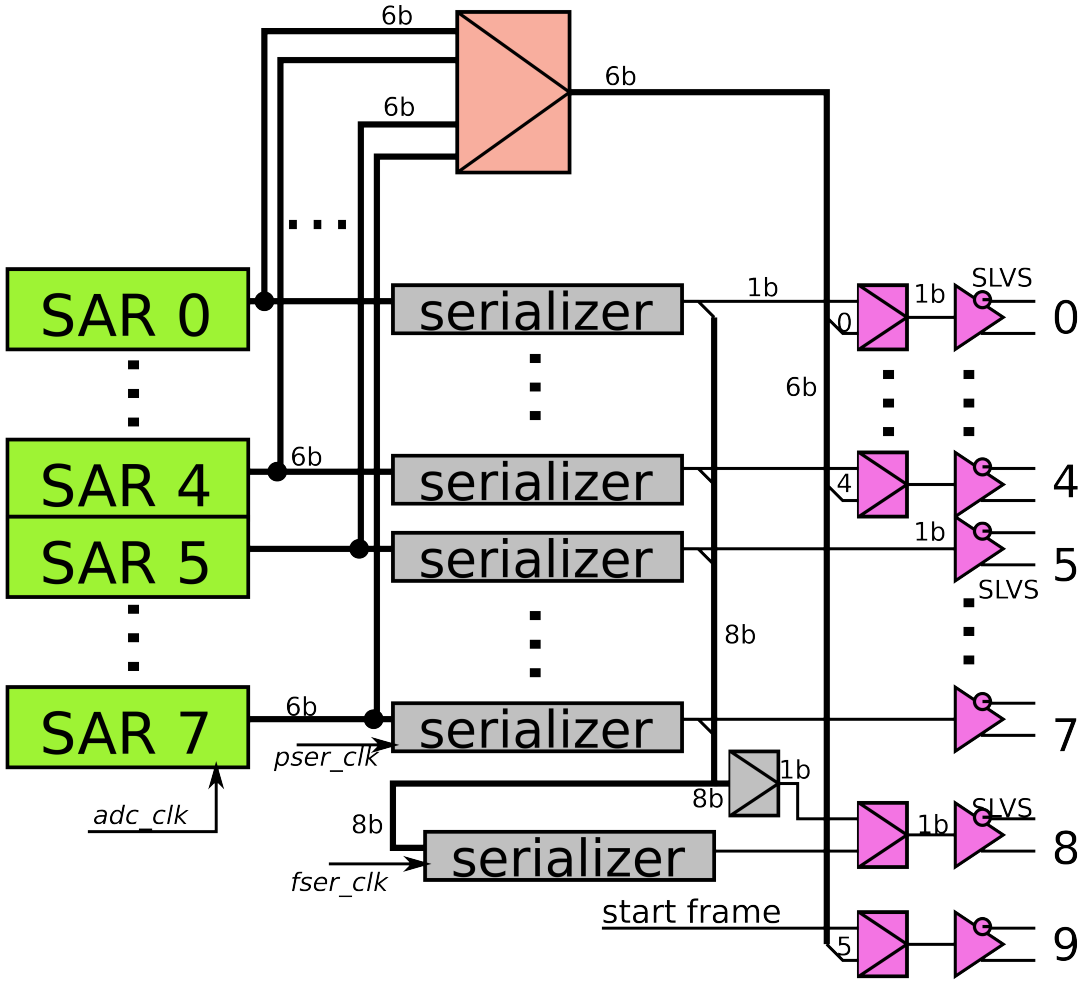
- Three modes
  - test
  - partial serialisation
  - full serialisation
- Two clock generation schemes (serialisation)
  - by division
  - by multiplication





Readout modes
Test readout mode

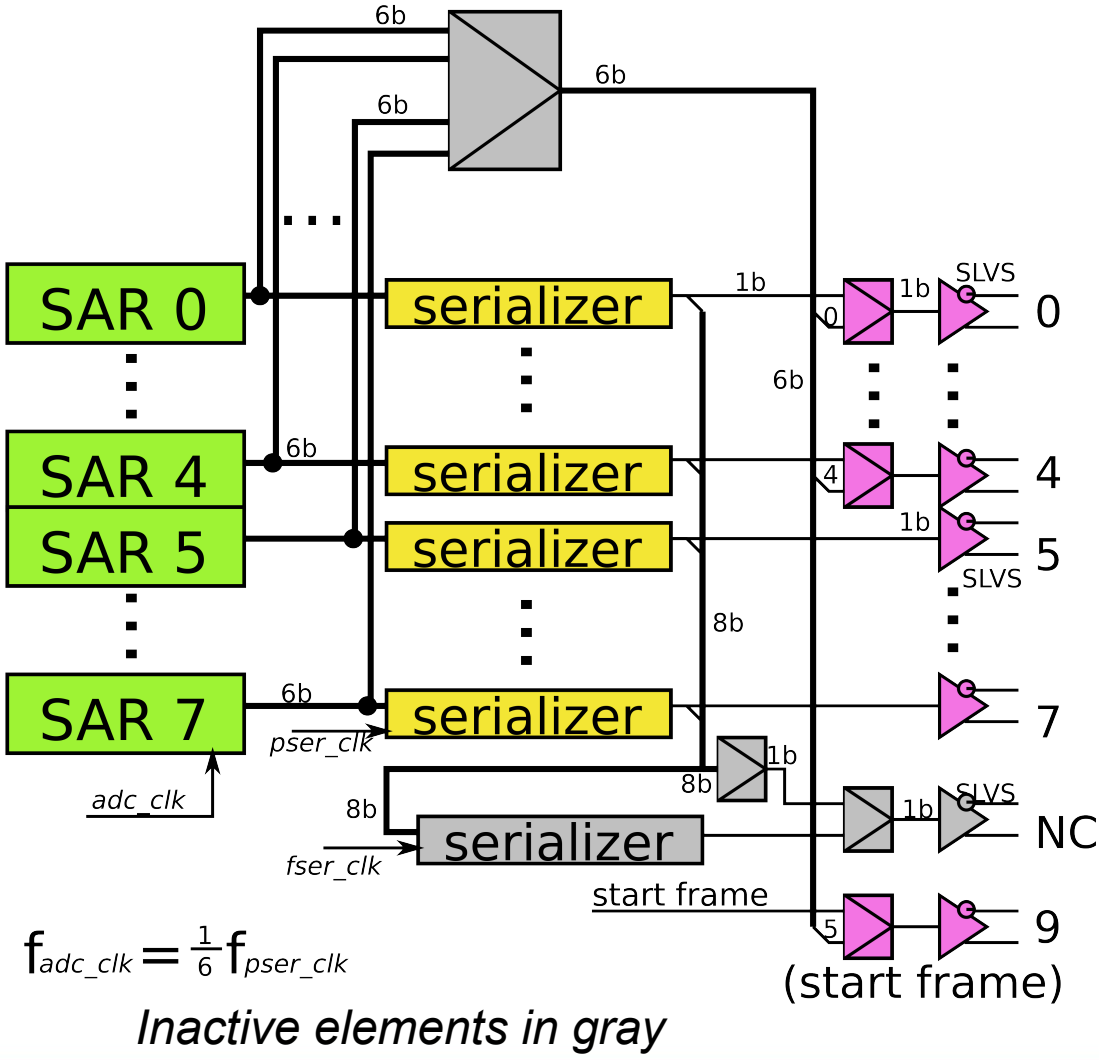
- 6 bits of single ADC are sent through 6 SLVS outputs
- Only one clock frequency = sampling frequency
- One SAR ADC can be tested at a time
- ADC sampling frequency not limited by serializer



Inactive elements in gray

Readout modes
Partial serialisation mode

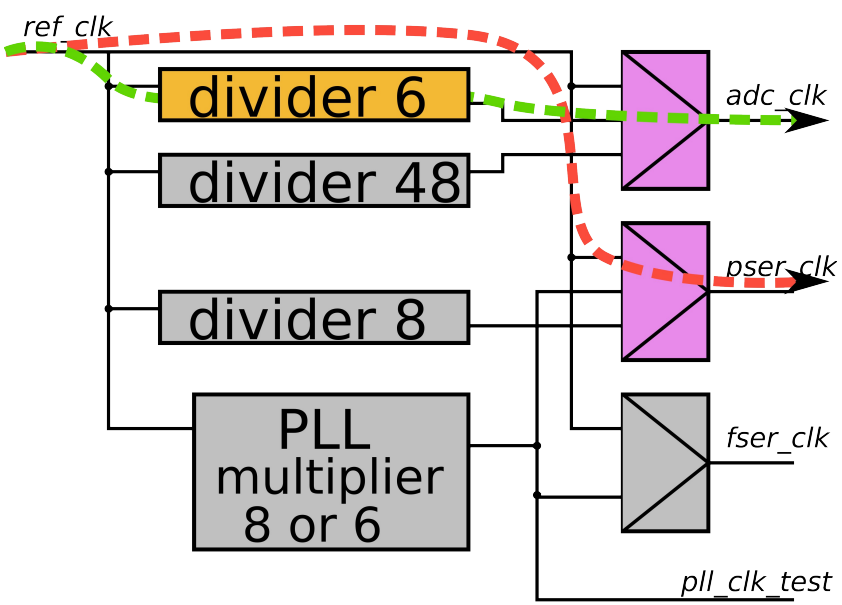
- Each ADC channel has its own serial output – all ADCs readout in parallel
- Needs two clock frequencies
  - slow – sampling
  - fast (x6) – readout
- Two clock generation schemes available (next slide...)

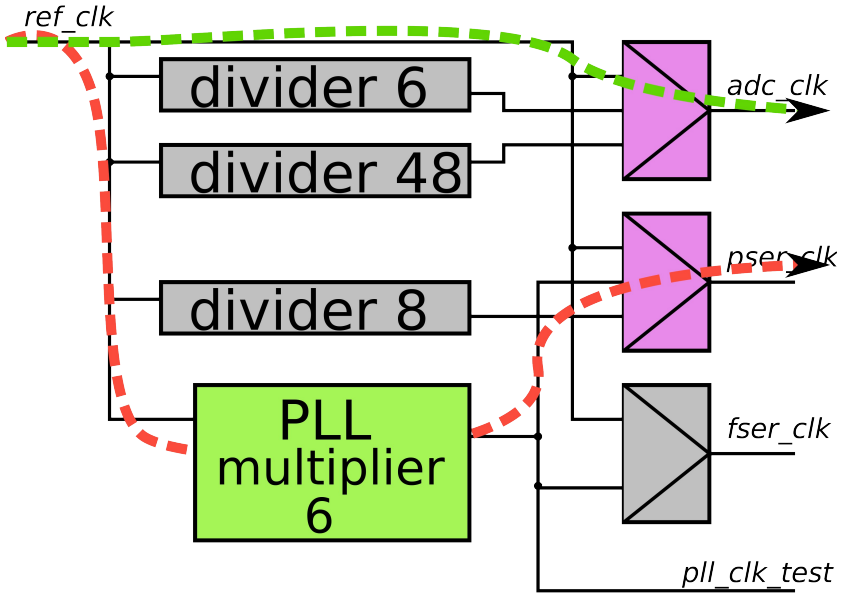


Inactive elements in gray

Readout modes
Partial serialisation clock generation

Inactive elements in gray

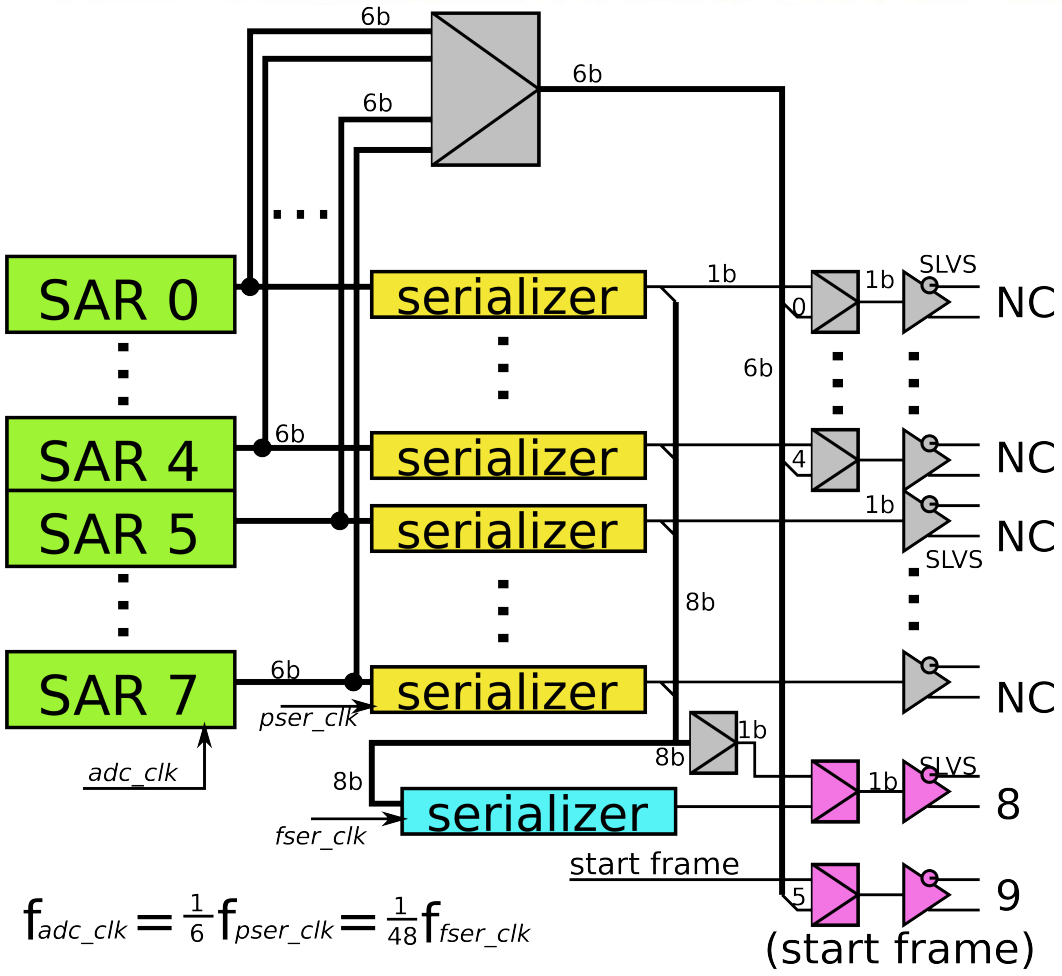




- Divider configuration
  - fast external readout clock
  - slow sampling clock generated by division
- PLL configuration
  - slow external sampling clock
  - fast (x6) readout clock generated by PLL

Readout modes
Full serialisation mode

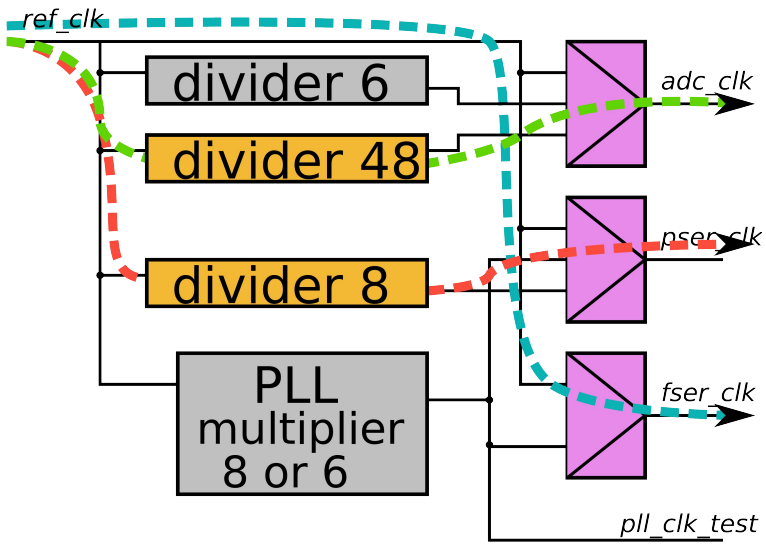
- One data output for all channels
- Uses partially serialised data – needs 3 clocks
  - slow – sampling
  - medium (x6) – partial serialisation
  - fast (x48) – readout
- The slowest sampling frequency (~7.5 MHz) – limited by readout

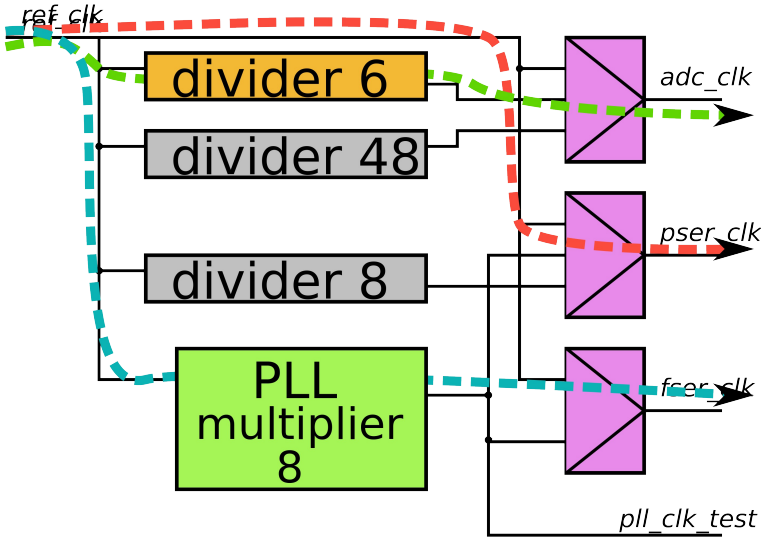


Inactive elements in gray

Readout modes
Full serialisation clock generation

Inactive elements in gray





- Divider configuration
  - fast clock external
  - slow and medium clocks achieved by division
- PLL configuration
  - medium clock external
  - slow clock generated by division
  - fast clock generated by PLL

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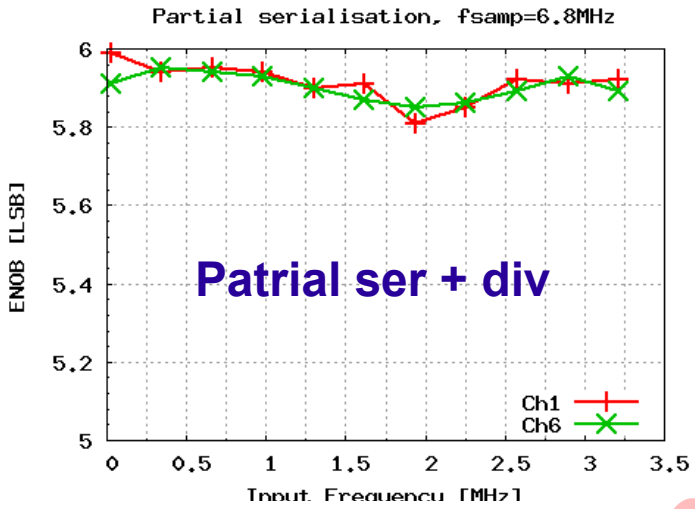
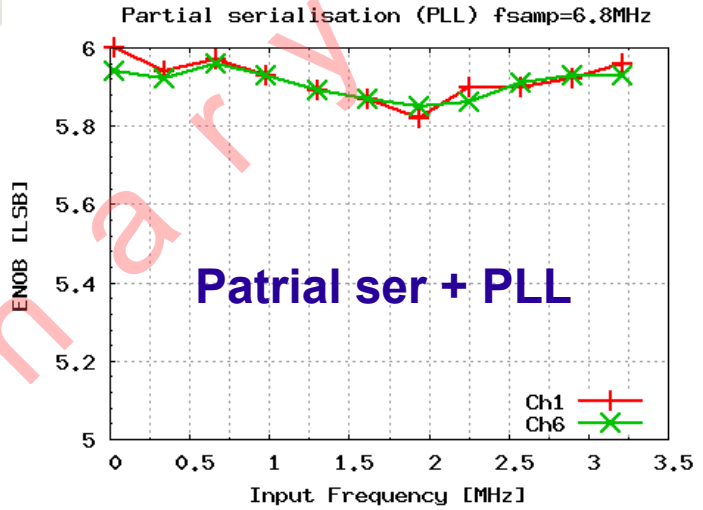
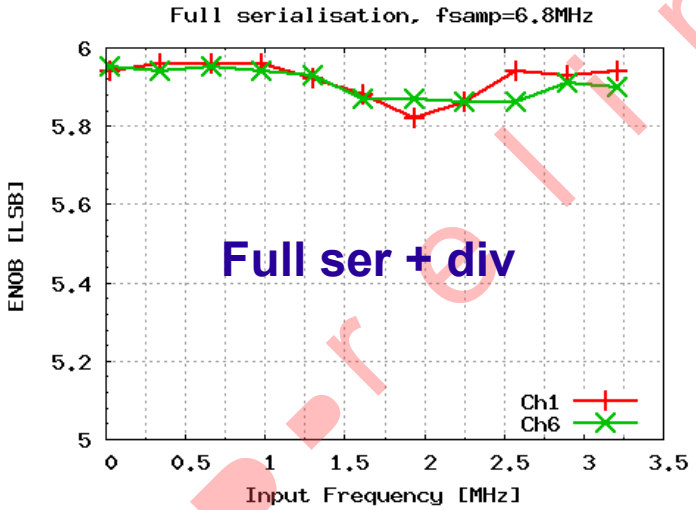
Present measurement assumptions/constraints Will be improved in the future...

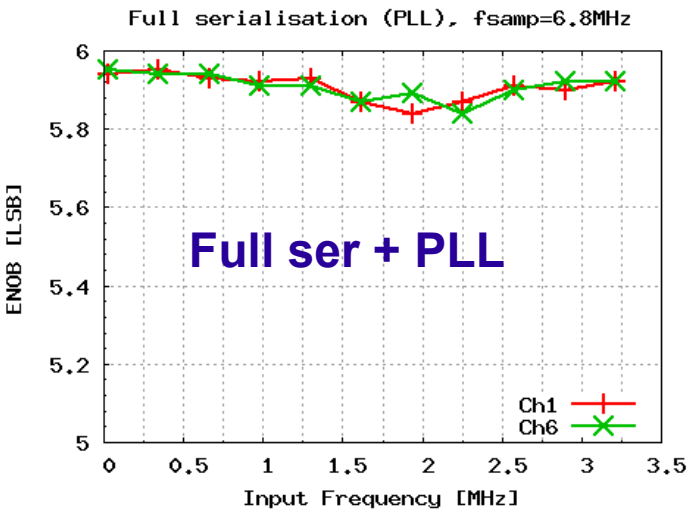
- Input signal can be connected to up to 2 channels only – temporary setup limitation
- Channels 1 & 6 chosen:
  - different pitch (40 vs 80 um)
  - no boundary effects
- Only Effective Number of Bits (ENOB) is shown
- Two regimes of sampling frequency
  - up to ~7MHz, available in all modes
  - up to ~50 MHz, more interesting region, but high sampling frequencies not possible in full serialisation mode

Measurement results
Different readout modes, fs=6.8 MHz



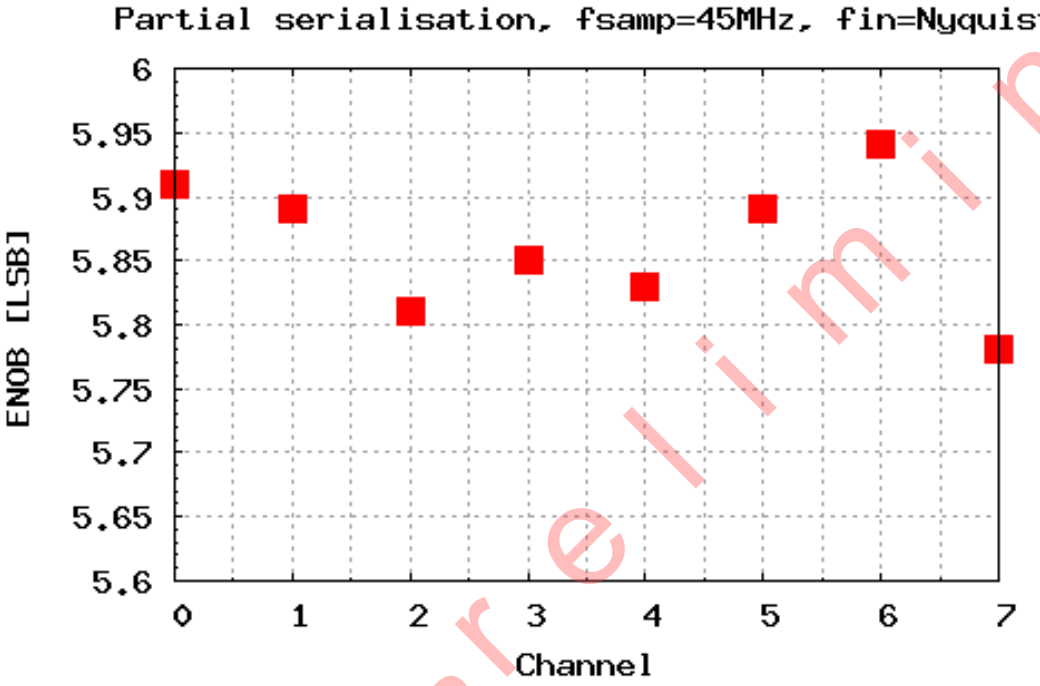






Very good and consistent results obtained in all modes!

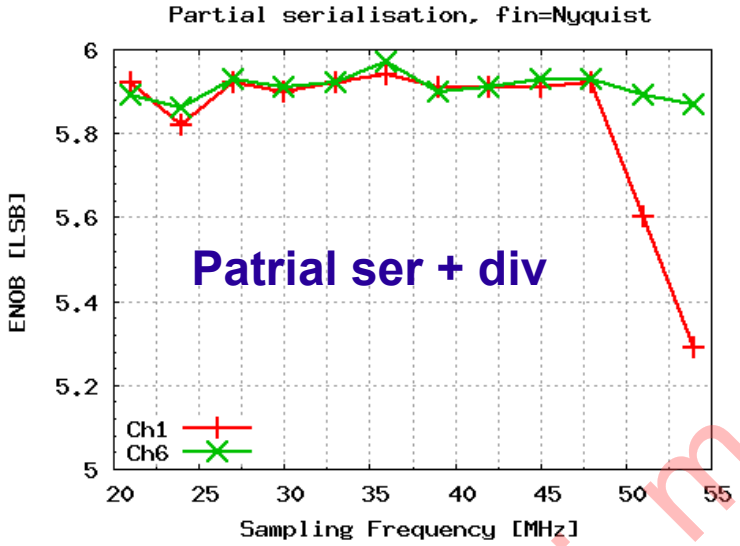
Measurement results
ENOB uniformity between channels

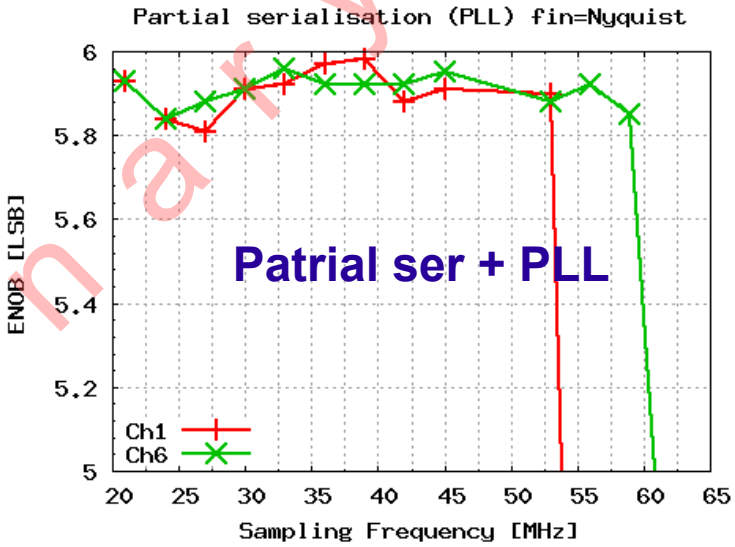


- Measured for pairs of channels – setup limitation: (0,7), (1,6), (2,5), (3,4) in partial serialisation mode
- fsamp = 45MHz
- fin, Nyquist (~22MHz)

Very good ENOB uniformity over channels

Measurement results
ENOB vs sampling frequency



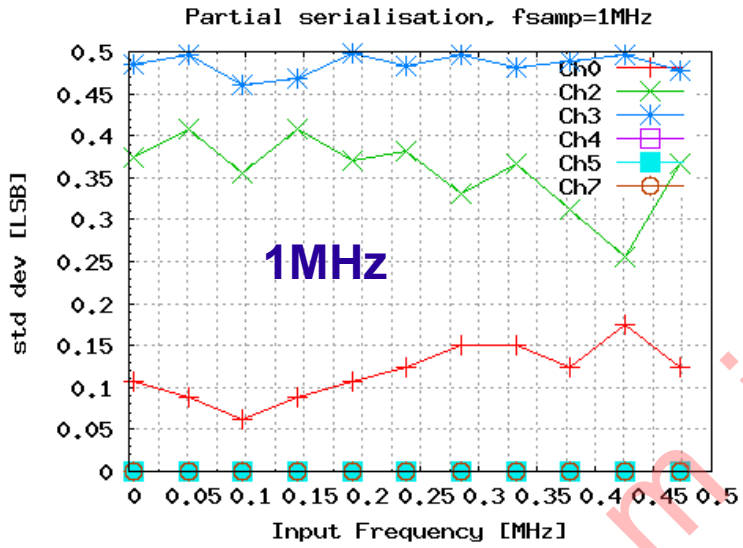


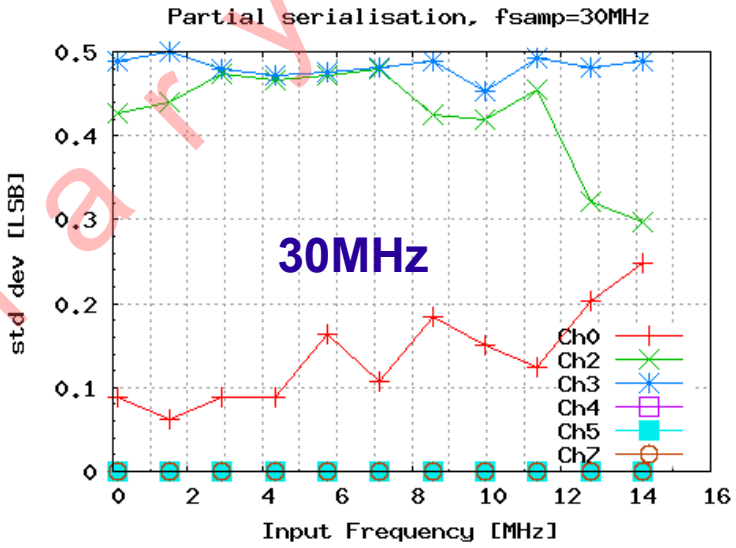
- Maximum frequency of ext. generator is 330MHz, giving max fsamp = 55MHz
- ADC works to ~54 MHz

- With PLL higher frequencies can be obtained
- ADC works up to ~60 MHz

Channel 6 (large pitch) faster than channel 1 (small pitch)

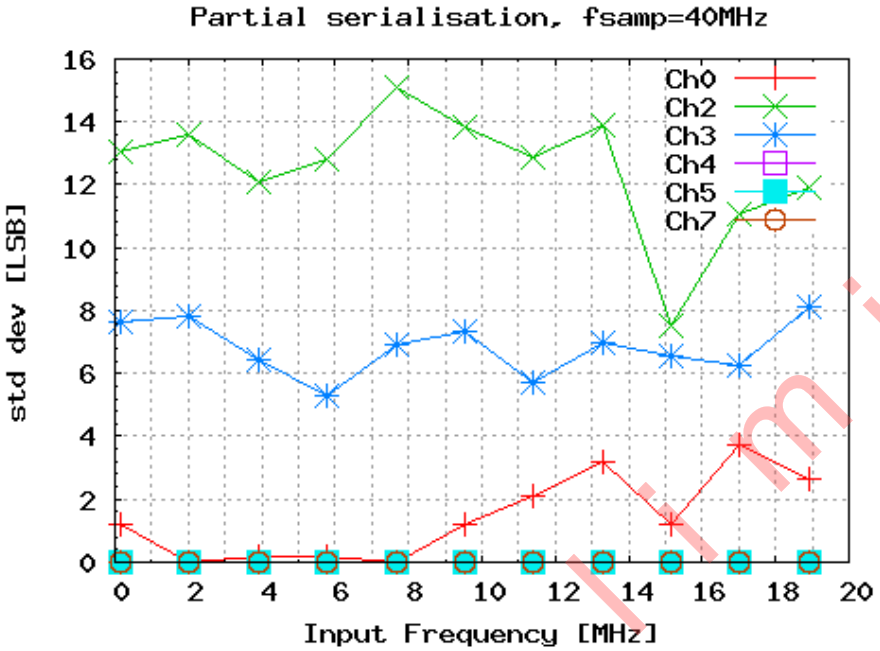
Crosstalk effects, fsmp < 40 MHz





- Signal in channels 1 & 6
- Standard deviation calculated in channels without signal
- Different behavior of ch 0-3 (small pitch) and 4-7 (large)
  - 4-7 are completely quiet, no “crosstalk” effect observed
  - 0-3 have small “crosstalk” slightly dependent on frequency, but since the effect is highest in non-neighbour channel (ch3) it is not pure crosstalk...

Crosstalk (?), fsamp > 40MHz



- Large difference between small and large pitch channels
- Ch 4-7 still quiet
- Ch 0-3 large effect

- Distant channels with good decoupling work well (4-7)
- Channels 0-3 show large “crosstalk” – presently under study – decoupling, power supply oscillations ?? ...

Summary

- Preliminary tests of 8-channel 6-bit SAR ADC have been done
- All ADCs in all readout modes are fully operational
  - partial (per channel) and full (per chip) serialisation
  - with internal PLL or dividing high freq. ext. clock
- Multichannel ADC works up to ~60MHz sampling frequency (readout limitation)
- Distant channels (80um pitch) with good decoupling show better performance than channels with 40um pitch; “crosstalk” effect needs further investigation
- Total power consumption not measured yet (8*0.35mW + 0.3mW + readout = ~3mW + readout, estimation from single ADC and PLL meas. @40MHz)

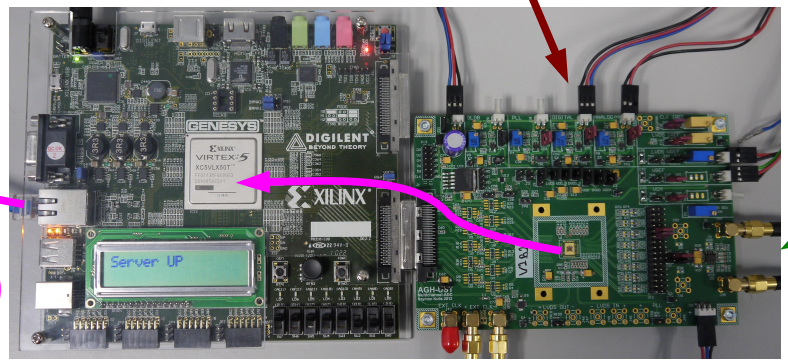
Thank you

Performance measurements
Measuring setup

DFT and data analysis – custom software

Power supply

Differential function generator – Agilent 81160A



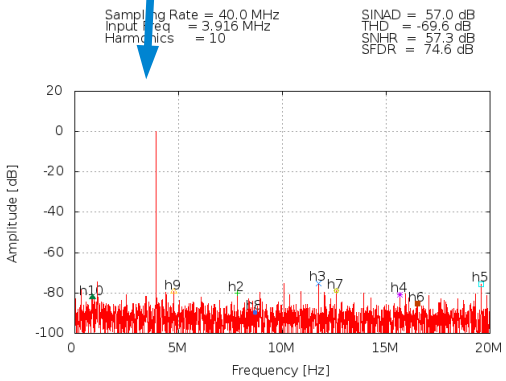
Input sine

Sample clock

Results

Sampled data (**low bitrate**)

Sampled data (**high bitrate**)



DAQ – receives fast transmission from ADC, captures the data and sends to PC via Ethernet for offline analysis

Measuring ADC dynamic characteristics
Theoretical summary

DFT of ADC transfer function → spectrum for given sampling frequency and input sine frequency

$$F(T_{ADC}) = f(f_{sample}, f_{sine})$$

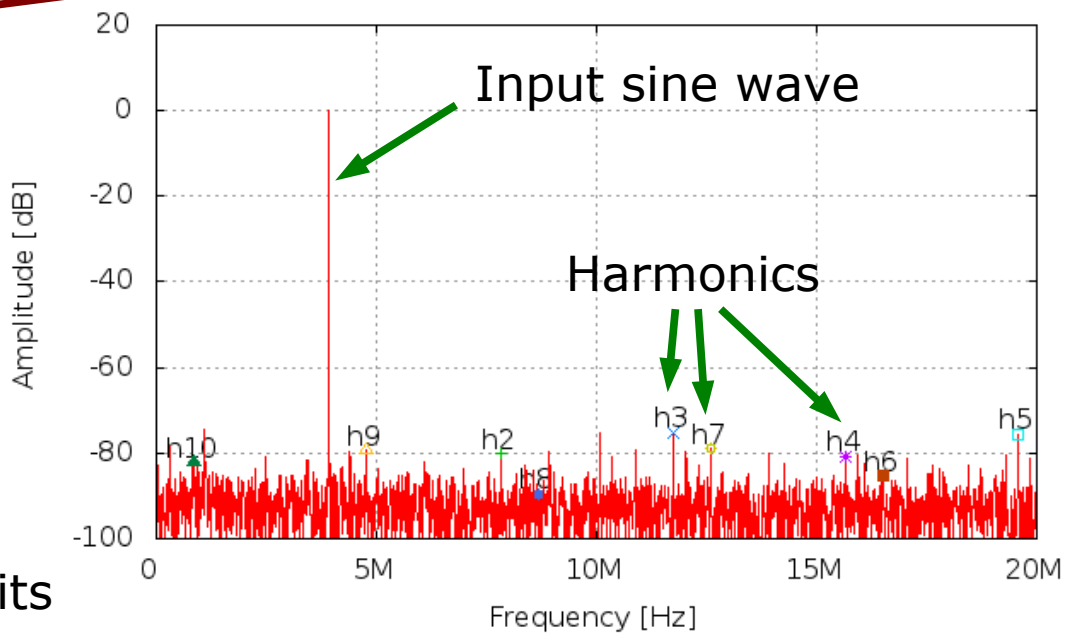
Sampling Rate = 40.0 MHz
Input Freq = 3.916 MHz
Harmonics = 10

SINAD = 57.0 dB
THD = -69.6 dB
SNHR = 57.3 dB
SFDR = 74.6 dB

Dynamic metrics calculated from obtained DFT, i.e.:

- **SINAD** – signal to noise and distortion (harmonics) ratio

$$SINAD = 20\log_{10}\sqrt{\frac{X_{sine}^2}{\sum_{k=1,k\neq sine}^{N/2} X_k^2}}$$

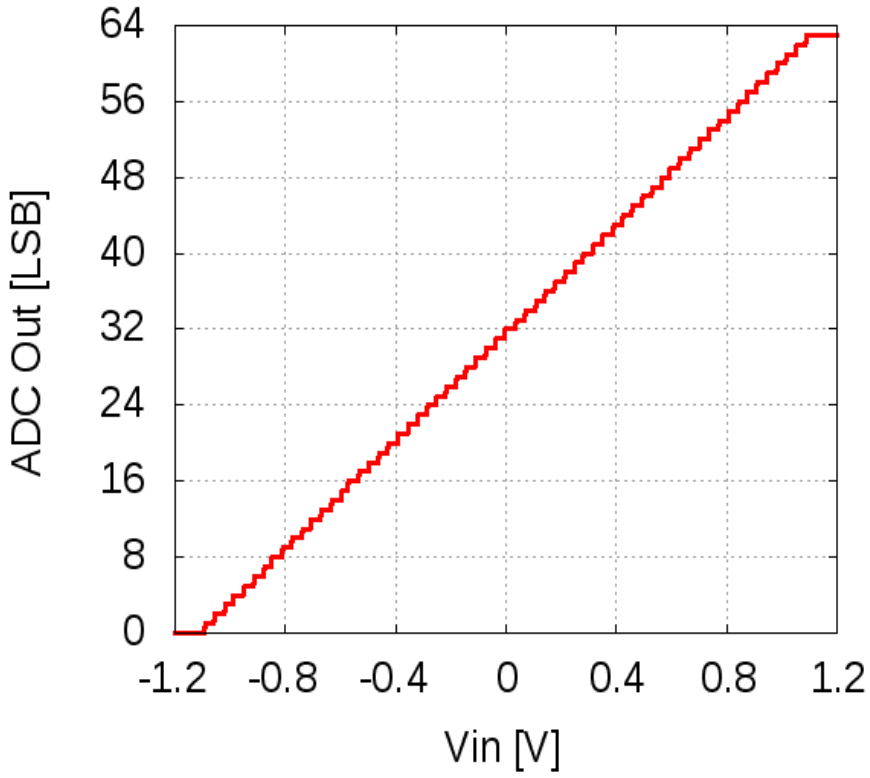


- **ENOB** – effective number of bits

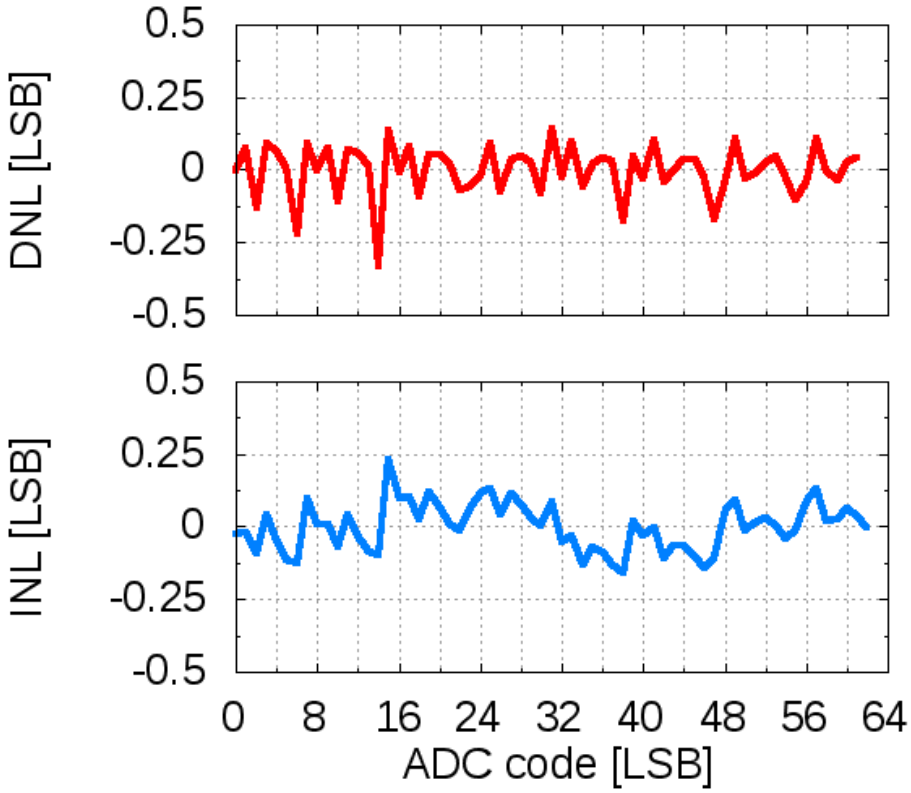
$$ENOB = \frac{SINAD - 1.76}{6.02}$$

6-bit SAR ADC
Static tests – linearity (@50 MS/s)

Transfer function



INL/DNL measurements



- Measurements show that ADC works very well
- At 50MHz sampling frequency good linearity INL, DNL < 0.4 is seen