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# A fast, low-power, multichannel 6-bit ADC ASIC with data serialization

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The multichannel 6-bit ADC ASIC with data serialization was designed in view of LHCb Tracker System Upgrade. The first prototype was designed and fabricated in CMOS 130 nm technology. The main chip components are 8 channels of fast, very low power (<0.5 mW per channel) 6-bit SAR ADCs, data serialization circuitry based on ultra-low power internal PLL and fast SLVS I/O differential interface. The nominal ADC sampling frequency is 40 MHz but the operation beyond 80 MHz is possible. Various modes of data serialization were implemented, the main three are: A) test mode - with 6 bits from the selected ADC sent to 6 SLVS differential outputs; B) partial serialization - when output bits of each ADC are serialized, with frequency multiplied six times by PLL, into separate SLVS output; C) full serialization - when output of all (6) bits of all (8) ADCs are serialized into one SLVS output.
In addition to standard operation the serialization circuitry contains also a block generating the test data (instead of using ADC output bits) which are serialized and sent out. This block is added for better ASIC testability and it allows to generate test patterns based on binary or pseudo-random counters. The ultra-low power (<1 mW) PLL was designed to generate clock in a wide frequency range, from tens of MHz to few GHz. The SLVS interface was designed for data rates beyond 1 GHz.

The description of the ASIC architecture and the results of measurements, in particular all main functionalities/blocks i.e. ADC, PLL, SLVS and serializer will be presented.

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