Contribution ID: **104** Type: **Oral**

The TDCPix ASIC: Tracking for the NA62 GigaTracker

Thursday 5 June 2014 17:10 (20 minutes)

The TDCPix is a hybrid pixel detector readout ASIC designed for the NA62 GigaTracker detector. The requirements are a single-hit timing resolution better than 200ps RMS, a hit loss of less than 1% in the presence of a (highly non-uniform) beam rate up to 1MHz/cmˆ2. This hit rate leads to an expected data rate at the output of the chip which can reach 6Gb/s.

The TDCPix comprises an asynchronously operating pixel array of 40 columns of 45 pixels, each 300 microns x 300 microns. This is instrumented with 40 Delay Locked Loop based time-to-digital converters connected to data buffering and concentrating logic. The read-out uses four 3.2Gb/s serialisers with the high speed clock being provided by a low-noise on-chip PLL. The high data rates negate the possibility of buffering whilst awaiting a trigger, thus a self triggering architecture has been adopted.

All configuration and state logic in the design deemed critical for the correct operation of the chip has been triplicated to provide increased single event effect tolerance. A number of on-chip digital-to-analogue converters provide threshold generation and trimming and are configurable through a single-signal configuration interface. The configuration and DAQ interfaces include a DC-balanced protocol layer permitting direct optical connections when the ASIC is installed in the experiment. Dedicated calibration circuitry is included to enable the required timing resolution to be reached.

The chip has been manufactured in a commercial 130nm process and testing is underway. A detailed description of the architecture and performance results will be presented.

Primary author: NOY, Matthew (CERN)

Co-authors: KLUGE, Alex (CERN); Dr AGLIERI RINELLA, Gianluca (CERN); KAPLON, Jan (CERN); POLTORAK, Karolina (AGH University of Science and Technology (PL)); PERKTOLD, Lukas (Graz University of Technology (AT)); MOREL, Michel (CERN); BONACINI, Sandro (CERN)

Presenter: NOY, Matthew (CERN)

Session Classification: III.a FE & ASICs

Track Classification: Data-processing: 3a) Front-end Electronics