MONOLITHIC PIXEL DETECTORS IN HEP EXPERIMENTS

P. Riedler, CERN

TIPP 2014 – "International Conference on Technology and Instrumentation in Particle Physics"
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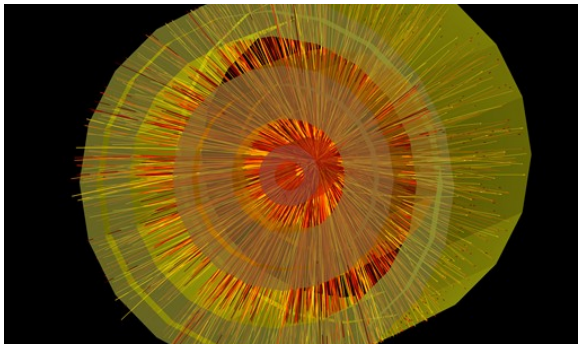
Outline

- Monolithic pixel detectors
- Present use in HEP
- Summary

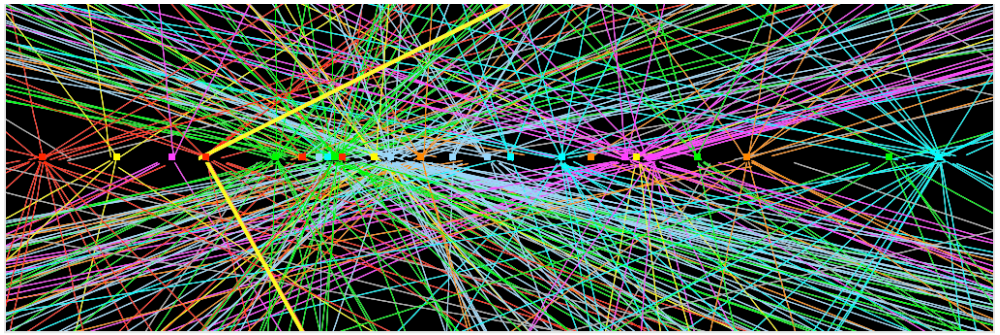
Disclaimer: *This talk presents a personal view on the various activities in the field of monolithic pixel detectors and is not intended as a complete list of all possible options nor applications.*

Pixel Detectors

Silicon pixel detectors are **high granularity tracking detectors**, which provide **unambiguous and precise hit information** in the **harsh environment** close to the interaction point.



Example: Pb-Pb event (ALICE, 2010)



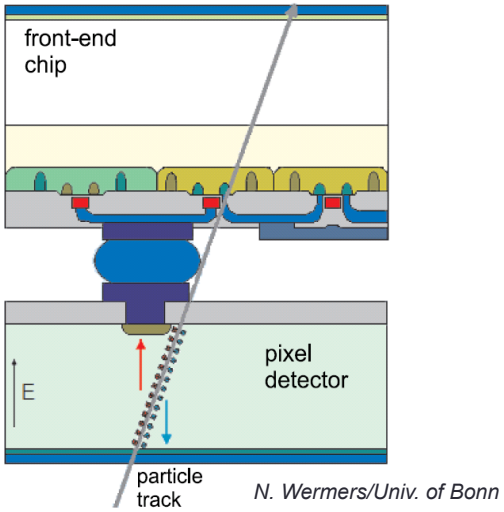
Example p-p collision~70 interactions/BX (ATLAS)

- Installed in LHC experiments ALICE, ATLAS and CMS.
- In the future all LHC experiments and several non-LHC experiments foresee upgrades using pixel detectors.
- All systems presently used at LHC are based on **hybrid pixel detectors**.

Monolithic Pixel Detectors - Definition

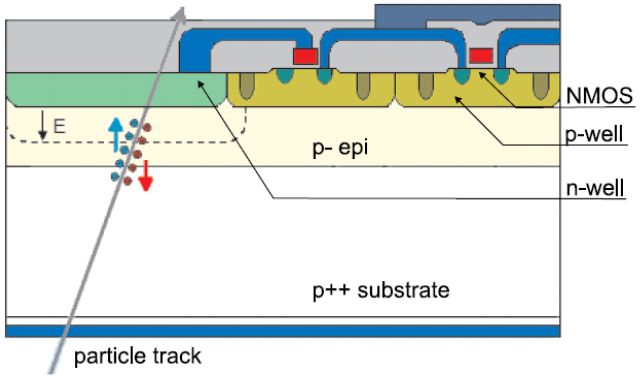
Compared to hybrid pixel detectors, the **sensitive volume and part or the full readout circuitry is combined in one piece of silicon**. The generated charge is collected on a dedicated collection electrode.

Hybrid Pixel Detector



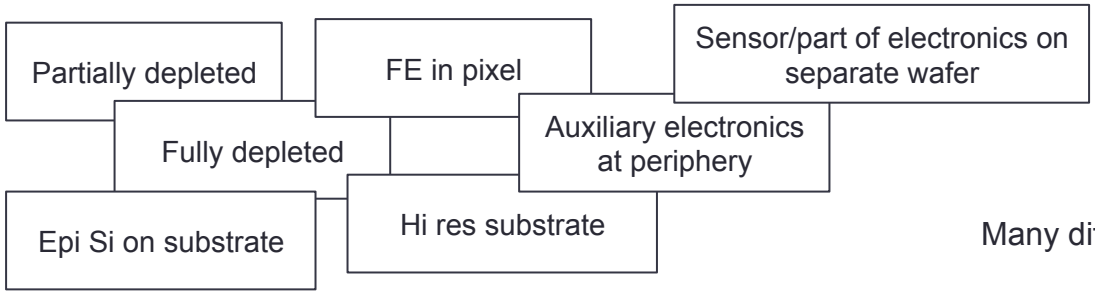
N. Wermers/Univ. of Bonn

Monolithic Pixel Detector (example)



Monolithic Pixel Detectors

Monolithic pixel detectors for HEP exist in many different flavours: CCD, Monolithic Active Pixel Detectors (MAPS), DEPFET, SOI Pixel Detectors, ….



Many different parameters…….

Common points:

- Profit from standard **industrial CMOS processing** (many foundries, larger wafer diameter, potentially low cost per area, stitching, ..)
- **Thin detectors** (O(50 µm Si)) → low material budget
- **High granularity** (small cell sizes)
- No need for cost intensive fine pitch bump bonding

Low Mass – Low Power

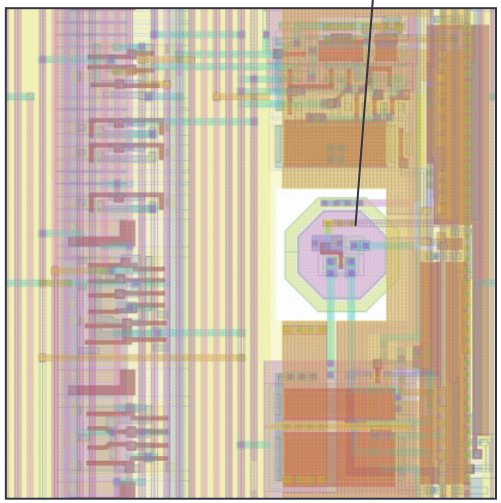
The **actual silicon thickness** is only part of the contribution and can be in the order of 50 µm (e.g. STAR HFT, ALICE ITS upgrade).

The **power consumption** will impact the overall material budget through cables and cooling → **optimize** analog, digital, data transmission power consumption

- Analog power: depends on collected charge over capacitance Q/C in the pixel → optimize sensing node

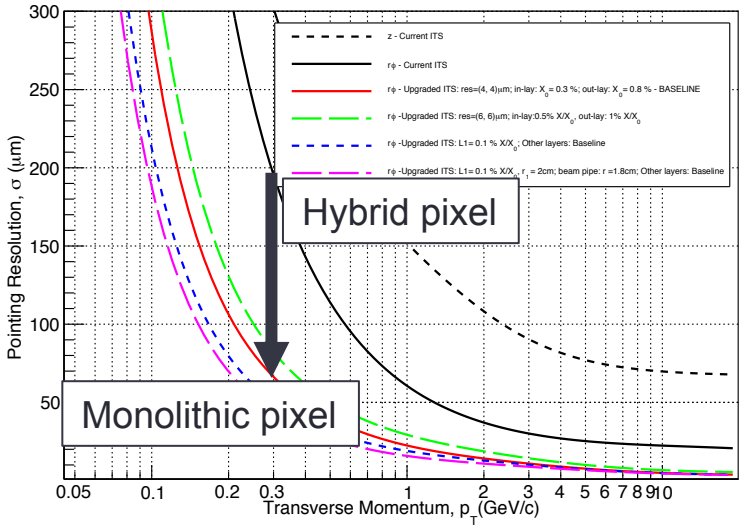
$$P \sim \left\{ \frac{S}{N} \frac{Q}{C} \right\}^{m} \quad with\ 2 \leq m \leq 4$$

Collection diode- ALICE ITS priority encoder
~ 2-3 µm ø, C~ O(few fF)
22 µm x 22 µm pixel



T Kugathasan, NSS 2013

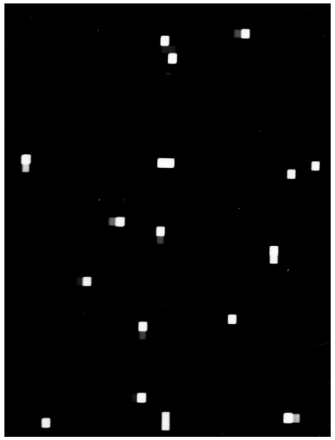
ALICE ITS Upgrade TDR, CERN-LHCC-2013-024



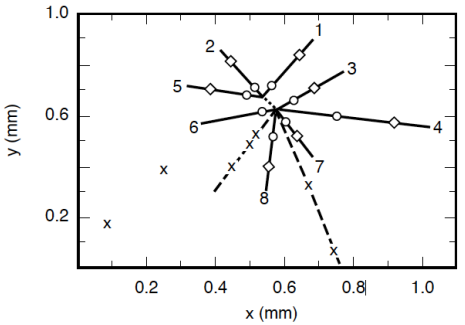
First Use in HEP Experiments - CCDs

Pixel-like silicon detectors based on CCDs in the early 1980s: SLD/SLAC, NA11/32 CERN

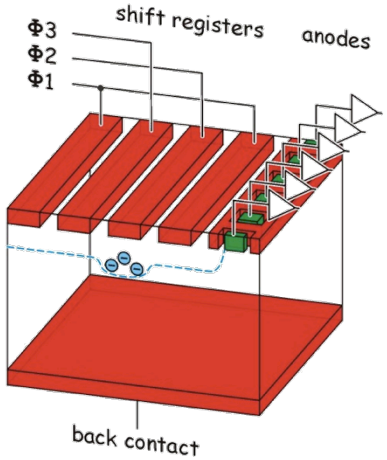
Charges are shifted through potential wells outside the active volume to the edge of the detector to the anodes.



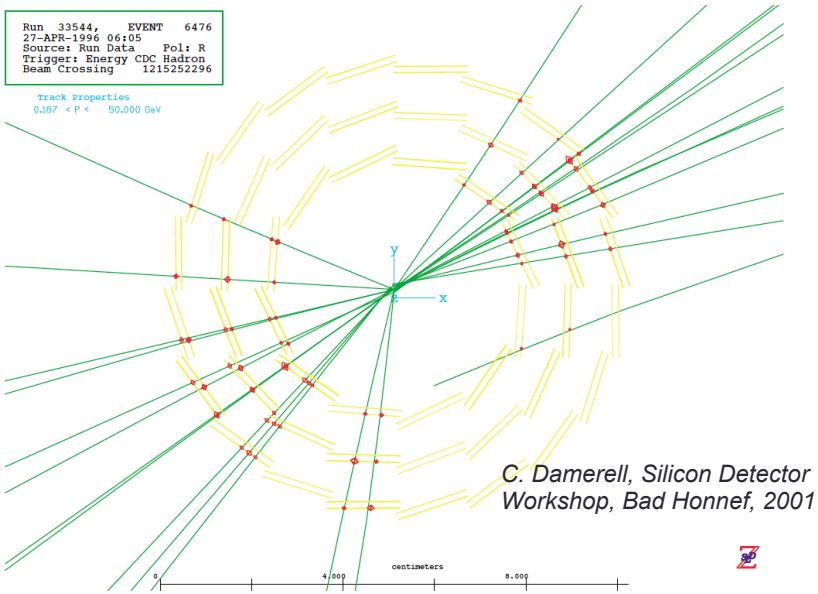
t6 – 1980



NA32 1985



Small pixel sizes (O(10 µm), slow matrix readout, low radiation tolerance

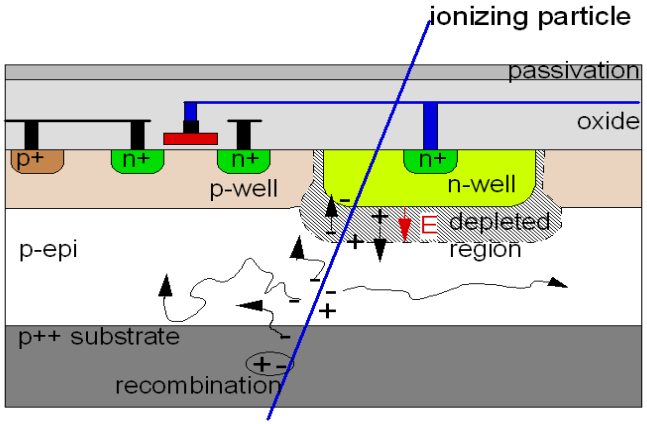


C. Damerell, Silicon Detector Workshop, Bad Honnef, 2001

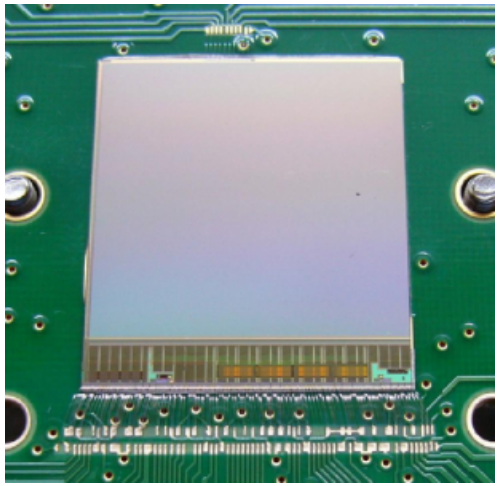
Traditional Monolithic Active Pixel Sensors - MAPS

In the late 1990s commercial **CMOS technologies with very few transistors per cell were proposed**

- Only one transistor type in the active area (NMOS).
- Often use rolling shutter architecture for reading out the matrix.
- No back-bias applied, charge mostly collected by diffusion → **more sensitive to displacement damage in the epi-layer.**



M. Winter

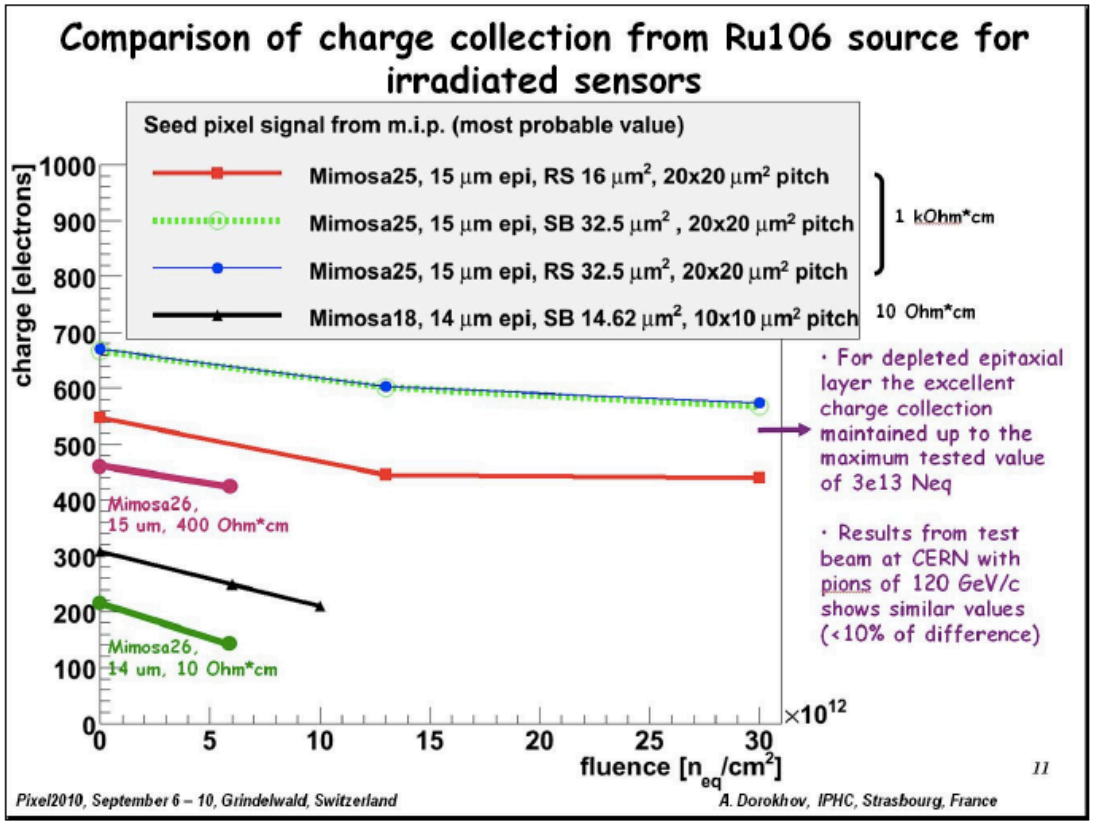


ULTIMATE chip for STAR HFT (IPHC Strasbourg)

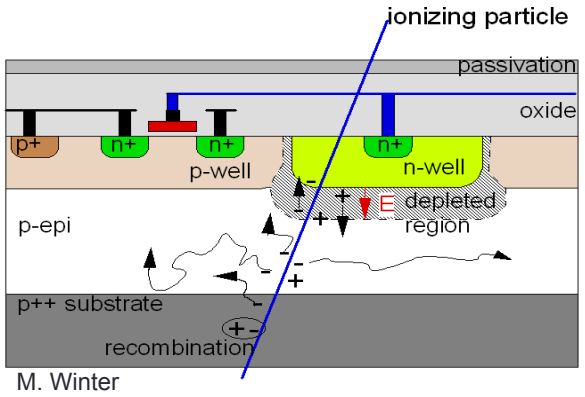
Radiation Tolerance

Transistor radiation tolerance improves with deeper sub micron processes and improved design layout.

Charge collection by diffusion suffers from radiation damage beyond 10^{13} n_{eq} cm^{-2}!



A. Dorokhov et al., Pixel 2010



M. Winter

Deplete part or all of the charge generation volume to **collect charge by drift**

Pixel Detectors in HEP – Inner Tracking Regions

	BX time [ns]	Particle Rate [kHz/mm^2]	Fluence [n_{eq}/cm^2 per lifetime]	Ion. Dose [Mrad per lifetime]
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2 x 10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2 x 10^{16}	>500
LHC HI (6 x 10^{27} cm^{-2}s^{-1})	20 000	10	10^{13}	0.7
RHIC (8 x 10^{27} cm^{-2}s^{-1})	110	3.8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

N. Wermes, CERN Seminar, 29/11/2013
Lifetime: LHC, HL-LHC: 7 years; ILC: 10 years; others: 5 years

Monolithic pixels:
- Lower rates
- Lower radiation
- Smaller pixels
- Less material

Examples: STAR HFT, BELLE II, ALICE Upgrade

Hybrid pixels:
- High rates
- High radiation

Examples: ATLAS, CMS, NA62

Monolithic Pixel Detectors in HEP – Perspectives

Monolithic pixel detectors are already now interesting options for low radiation and rate environments and have been adopted for the STAR HFT, BELLE II and the ALICE ITS upgrade.

The application in high radiation areas will require **radiation hard options** which can sustain the **high rates and provide adequate time resolution**.

Potentially, the **low cost manufacturing** of CMOS monolithic pixel detectors and the availability of large wafer diameters could have a significant cost impact also for larger trackers – if the **power density** can be brought to values compatible with strip detectors with a sufficiently fast readout.

LHC Tracker Upgrades	Area
ALICE ITS	12 m^2
ATLAS Pixel	8.2 m^2
ATLAS Strips	193 m^2
CMS Pixel	4.6 m^2
CMS Strips	218 m^2
LHCb VELO	0.15 m^2
LHCb UT	5 m^2

Different Monolithic Pixel Designs

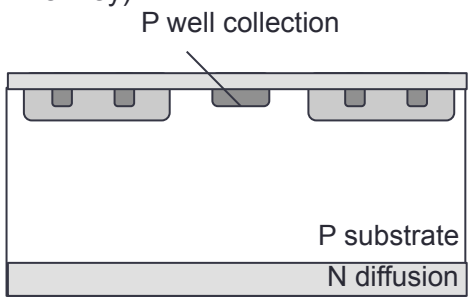
Ideally one would like to achieve:

- Low capacitance → low power
- Good S/N
- ~ns time resolution
- High rate capability (>10 MHz/mm^2)
- Full depletion → radiation tolerance
- Single sided processing → low cost mass production

No unique solution for all yet, but some aspects addressed.
Examples:

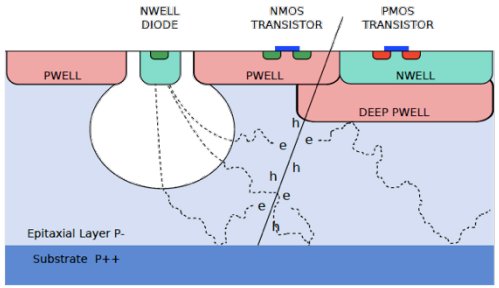
High resistivity substrate with back side processing and simple amplification stage in pixel, e.g:

- DEPFET (see next slides)
- Junction on the back (W. Snoeys, S. Parker, J. Plummer, C. Kenney)



High resistivity epi layer with full CMOS circuitry in pixel:

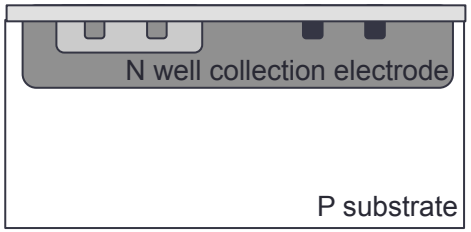
- ALICE ITS upgrade (see next slides)



Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)

All circuit inside deep n-well collection electrode, e.g:

- LePIX
- HV CMOS (see next slides)

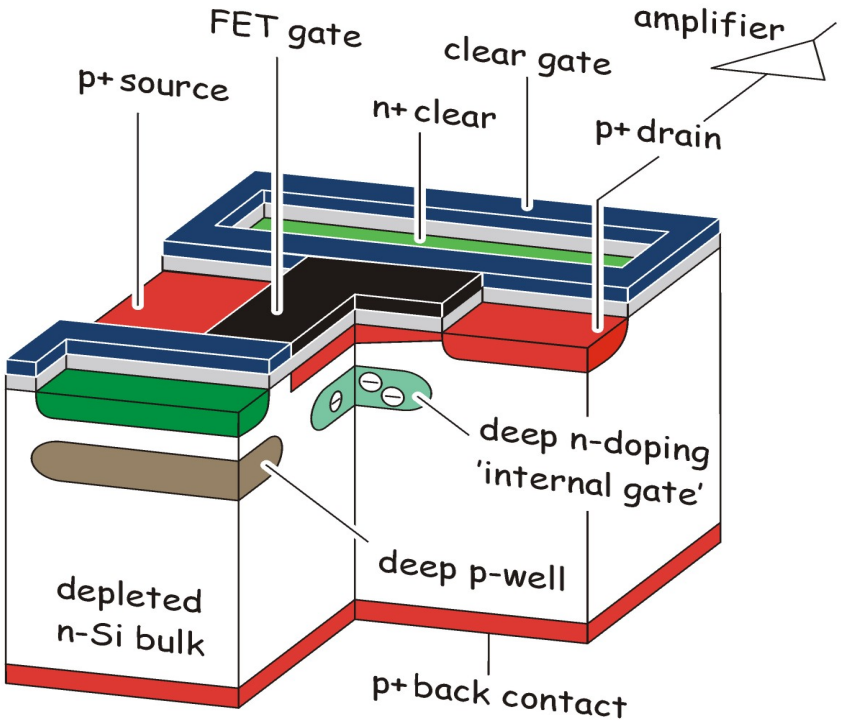


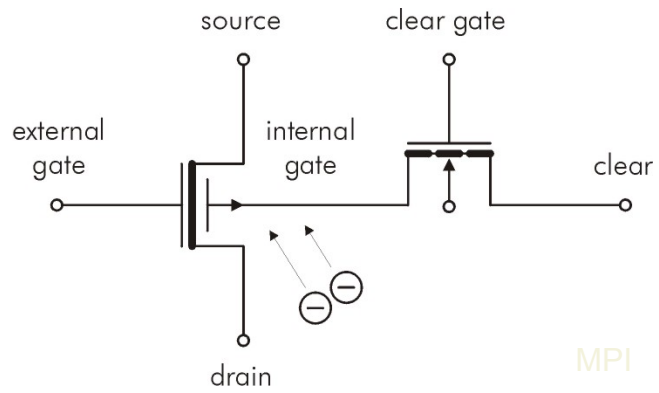
Example: DEPFET

Depleted p-channel FET on high resistivity substrate (Kemmer & Lutz, 1987)

- First stage amplification in pixel
- Fully depleted bulk
- Charge is stored underneath an internal gate causing a modulation in the transistor current
- Charge needs to be cleared after readout
- Requires off-chip read-out circuitry

Used in the BELLE II pixel detector upgrade



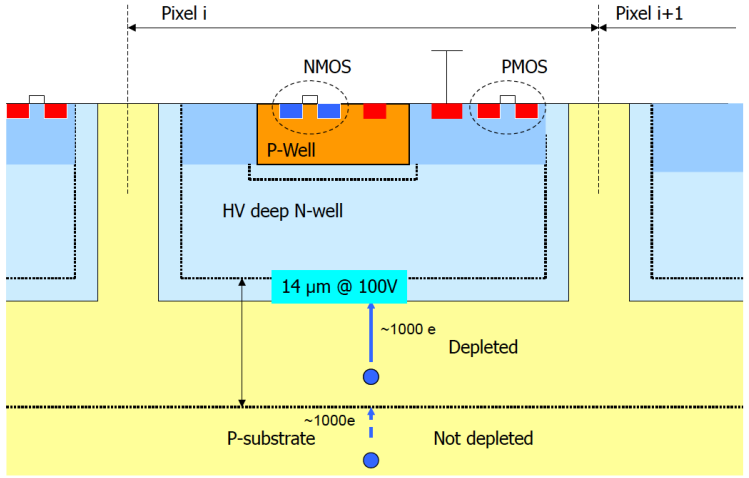


Presentation at TIPP: C. Marinas

Example: HV CMOS

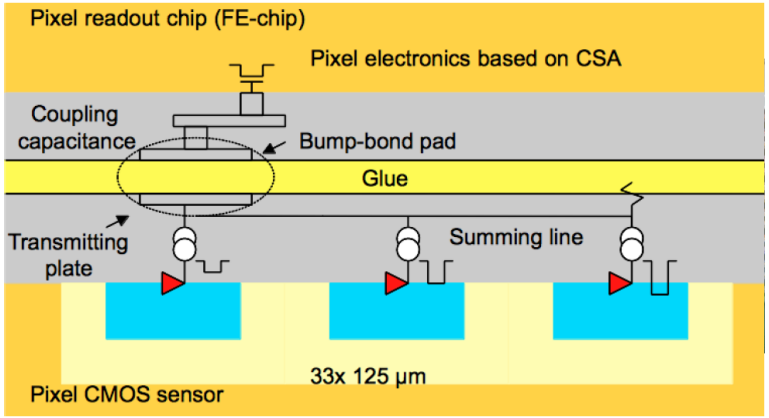
CMOS process with deep n-well collection electrode

- Structures realized in 0.18 and 0.35 µm CMOS
- Substrate resistivity ~ 10 Ohmcm
- **Biasing of the substrate up to ~100V →** homogeneous depletion layer (~ 14 µm deep)
- First stage amplification in pixel and additional electronics (e.g. discriminator etc.) possible
- Radiation tests with FEI4 glue bonded indicate radiation hardness up to 10^{16} $n_{eq}cm^{-2}$



CMOS electronics placed inside the diode (inside the n-well)

D. Münstermann, VERTEX 2013

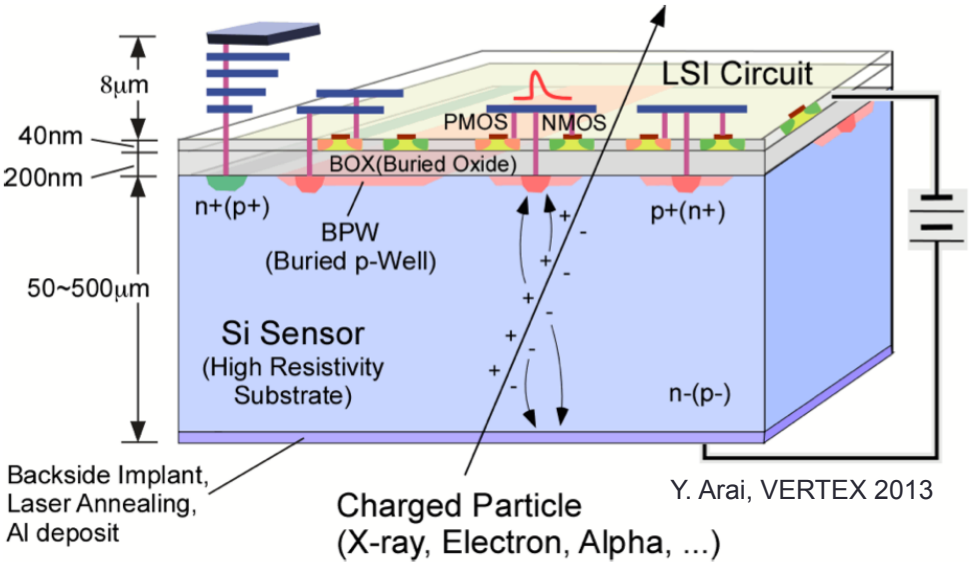


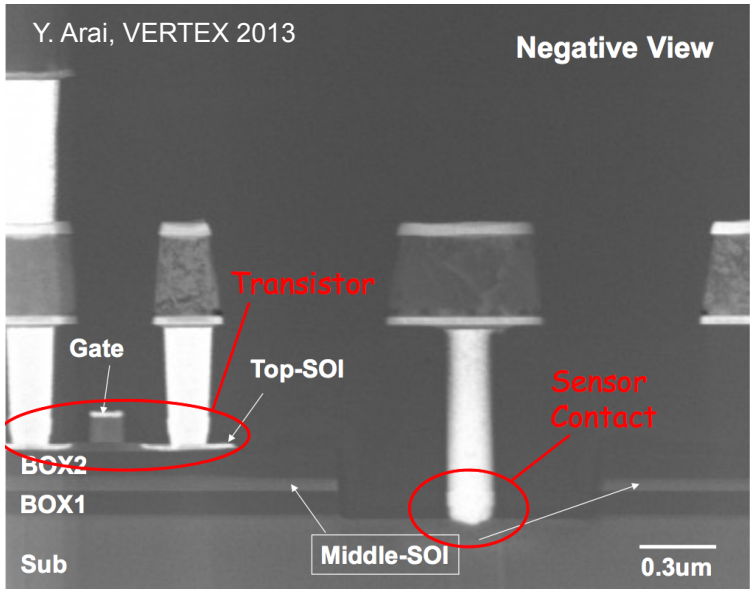
D. Münstermann, VERTEX 2013

Presentations at TIPP: S. Feigl, S. Shrestha

Example: SOI – Silicon On Insulator

- SOI wafer with high resistivity sensor part and thin CMOS chip connected via oxide
- Fully depleted thick sensing region with low C, offers good Q/C
- BOX causes reduced radiation tolerance, double BOX improves this, further development in progress.
- Is one of the ways to integrate large amount of in-pixel circuitry





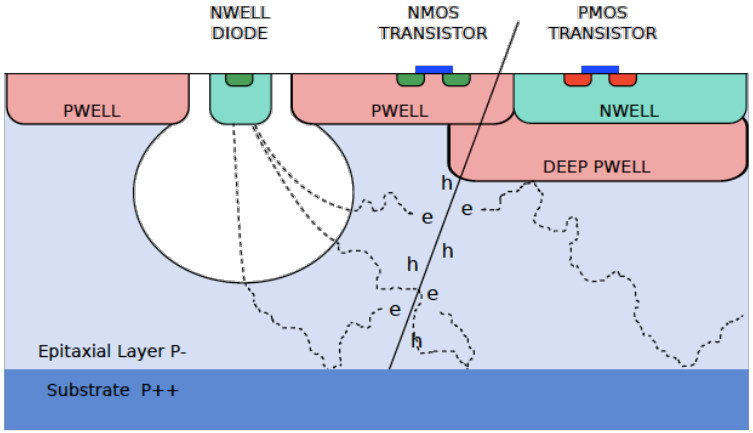
Presentations at TIPP: A. Takeda, H. Matsumura,T. Miyoshi, S. Honda

Example: High res epi layer MAPS

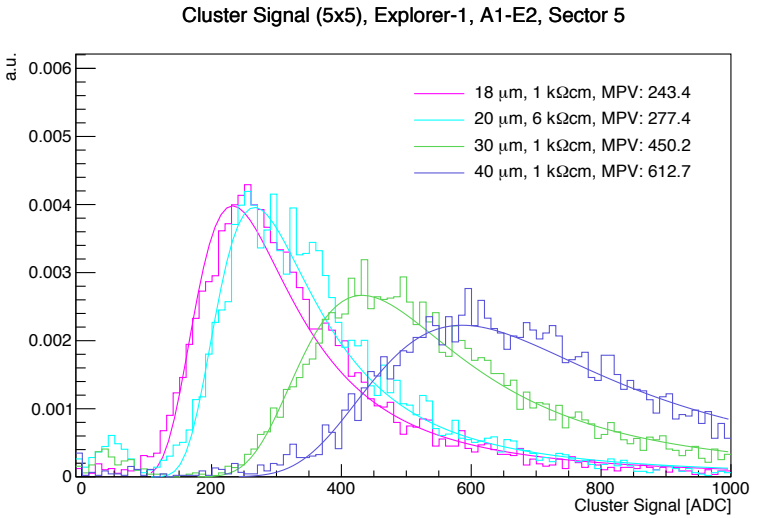
N-well collection electrode in high resistivity epitaxial layer (>1kohmcm)

- Full CMOS circuitry possible inside the pixel cell (deep p-well)
- Small n-well diode (2-3 µm diameter), ~ 100 times smaller than pixel → low capacitance
- Epi thicknesses 20-40 µm tested → higher cluster signal
- Partial depletion of the epi layer (limited by circuitry)

Will be used in the ALICE ITS Upgrade



Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)



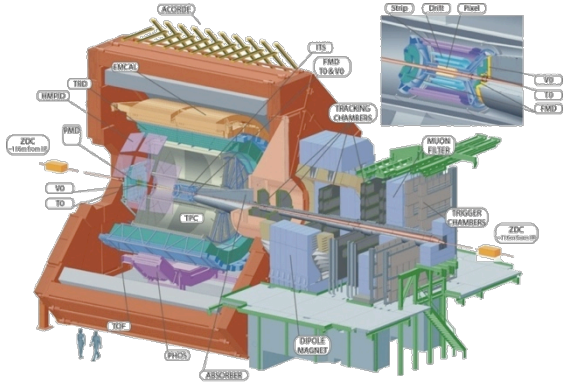
J. Van Hoorne, TIPP2014

Presentations at TIPP: J. Van Hoorne, T. Wang, F. Wilson
Poster: A. Collu

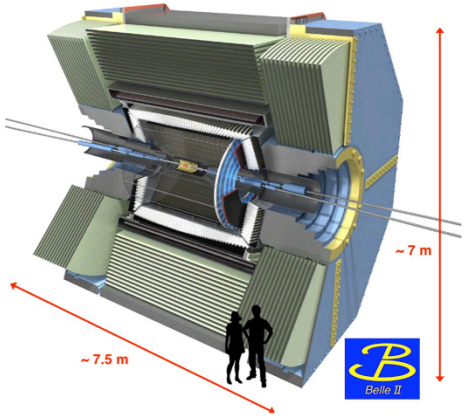
Monolithic Pixel Detectors in HEP Experiments

Thanks to the progress made several experiments have selected monolithic pixel detectors for their tracker upgrades:

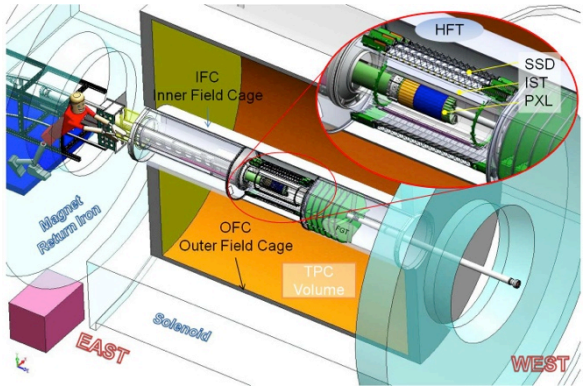
ALICE



BELLE II



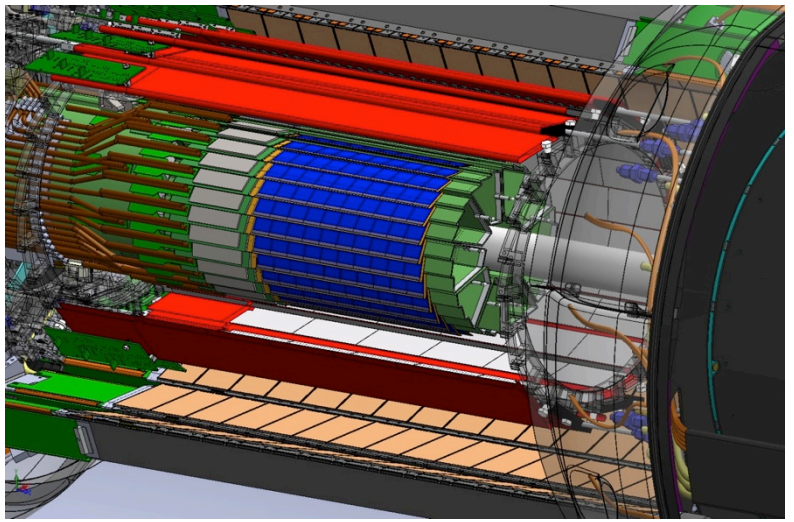
STAR



STAR Heavy Flavour Tracker (HFT) at RHIC

Monolithic Active Pixel Sensors – **MAPS**

- **2 barrel layers**
- **ULTIMATE chip** developed by IPHC Strasbourg (2 cm x 2 cm)
- 0.35 µm CMOS process
- Pixel size 20.7 µm x 20.7 µm (hit res. 6 µm)
- Rolling shutter readout with discriminators at the end of column
- Integration time 185.6 µs, in-pixel CDS
- Power dissipation ~170 mW/cm² @ 3.3V
- Chips thinned to 50 µm



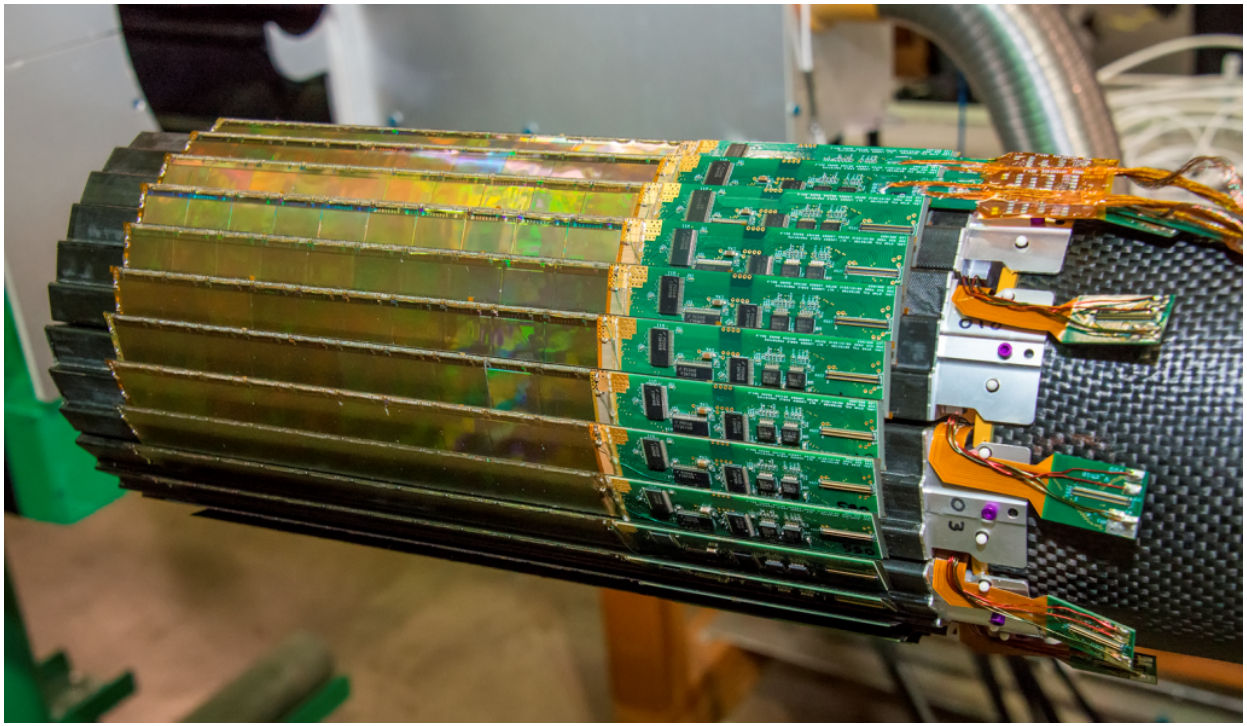
L. Greiner, FEE 2014

Radiation environment:
20 to 90 krad / year
$2*10^{11}$ to 10^{12} 1MeV n_{eq}/cm^2

Material budget:
0.37 % X_0 per layer

356 M pixels
~0.16 m^2

STAR Heavy Flavour Tracker (HFT) at RHIC



L. Greiner, FEE 2014

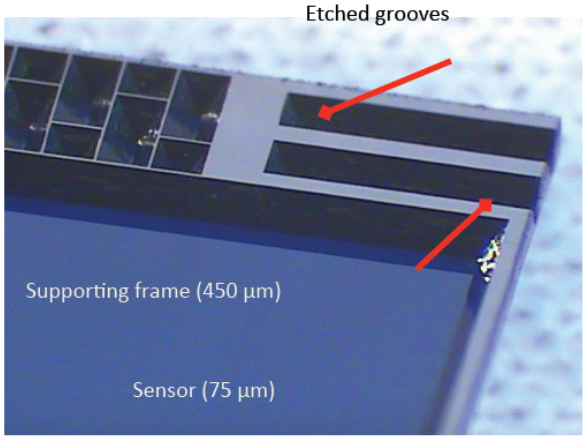
- **Detector installed end 2013, started data taking in Au-Au run 2014**
- Spare detector will be ready in about one month – will be used in the next run (1 day installation time)
- First operation experience shows resolution performance as expected

Belle II Pixel Detector at SuperKEKB

Pixel detector based on **DEPFET** sensors to be installed in 2015 (physics in 2016)

- 2 barrel layers (r=1.4 cm and 2.2 cm)
- Pixel size 50 µm x 75 µm
- Row-wise read-out (rolling shutter), 20 µs/frame
- Special thinning of the matrix area to reduce material budget (75 µm thick)

S. Tanaka, HSTD9, 2013



C. Lacasta, VERTEX 2013

Radiation environment:
~ 1.9 Mrad / year
~ 1.2 10^{13} 1MeV n_{eq}/cm^2 per year

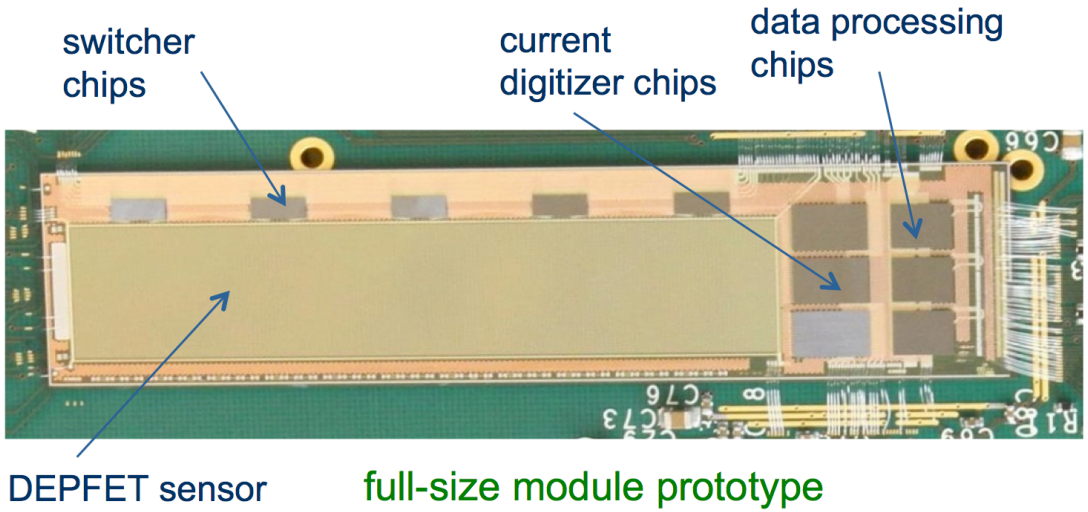
Material budget:
0.21 % X_0 per layer

Presentation at TIPP: K.Kishishita

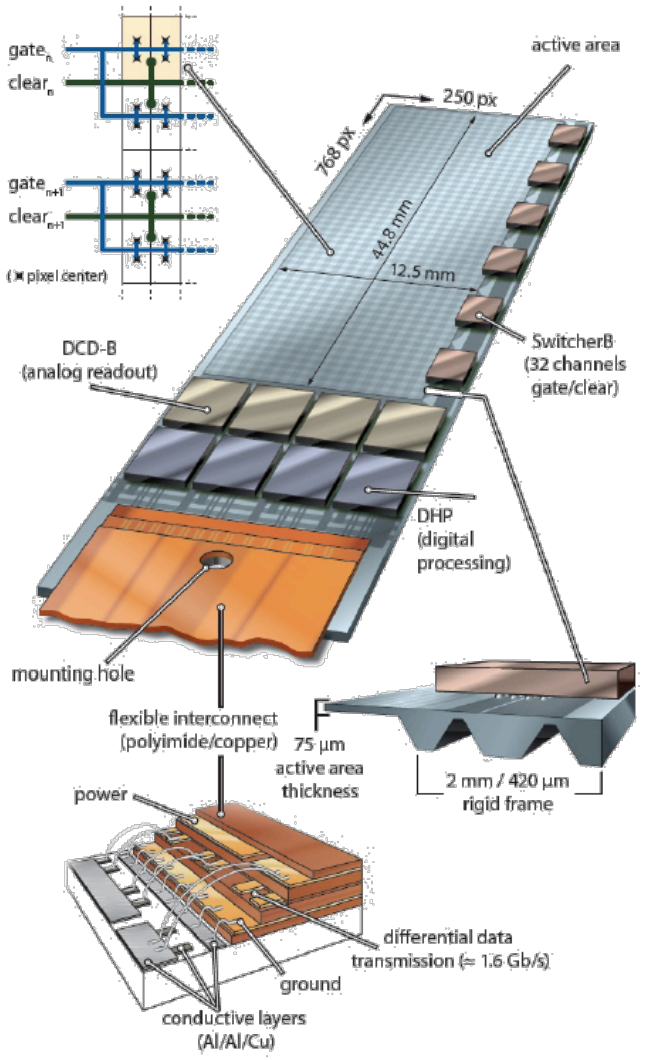
Belle II Pixel Detector at SuperKEKB

Ladder contains 2 half-modules with DEPFET sensor and auxiliary ASICS:

- First stage amplification in the pixel cell
- Three auxiliary ASICS bump bonded to the DEPFET sensor frame:
  - SWITCHER: row selection and clear
  - DCD-B: amplification and digitisation
  - DHP: pedestal subtraction and zero suppression, timing and trigger control



full-size module prototype



N. Wermes, CERN Seminar, 29/11/2013

ALICE Inner Tracking System Upgrade at LHC

Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

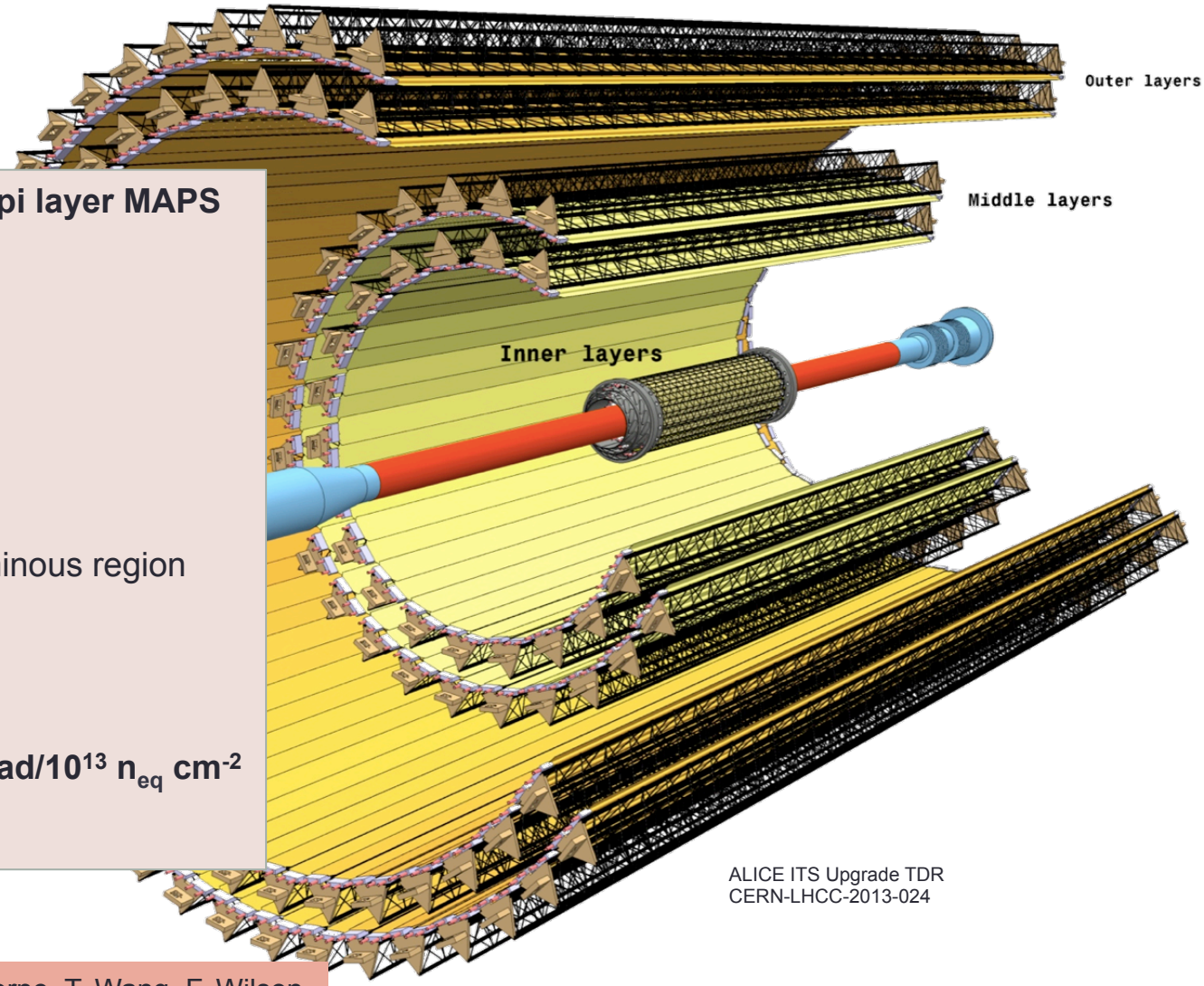
~ 10 m^2

$|\eta|<1.22$ over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

Radiation level (L0): 700 krad/10^{13} n_{eq} cm^{-2}

Installation during LS2



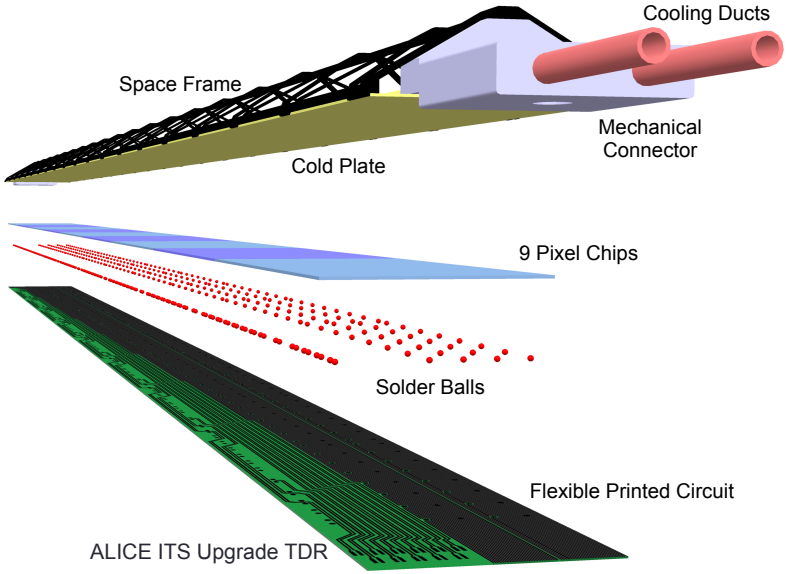
ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

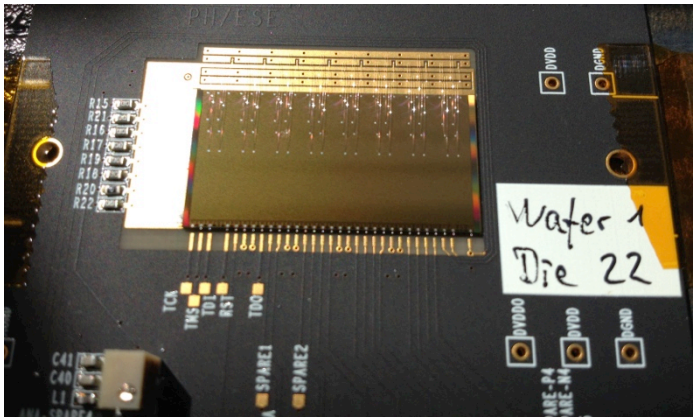
Presentations at TIPP: J. Van Hoorne, T. Wang, F. Wilson
Poster: A. Collu

ALICE Inner Tracking System Upgrade at LHC

Based on **CMOS MAPS on high resistivity epi layer with deep PWELL:**

- 0.18 µm CMOS process with full CMOS in the pixel
- Chips: 15 mm x 30 mm, thinned to 50 µm
- Pixel size 20 µm x 20 µm
- Integration time < 30 µs
- Power: < 300 (100) mW/cm^2 for the inner (outer) barrel
- Several readout architectures under study:
  - Classical rolling shutter (MISTRAL)
  - Rolling shutter with in pixel discrimination (ASTRAL)
  - Parallel rolling shutter (CHERWELL)
  - Self-triggered with in pixel discriminator and comparator (ALPIDE)
- **Full size (15 mm x 30 mm) prototype chips currently under study**





pALPIDEfs chip: 15 mm x 30 mm
M. Mager

Summary

- Monolithic pixel detectors are being studied intensively for their use in HEP experiments. They provide potentially low cost high precision tracking sensors with simplified interconnections compared to hybrid pixel detectors.

- Many different versions are under study, tackling the issues to make such detectors suitable for high radiation and high rate environments.

- Several experiments (ALICE, BELLE II, STAR) have chosen monolithic pixels for their upgrade.

- There is a number of presentations on the development of monolithic pixel detectors at this conference indicating the high interest in this field.