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3D integration of imagers

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A classical imager contains a 2D array of pixels responsible for the capture of the optical signal, surrounded by peripheral electronics which is reading out all pixels and sending the obtained image off-chip. For almost all application a trend towards high image resolution (and therefore smaller pixels) is observed. However, this leads to several performance issues. First, the area per pixel is reduced, while the required functionality per pixel is often increasing. Moreover, many more pixels need to be read out over a fairly long distance (i.e. the physical imager size), typically at a high speed. Some applications (such as X-ray imaging for medical applications) require very large area detection with minimal information loss.

Many of the above challenges can be solved by using vertically stacking dies using 3D integration technologies such as high density bumps or wafer-to-wafer interconnects, flip-chip or wafer-to-wafer bonding, through Si vias, wafer thinning etc. At the same time the concept of vertically stacking and interconnecting dies offers both optical performance benefits (i.e. when using backside illumination) as well as readout design opportunities, both in terms of available area per pixel, as in terms of architectural freedom (i.e. to distribute different functional blocks on different levels).

The advantages and challenges of the required processing technologies as well as different 3D stacked imager concepts will be discussed.

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