The QIE10/11

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About This Presentation

Simple English Summary:

The QIE is an electronic **chip that takes a current signal and integrates it** over 25 nanosecond periods. **The CMS hadron calorimeter (HCAL) uses these chips to measure energy.** This presentation is about the testing and verification of the QIE, which takes place at Fermilab.

Presentation Outline:

(0) Context

(1) The QIE10/11

(2) Single-Chip Tests

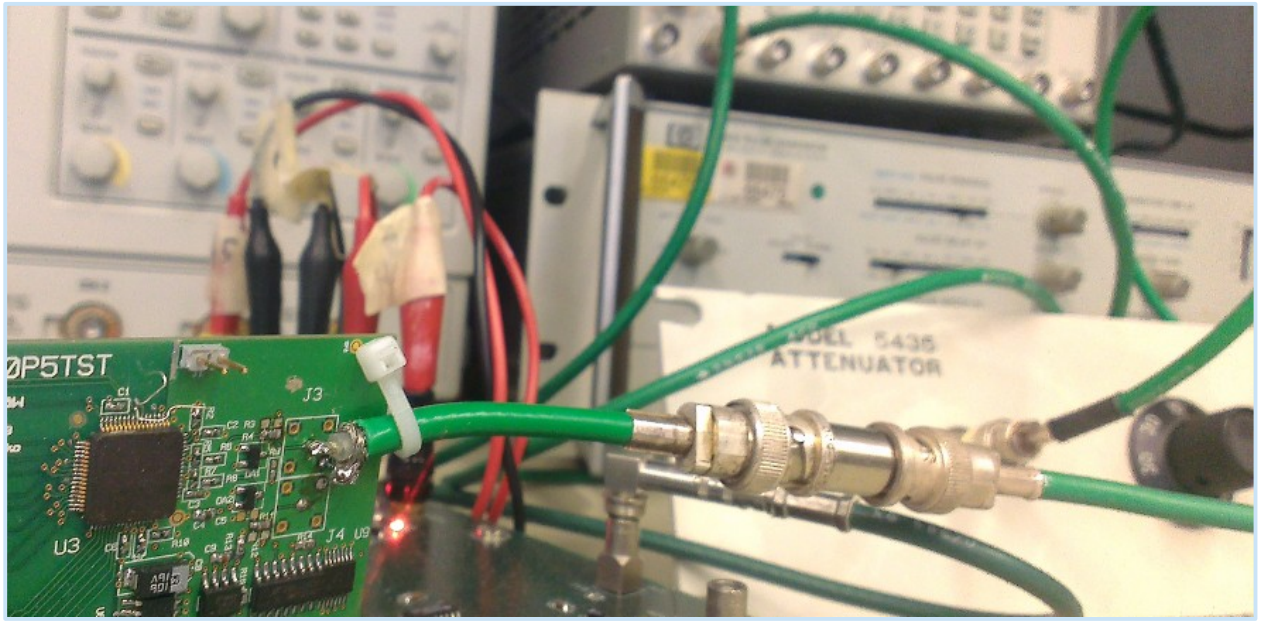
(3) ADC Response

(4) TDC Response

(5) Other Tests

(6) Radiation Tolerance

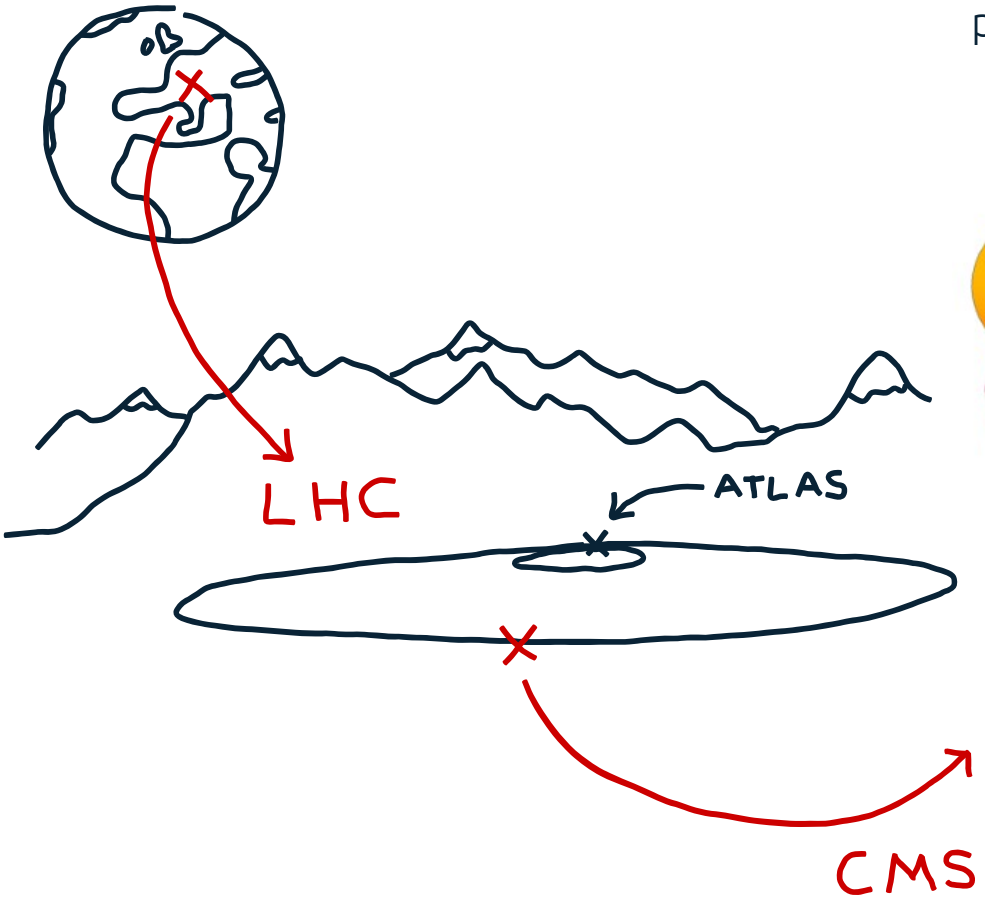
(7) Conclusion



Teststand at Fermilab

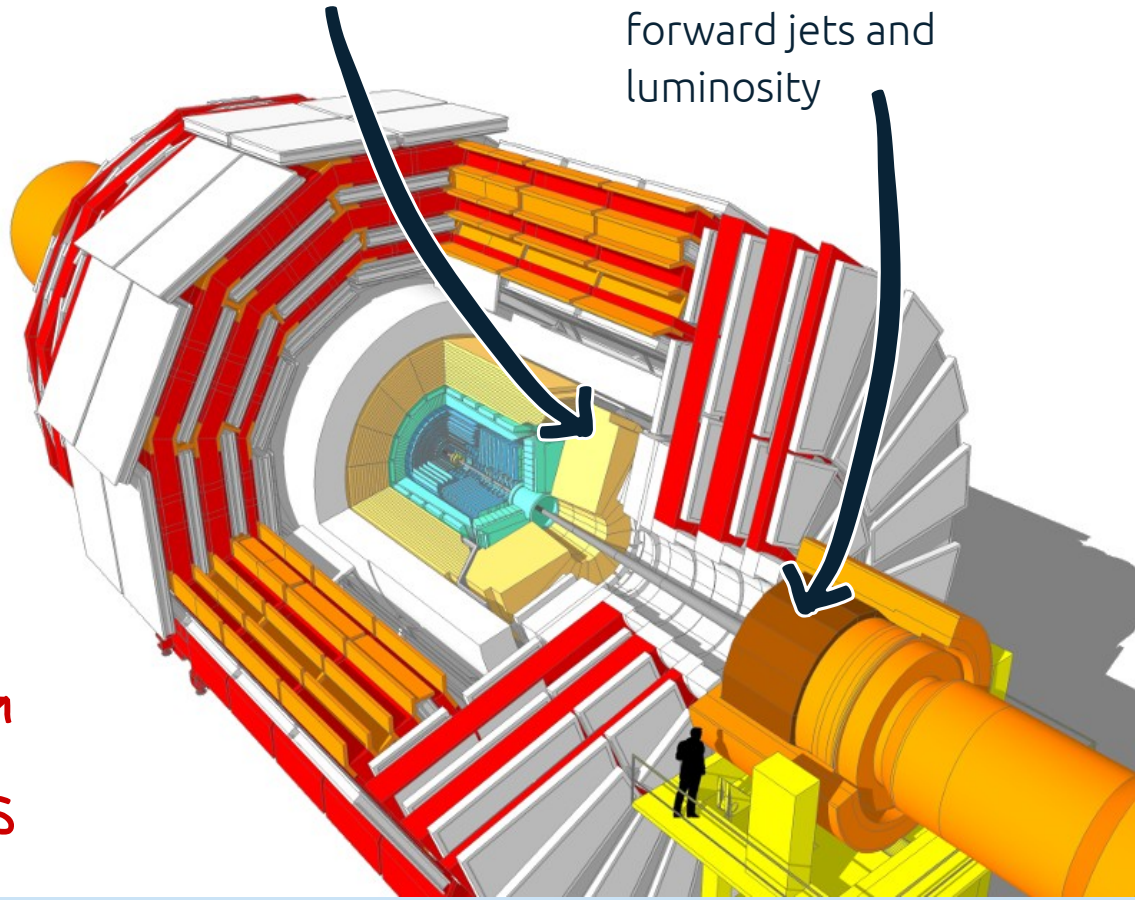
(0) The CMS Detector

Before I talk about the chip, let me motivate it by putting it in the context of **the compact muon solenoid (CMS) detector**:



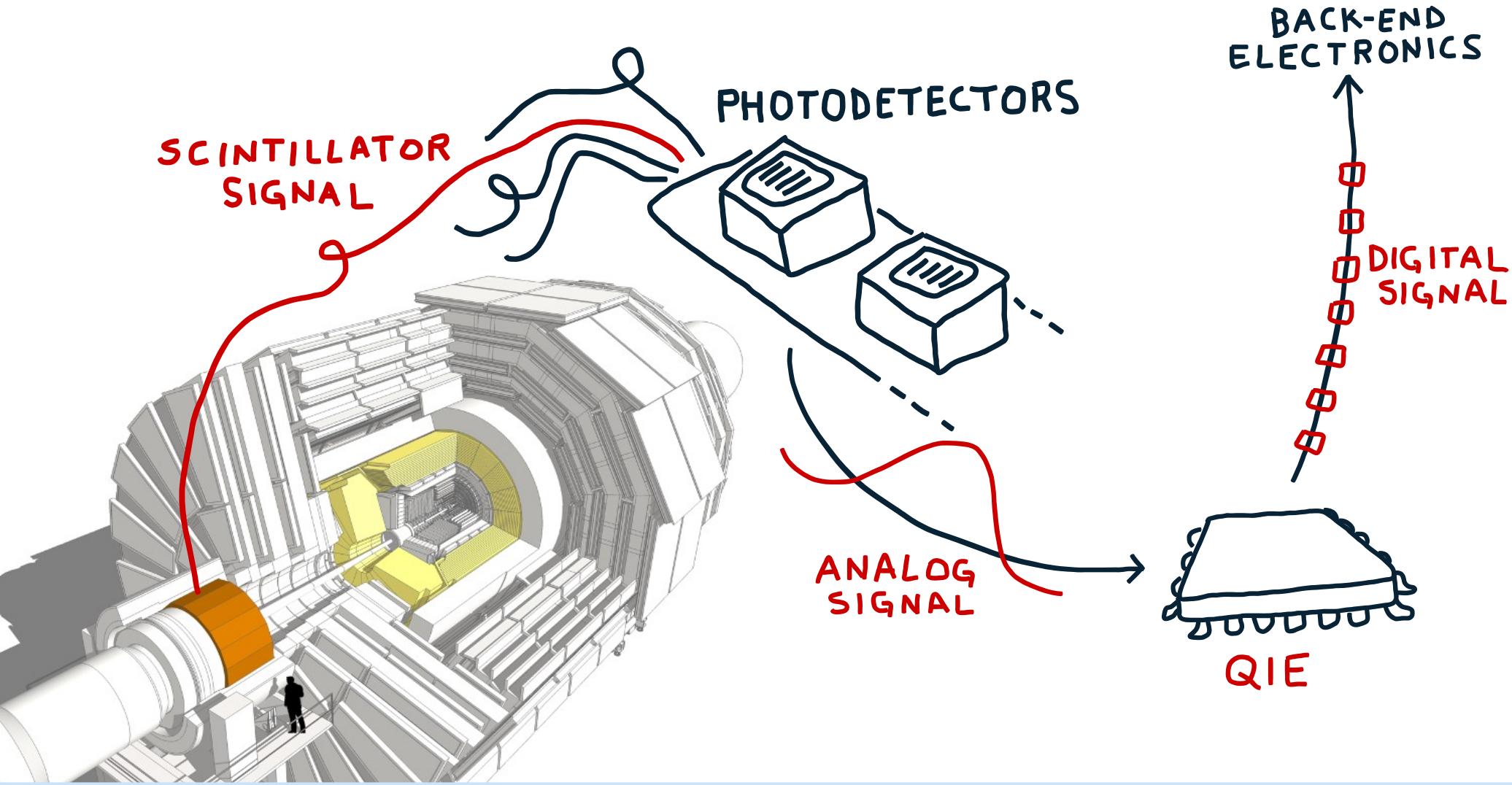
Hadron Calorimeter Barrel (HB) And Endcaps (HE):
Measures the energy of hadrons and, indirectly, the energy of non-interacting particles such as neutrinos

Forward Hadron Calorimeter (HF):
Important for measuring forward jets and luminosity



(0) The QIE

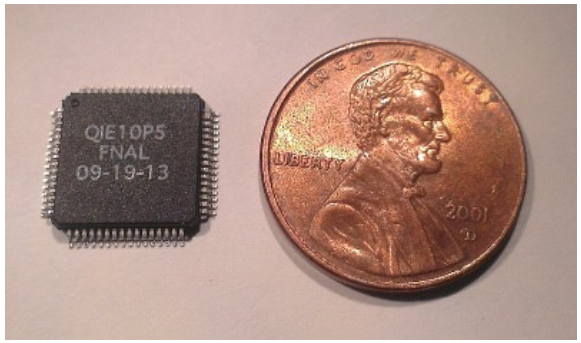
The **QIE chip is the analog-to-digital (ADC)** application-specific integrated circuit (ASIC) that digitizes data from the hadron calorimeter (HCAL) photodetectors:



(1) QIE Overview

QIEx:

(Q) Charge
(I) Integrator
and
(E) Encoder
(x) version #



The diameter of a US penny is 3/4 in, or ~ 2 cm

History:

- **1989:** Invented by Bill Foster for the Solenoid Detector Collaboration (SDC) at the Superconducting Super Collider (SSC)
- **1995 (QIE5):** First functioning prototype designed by Thomas Zimmerman for the Kaons At The Tevatron (KTeV) experiment at Fermilab
- **1996 (QIE6):** Used in the calorimetry of the Collider Detector At Fermilab (CDF)
- **2002 (QIE7):** Used in the front-end of the Main Injector Neutrino Oscillation Search (MINOS) Near Detector at Fermilab
- **2003 (QIE8):** Used in the front-end of the CMS HCAL at CERN
- **2014 (QIE10/11):** New versions designed for the CMS HCAL Phase 1 Upgrade

(1) QIE10/11 Design

The QIE10 and the QIE11 are identical in design, except the QIE11 includes a programmable current shunt:

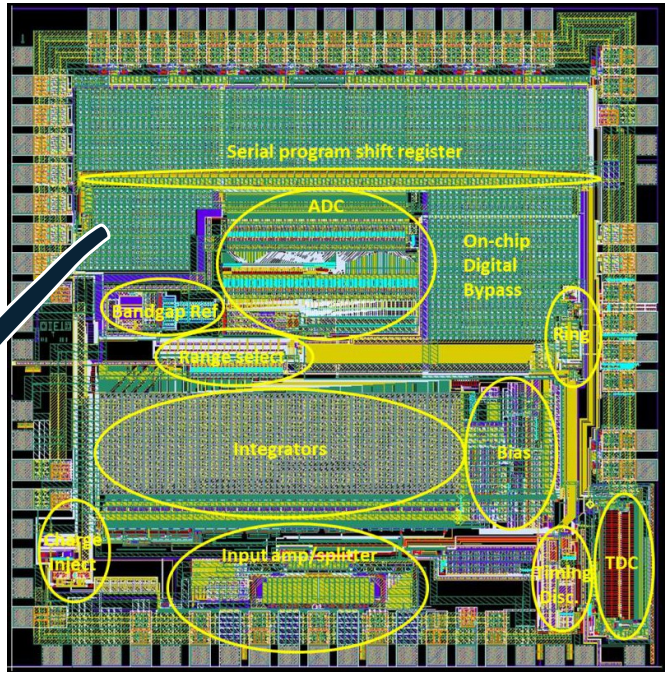
Features:

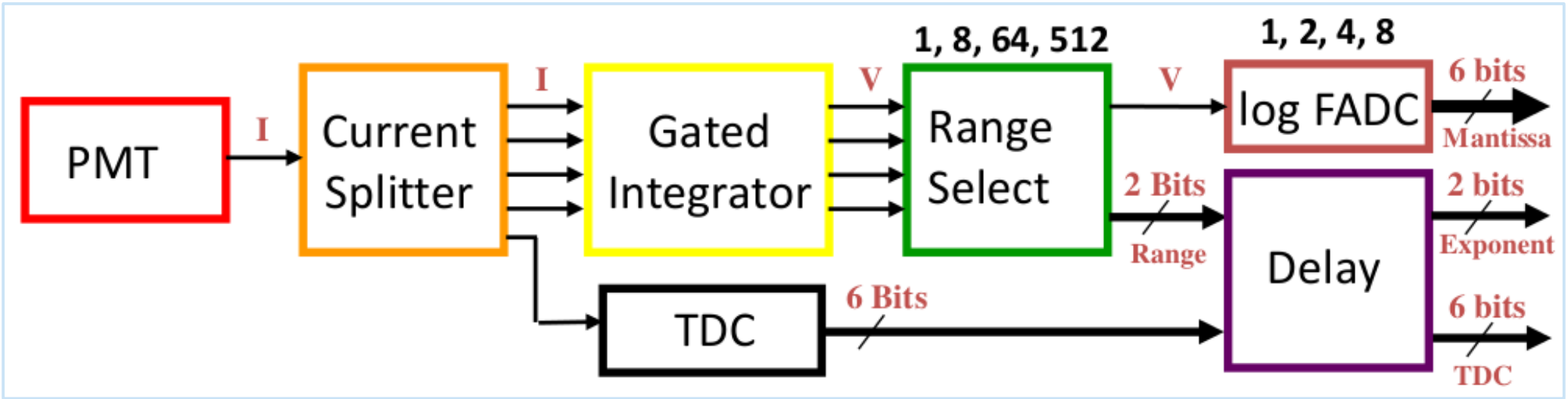
- **Deadtimeless operation at 40 MHz (25 ns):** Achieved by four-phase operation (see next slide)
- **Large dynamic range:** About 400 fC at about 3 fC resolution, this is 10 times wider than the previous version.
- **Timing information (TDC):** The position in time of the first rising edge is measured with 500 ps resolution.
- **Programmable:** Pedestal, timing threshold, and operation mode settings are all configurable.
- **Internal calibration:** An eight-valued charge injector inside the chip can be used for rudimentary calibration.
- **Low power draw:** The chip draws about 310 mW.
- **350 nm AMS SiGe fabrication process**: This is the first QIE version designed with this process.
- **Programmable gain (QIE11):** The QIE11 features a programmable gain by providing a configurable series of current shunts at the input.

(1) QIE10/11 Design

Deadtimelessness is achieved by four operational phases:

- Integrate, range select, digitize, reset integrator
- Each phase takes 25 ns, so four pipelines are run in parallel.
- Each pipeline is identified by a capacitor ID (CapID).





(2) Single-Chip Tests

We have **310 packaged QIE10 chips and 20 QIE11 chips** that we study.

- With this amount of chips we're able to get a hint of large batch performance and yields.
- Tests are performed at Fermi National Accelerator Laboratory (**Fermilab**) in Illinois, USA.

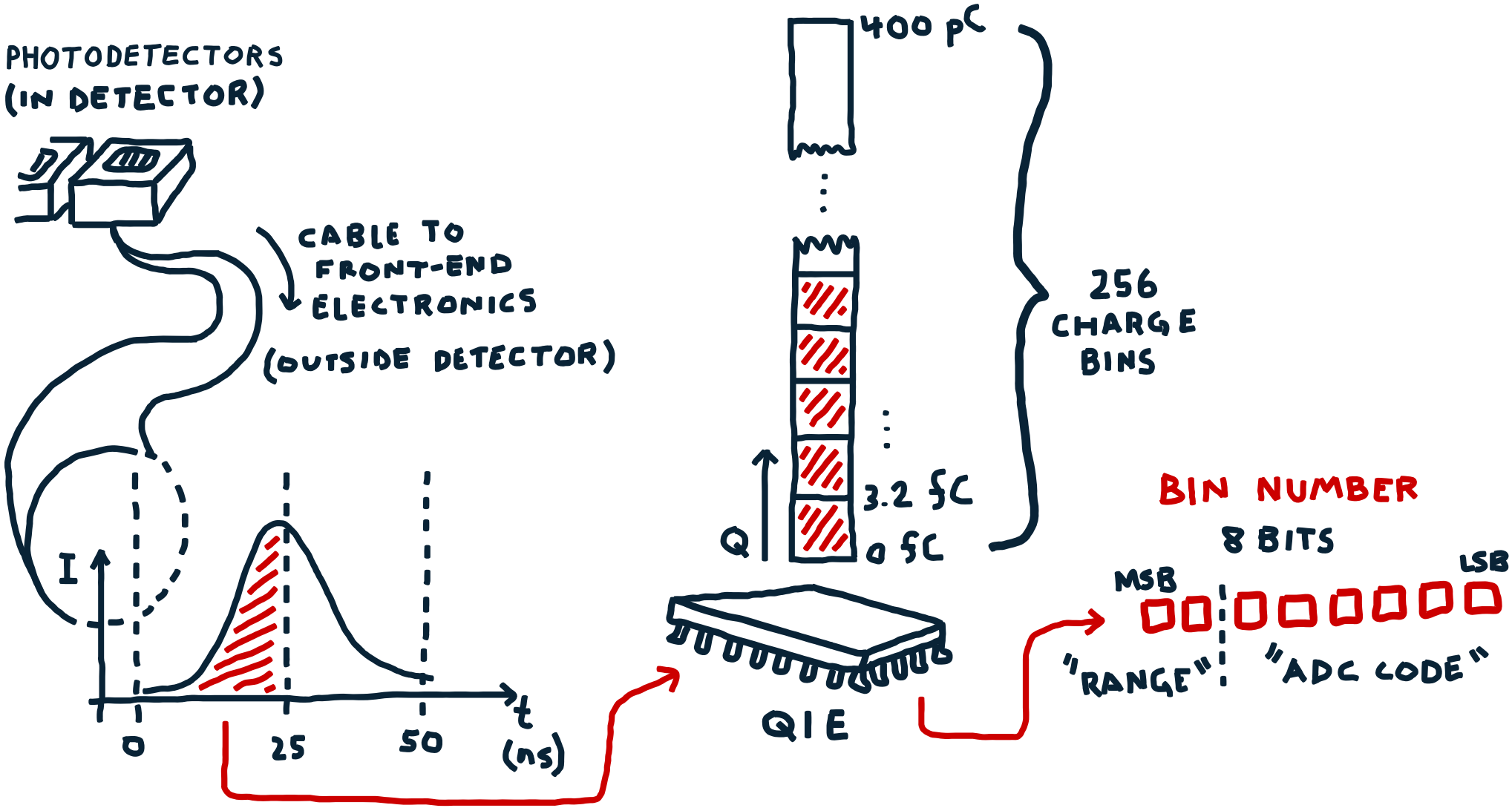
- **"Chips"**: number of chips used in specific test
- **"Success"**: number (percentage) of chips that passed the test's specifications for acceptable performance

Test	Chips	Success
Operable	310	299/310 (96 %)
Dynamic Range: (A) ranges present	20	20/20 (100 %)
Dynamic Range: (B) charge	20	20/20 (100 %)
Range Overlap	299	296/299 (99 %)
Pedestals: (A) untuned	100	98/100 (98 %)
Pedestals: (B) untuned spread	100	99/100 (99 %)
Pedestals: (C) tuned	100	100/100 (100 %)
Pedestals: (D) tuned spread	100	100/100 (100 %)
Pedestals: (E) pedestal DAC	100	99/100 (99 %)
ADC: (A) nominal bin widths	20	20/20 (100 %)
ADC: (B) DNL	20	20/20 (100 %)
ADC: (C) coarse bin widths	299	288/299 (96 %)
TDC: (A) detailed	1	1/1 (100 %)
TDC: (B) coarse	20	20/20 (100 %)
TDC: (C) special codes	299	299/299 (100 %)
Pulse Integration	1	1/1 (100 %)
Stability	1	1/1 (100 %)
QIE11 Shunts	1	1/1 (100 %)
Total Yield	**310**	**281/310 (91 %)**

Summary of single-chip tests

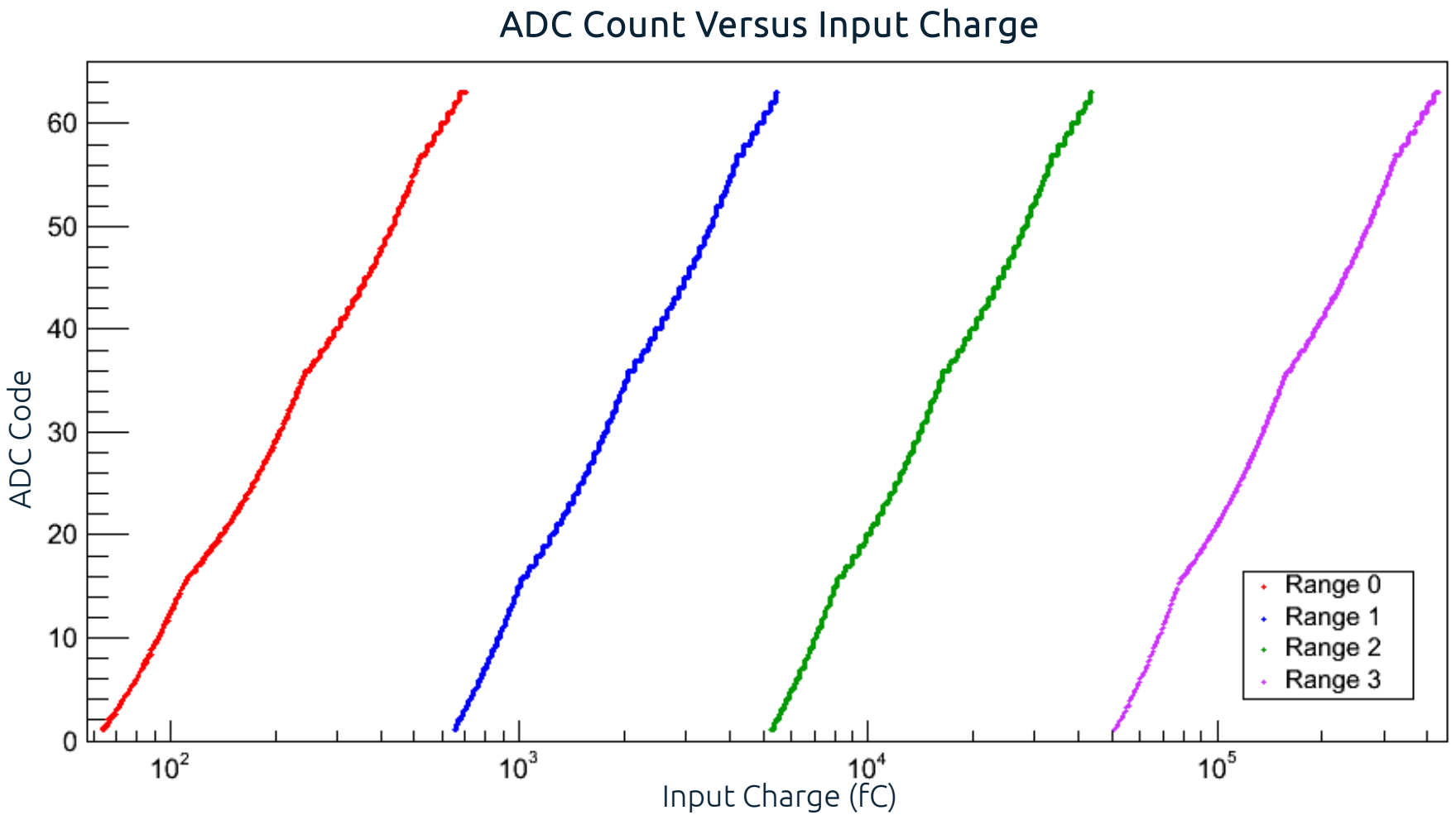
(3) ADC Response

The following sketch illustrates how the ADC functionality works:



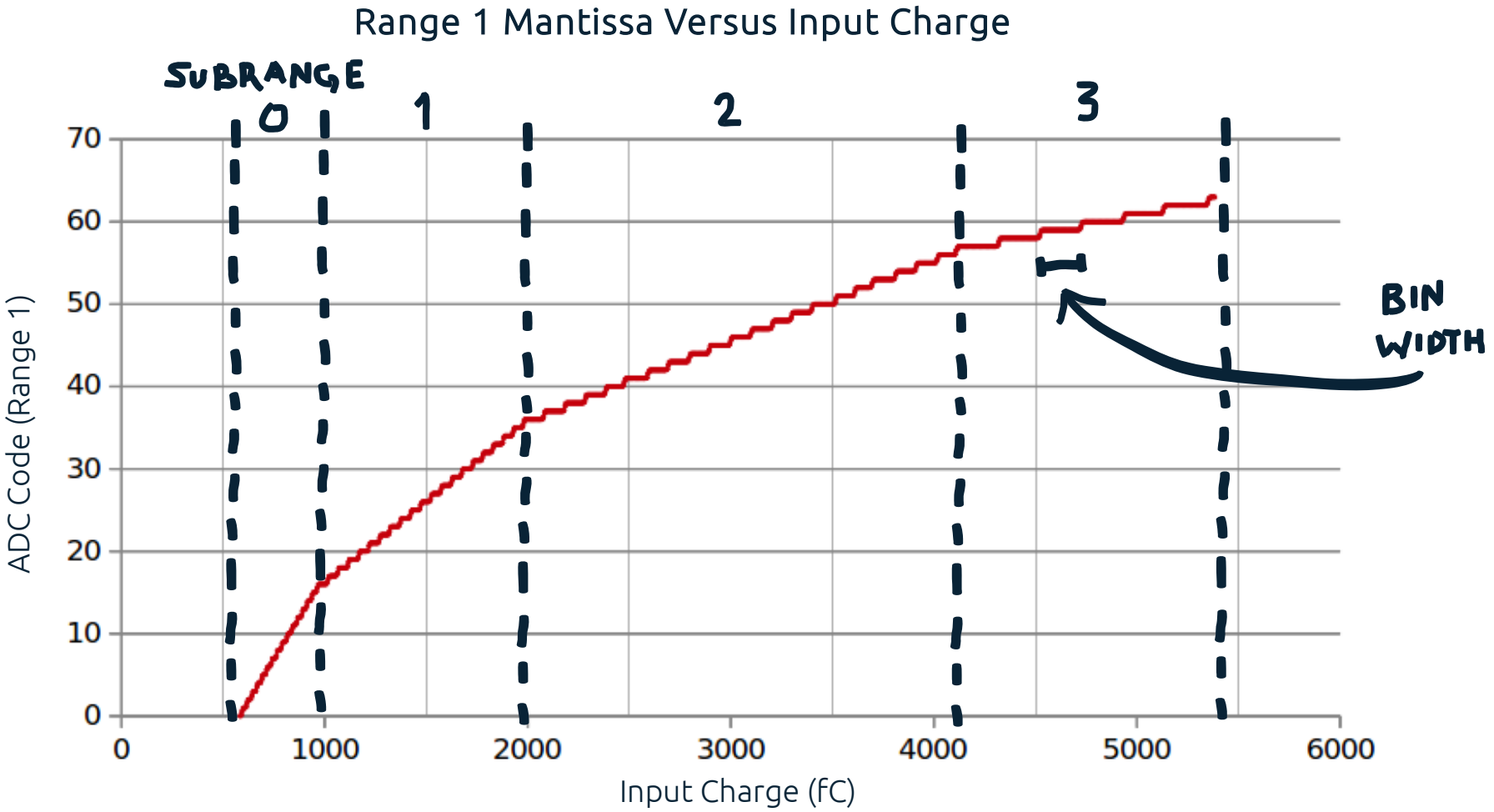
(3) ADC: Dynamic Range

The dynamic range of the QIE10 is roughly 400 pC. This is a plot showing the entire dynamic range of a chip:



(3) ADC: Subranges

Each of the 4 ranges are divided into 4 subranges. Each subrange has a different characteristic bin width:



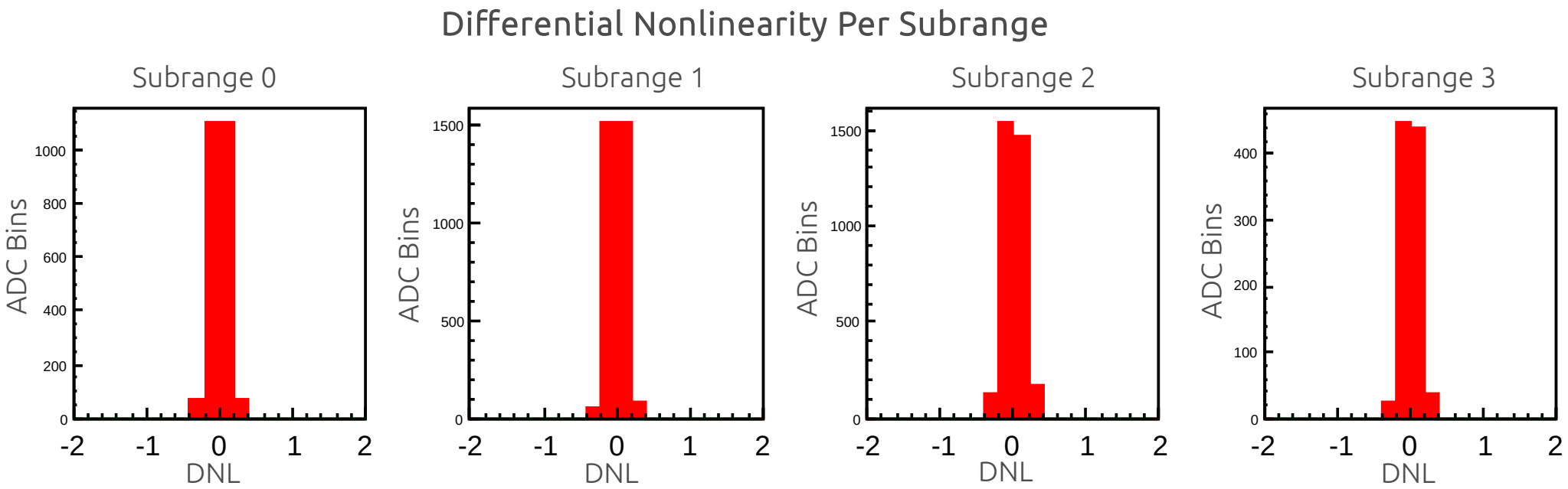
(3) ADC: Subranges

For 80 chips, we measure each subrange's bin width:

We don't expect measured bin widths to be exactly equal to the nominal values. Between chip production runs, **bin widths will differ on the order of 10 %** due to normal and expected process variations.

(3) ADC: Subranges

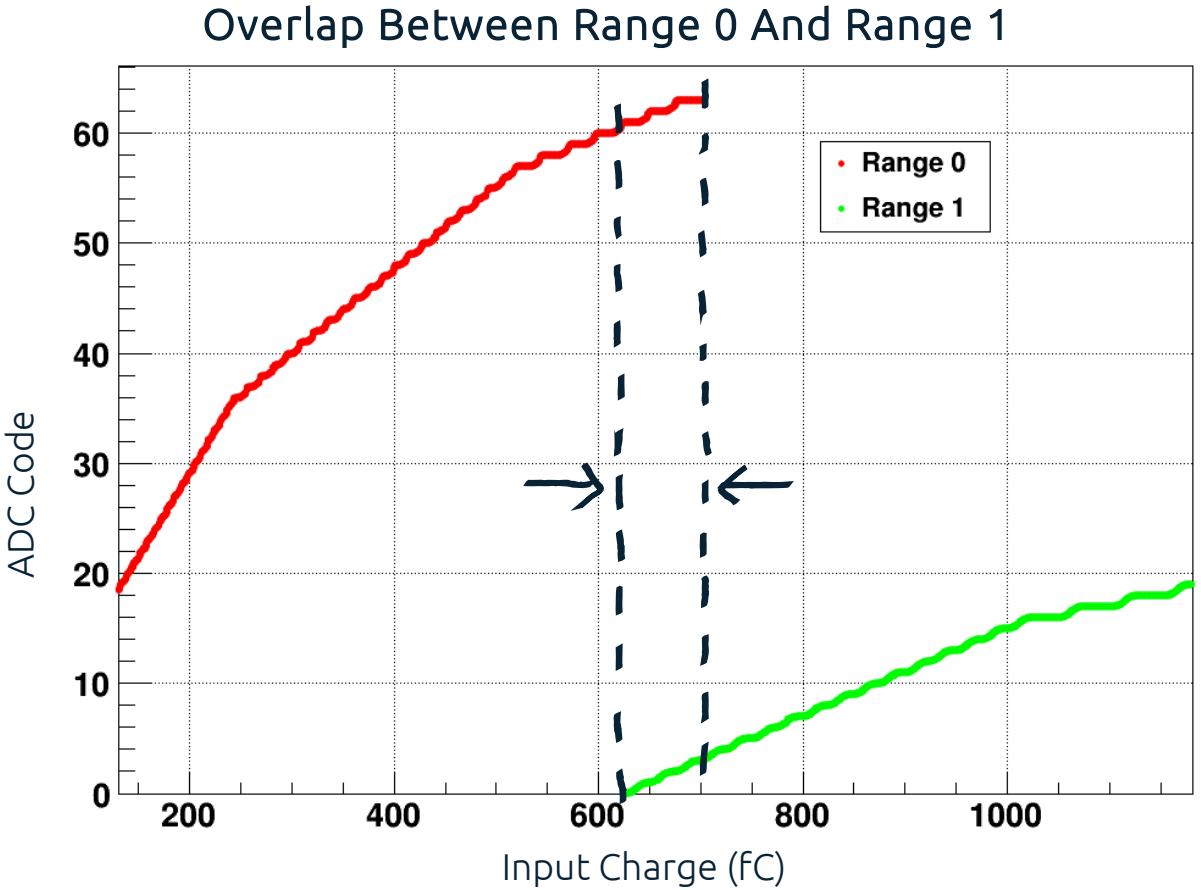
We want the bin widths to have the correct average value, but we also want the bins to be consistent within each subrange:



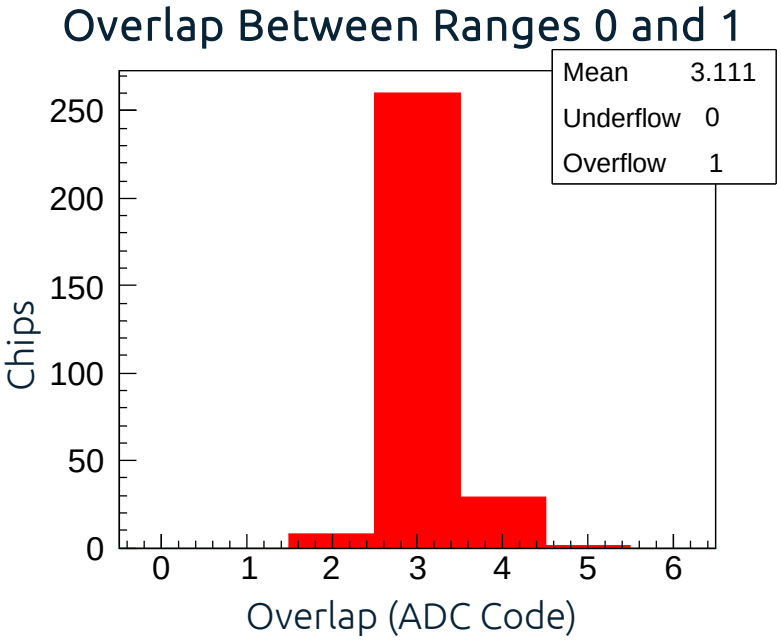
$$DNL = \frac{BIN\ WIDTH_{MEASURED} - WIDTH_{EXPECTED}}{WIDTH_{EXPECTED}}$$

(3) ADC: Range Overlap

The bins at the intersections between **ranges are intentionally constructed to overlap**. This prevents gaps between ranges, which would result in loss of signal. The bin width is the same for bins in the highest subrange of a specific range and the lowest subrange in the next range.

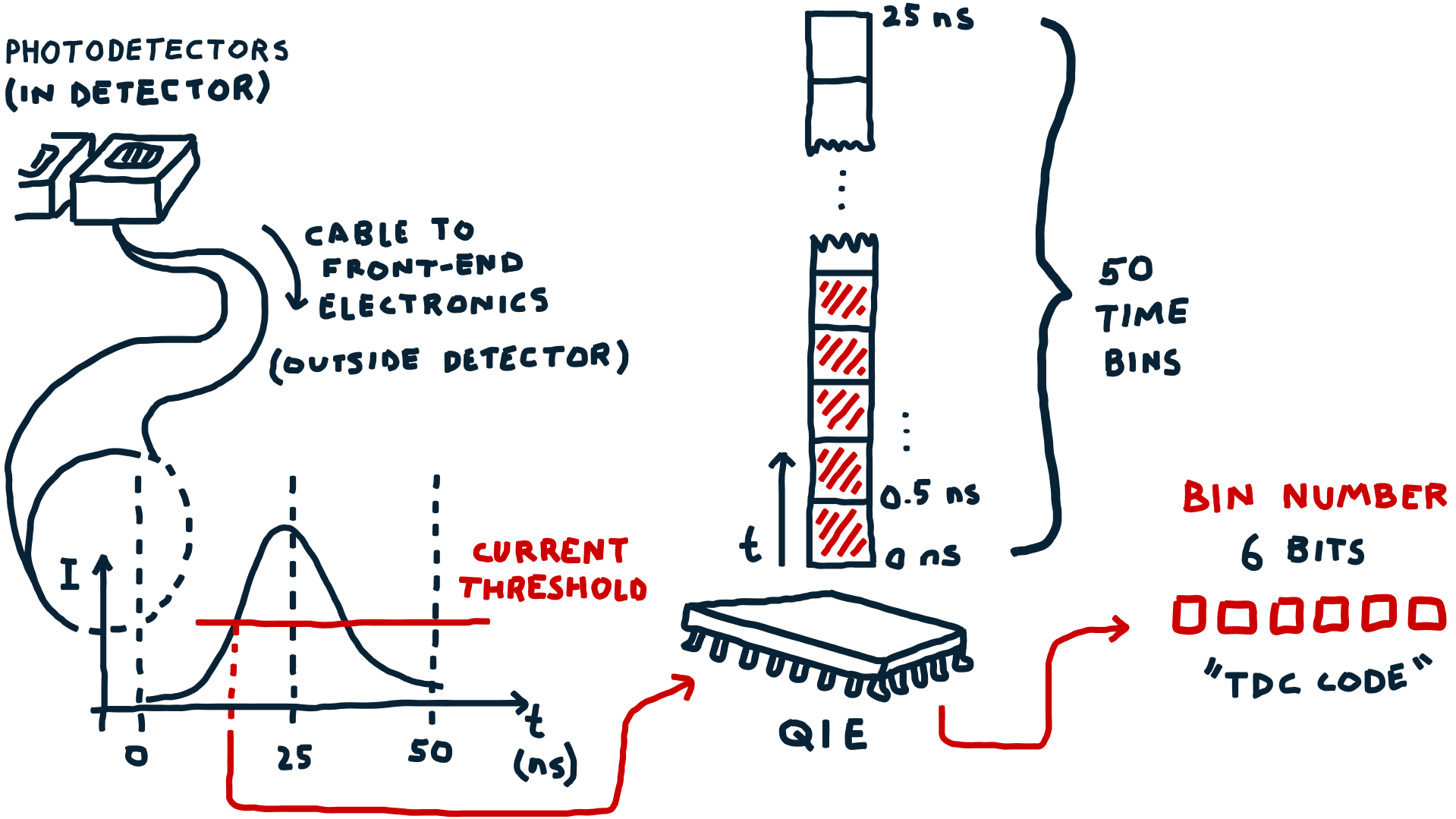


For 299 chips, we measure each range overlap:



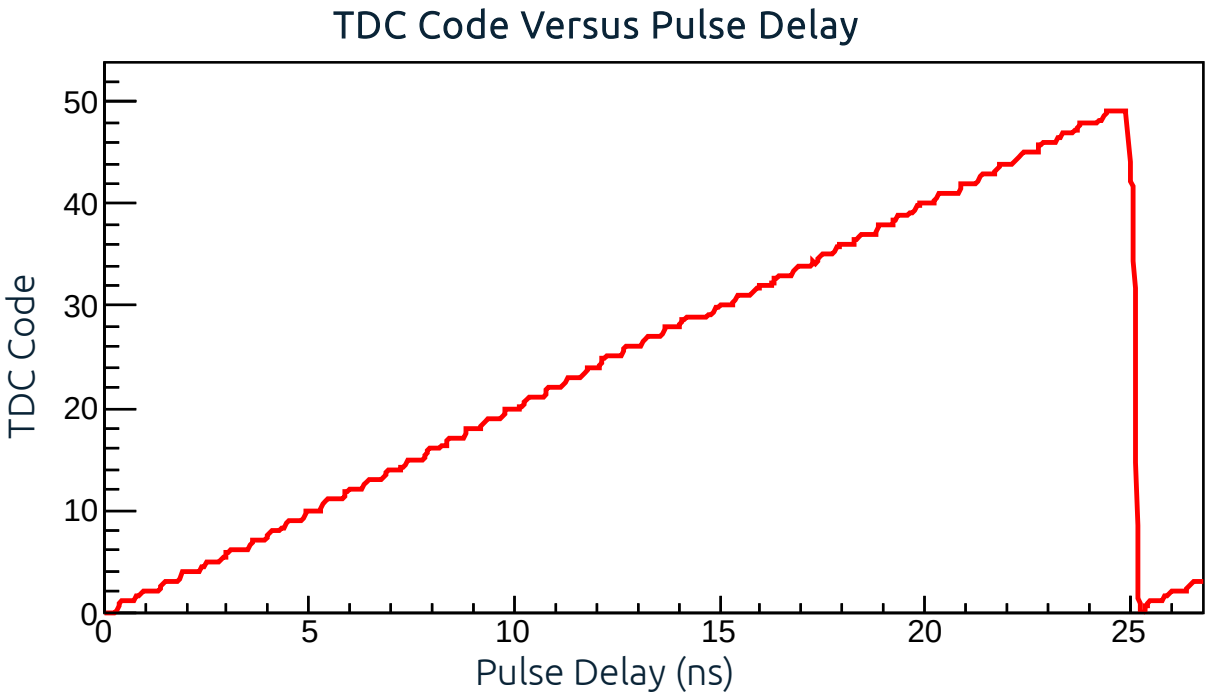
(4) TDC Response

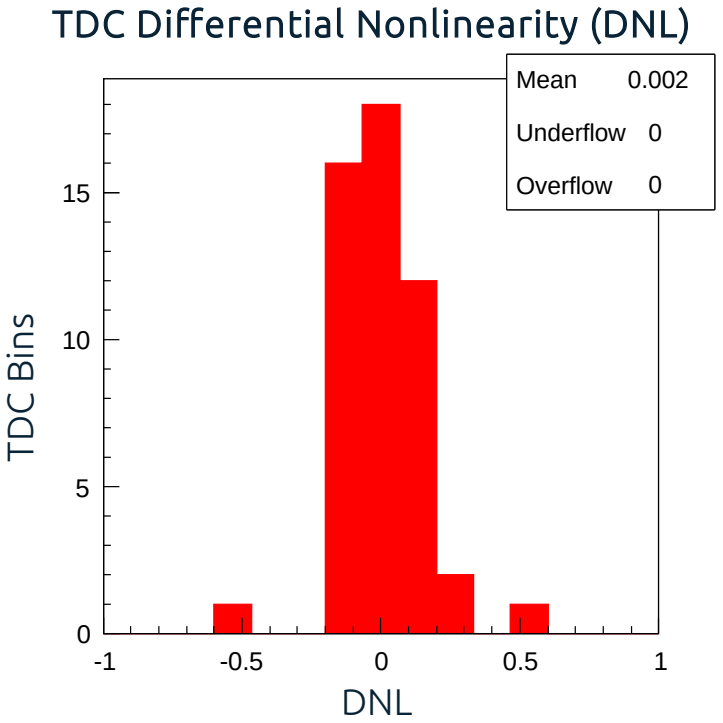
The following sketch illustrates how the TDC functionality works:



(4) TDC: Bin Architecture

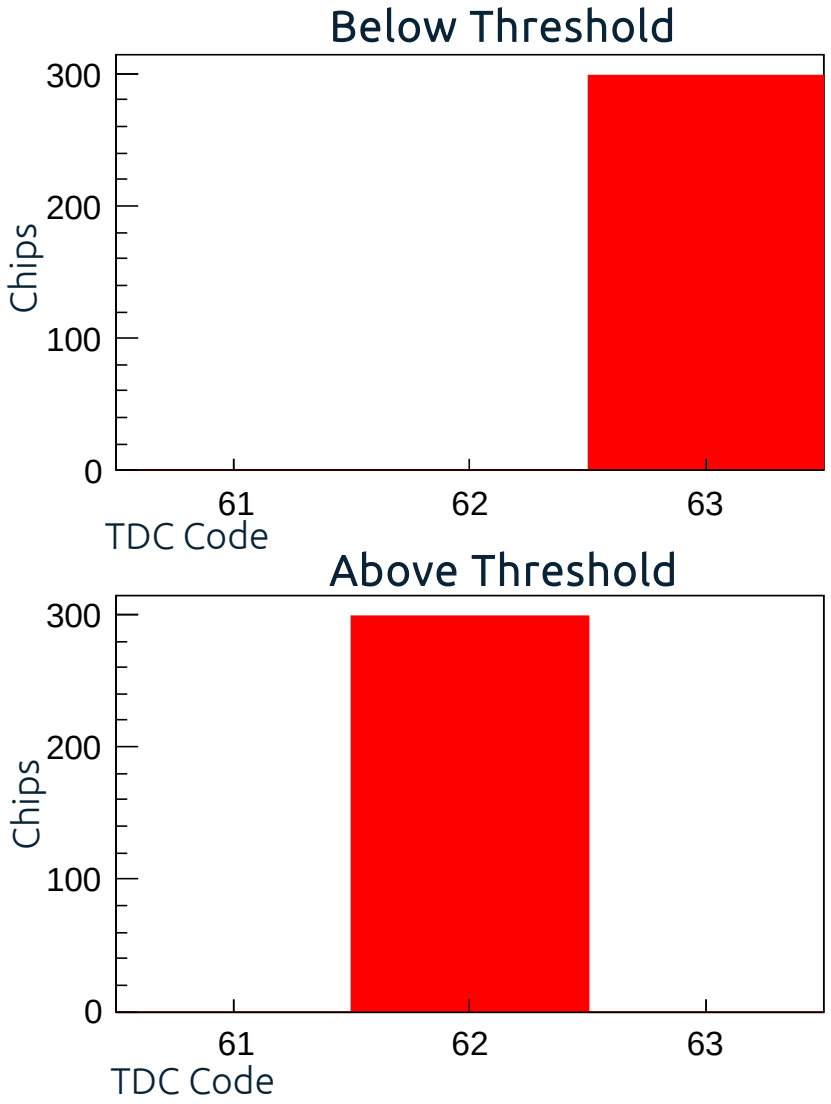
These plots show the TDC response of a chip:





Since **TDC functionality is a new feature** to the QIE, our original teststand is not ideally suited to studying TDC response. Each chip we look at in detail must be soldered to a modified testboard.

(4) TDC: Special Codes



For each chip, we set two different TDC thresholds and inject charge at points well below and well above this threshold.

Special Codes:

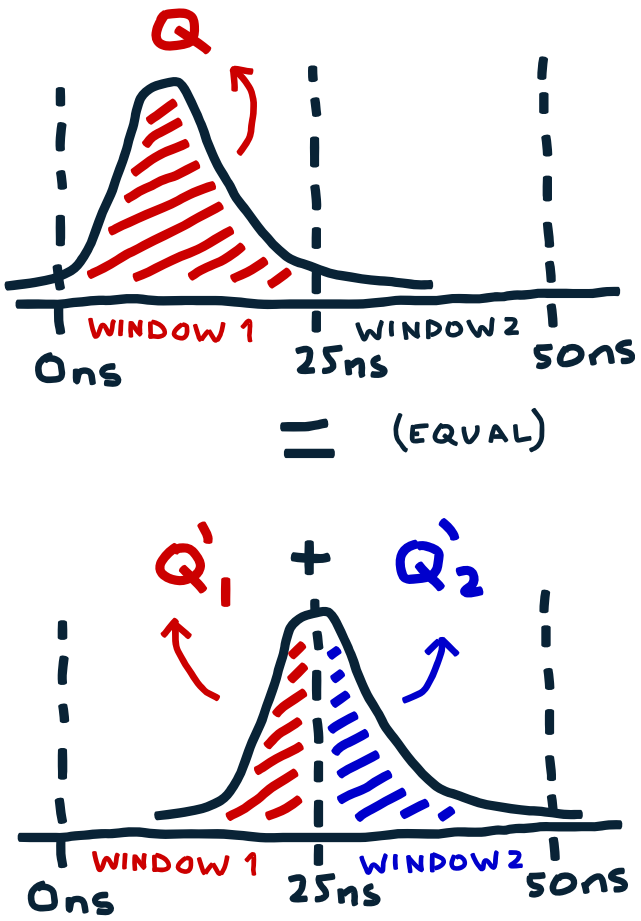
61: Delay lock loop unlocked. This is bad; it means the TDC won't function correctly.

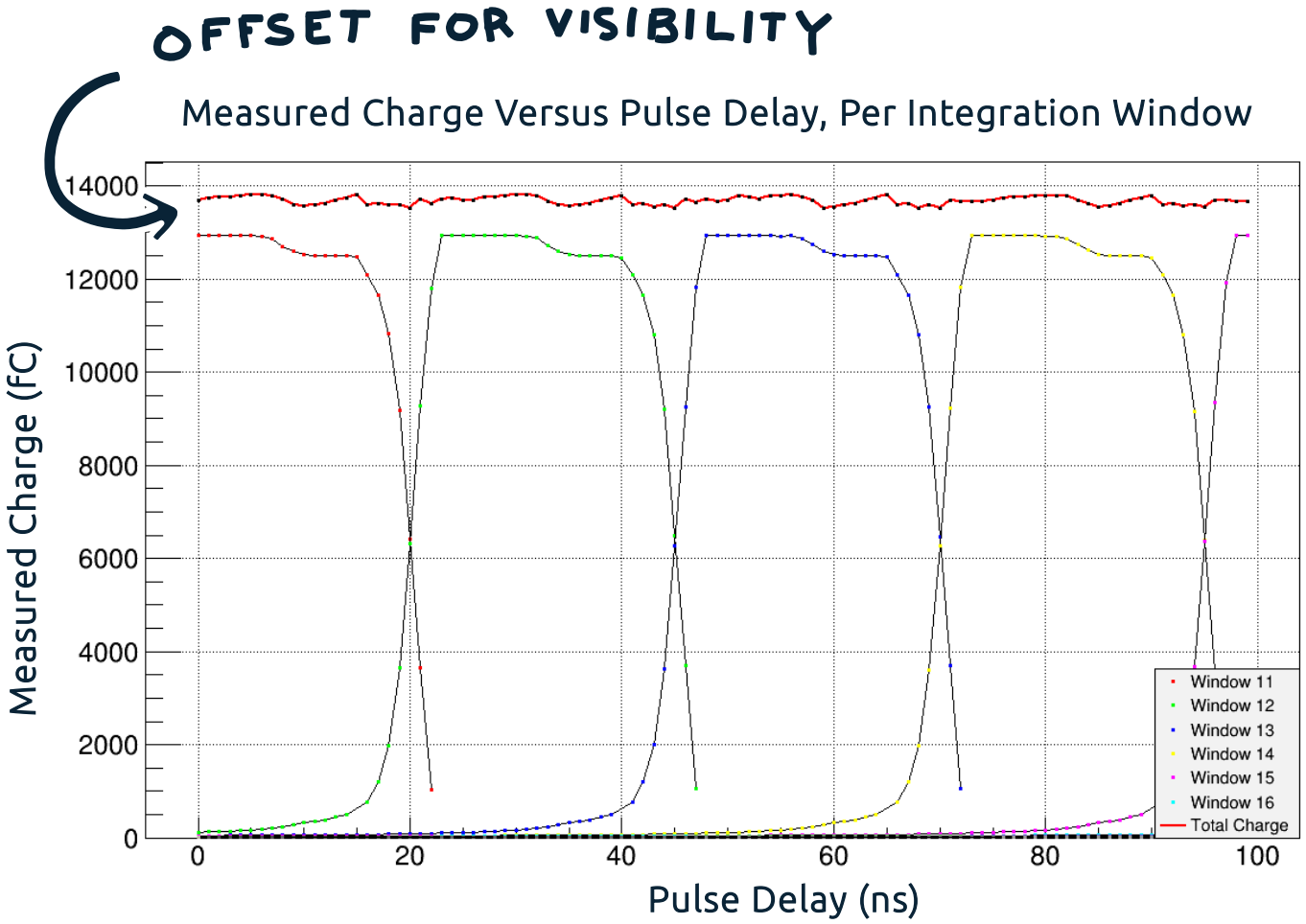
62: Input current stayed above threshold for the whole integration window.

63: Input current stayed below threshold for the whole integration window.

(5) Pulse Integration

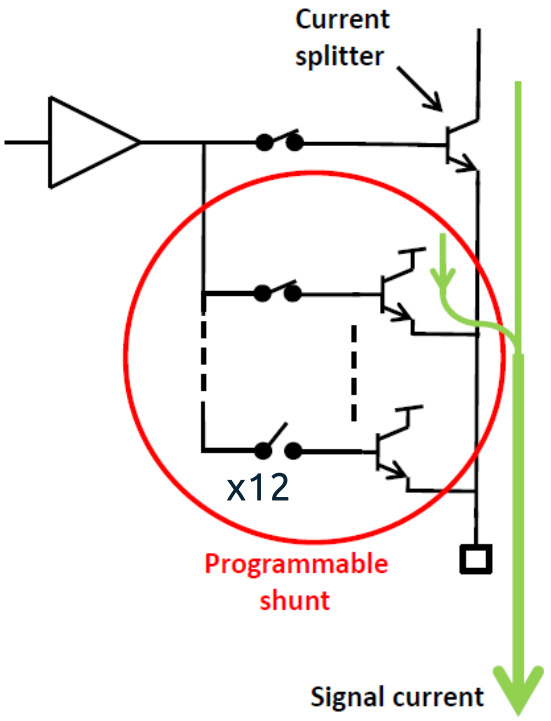
It's crucial that a pulse is integrated to the same total charge regardless of its position in time. In the following study, we slowly delay a pulse across a number of integration windows and find the total charge at each time:

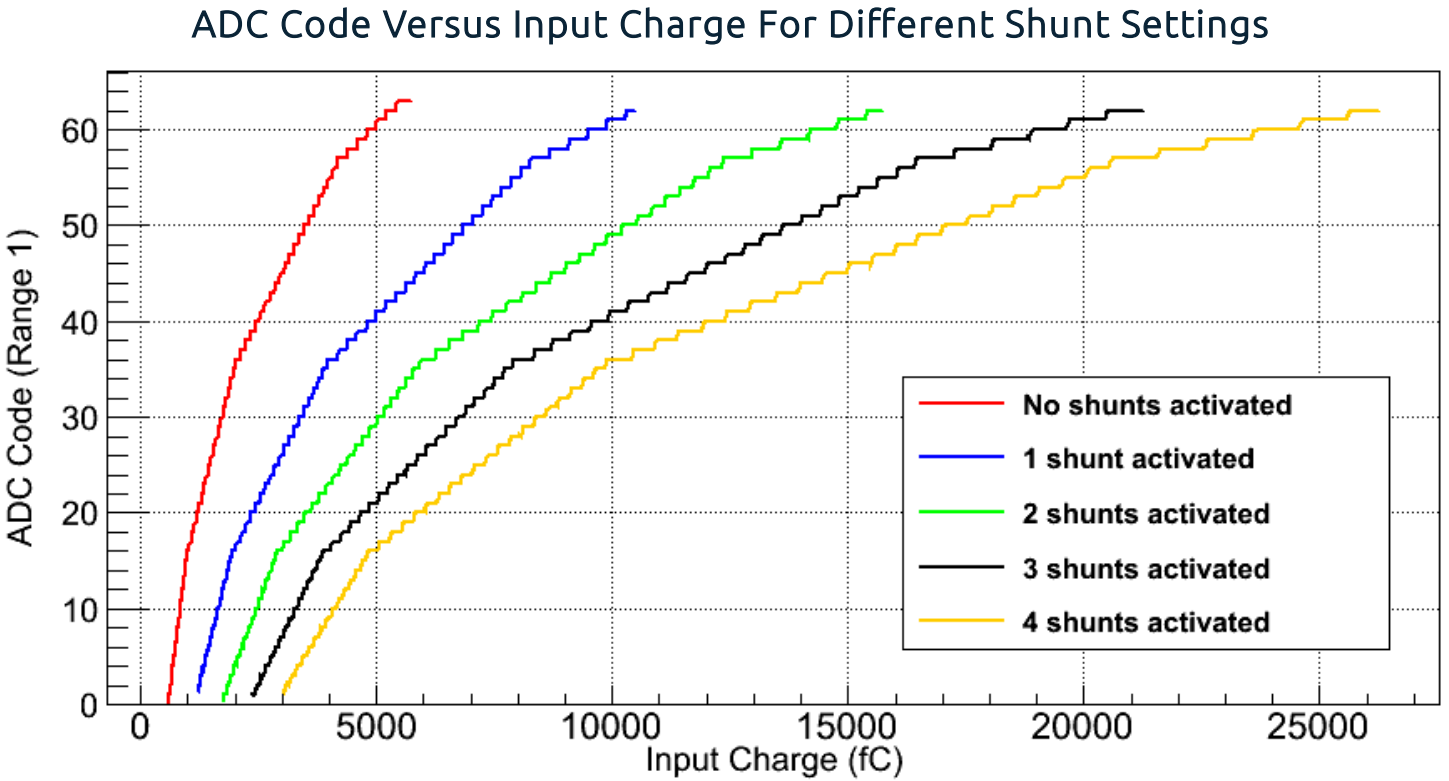




(5) Programmable Gain

There are 12 identical current shunts at the input of the QIE11. Together, they form a 12-valued programmable gain for the input signal. Here are the ADC response curves of five different shunt settings, for a representative chip:

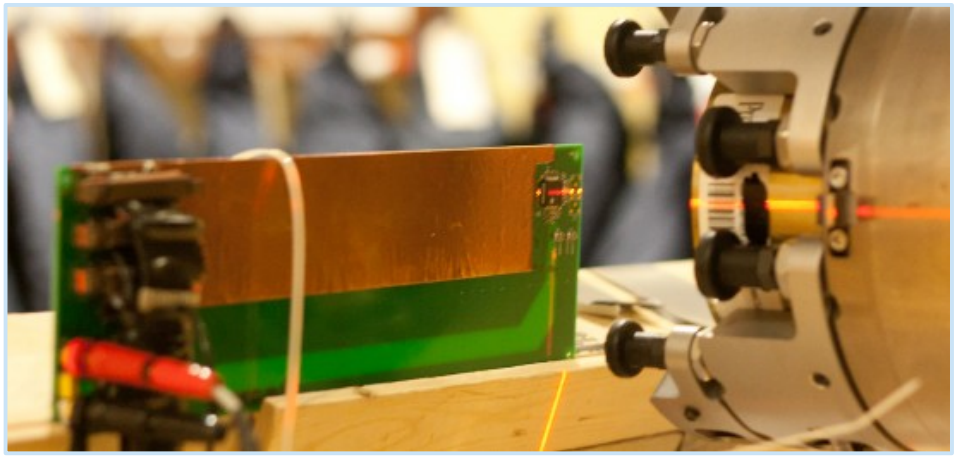


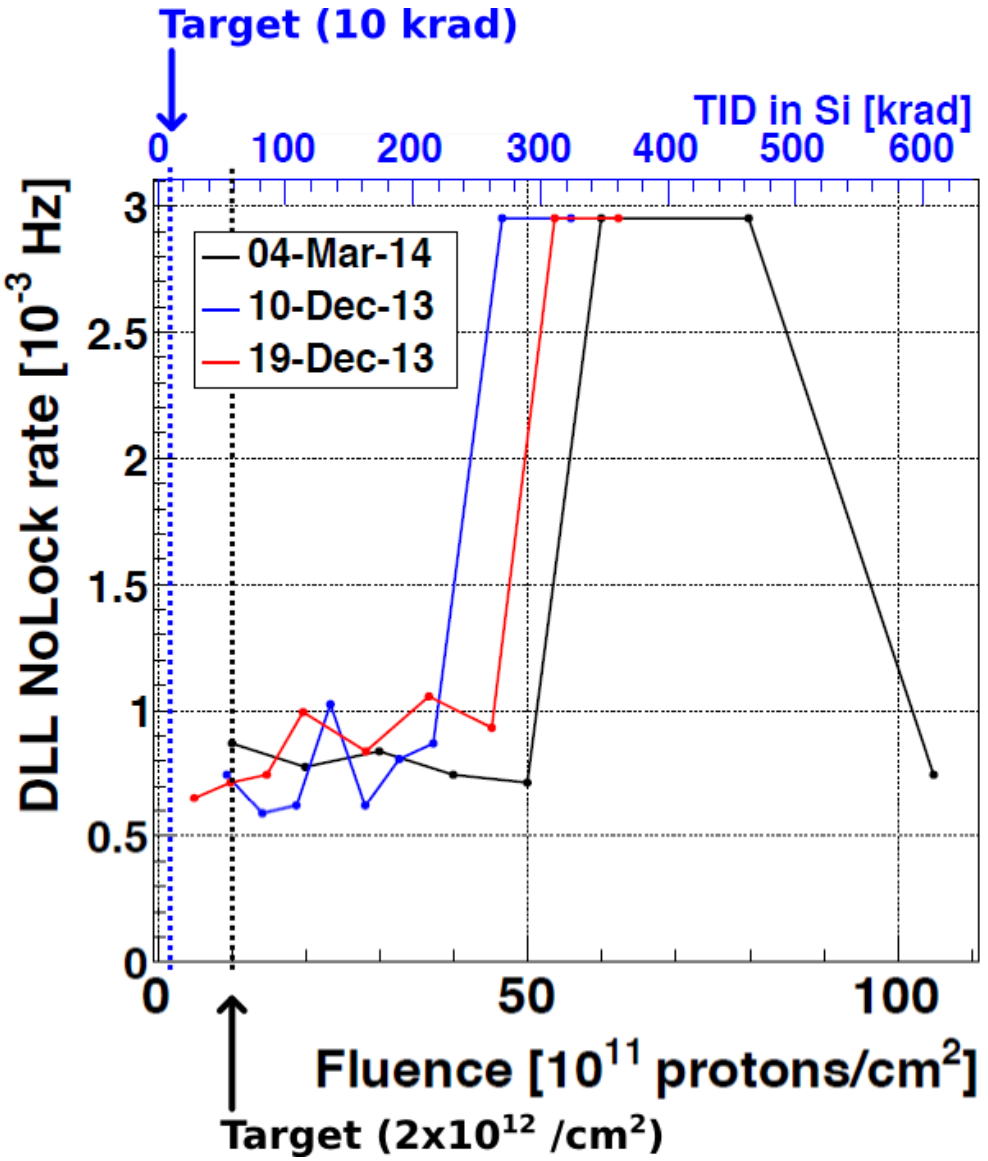


(6) Radiation Tests

The QIE10/11 is **more radiation tolerant than previous versions**:

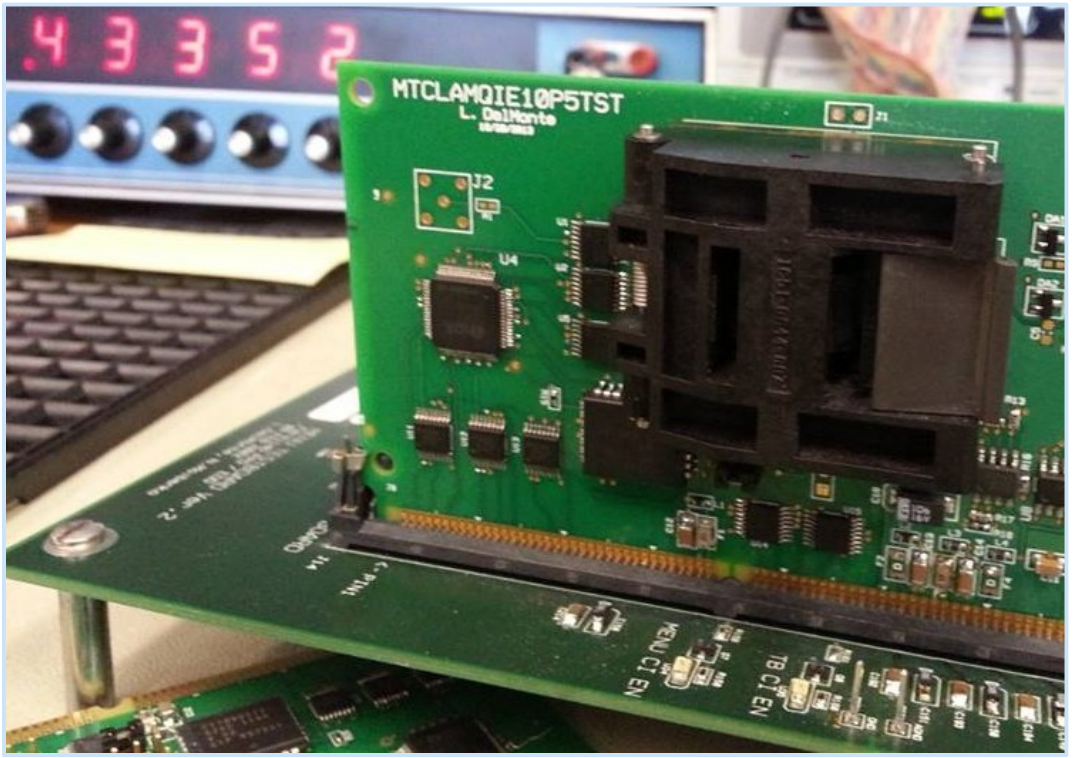
- The chip performs acceptably up to and past target specifications of 10 krad total ionizing dose (TID) and 2x1012 neutrons/cm2 of fluence.
- No errors were seen in parts of the chip designed to be radiation hard (the shadow register).





(7) Conclusion

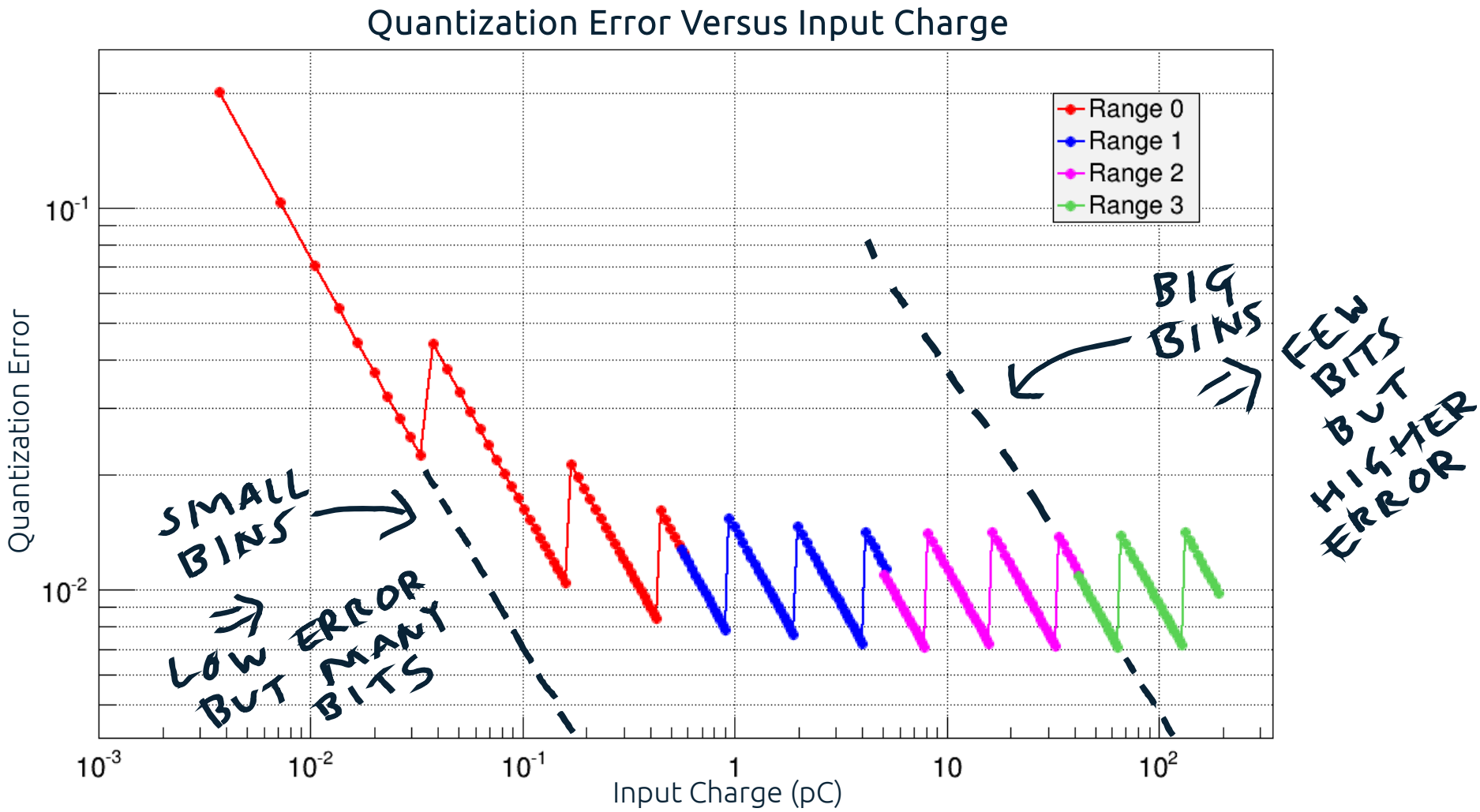
- Bench tests conducted at Fermilab have successfully validated the performance of the QIE10/11.
- The QIE10/11 design is complete and ready for the CMS HCAL Phase 1 Upgrade.
- The QIE10 might be used in other experiments: A Toroidal LHC Aparatus (ATLAS) and the CMS Beam Halo Monitor (BHM). Add your experiment to the list!



Teststand at Fermilab

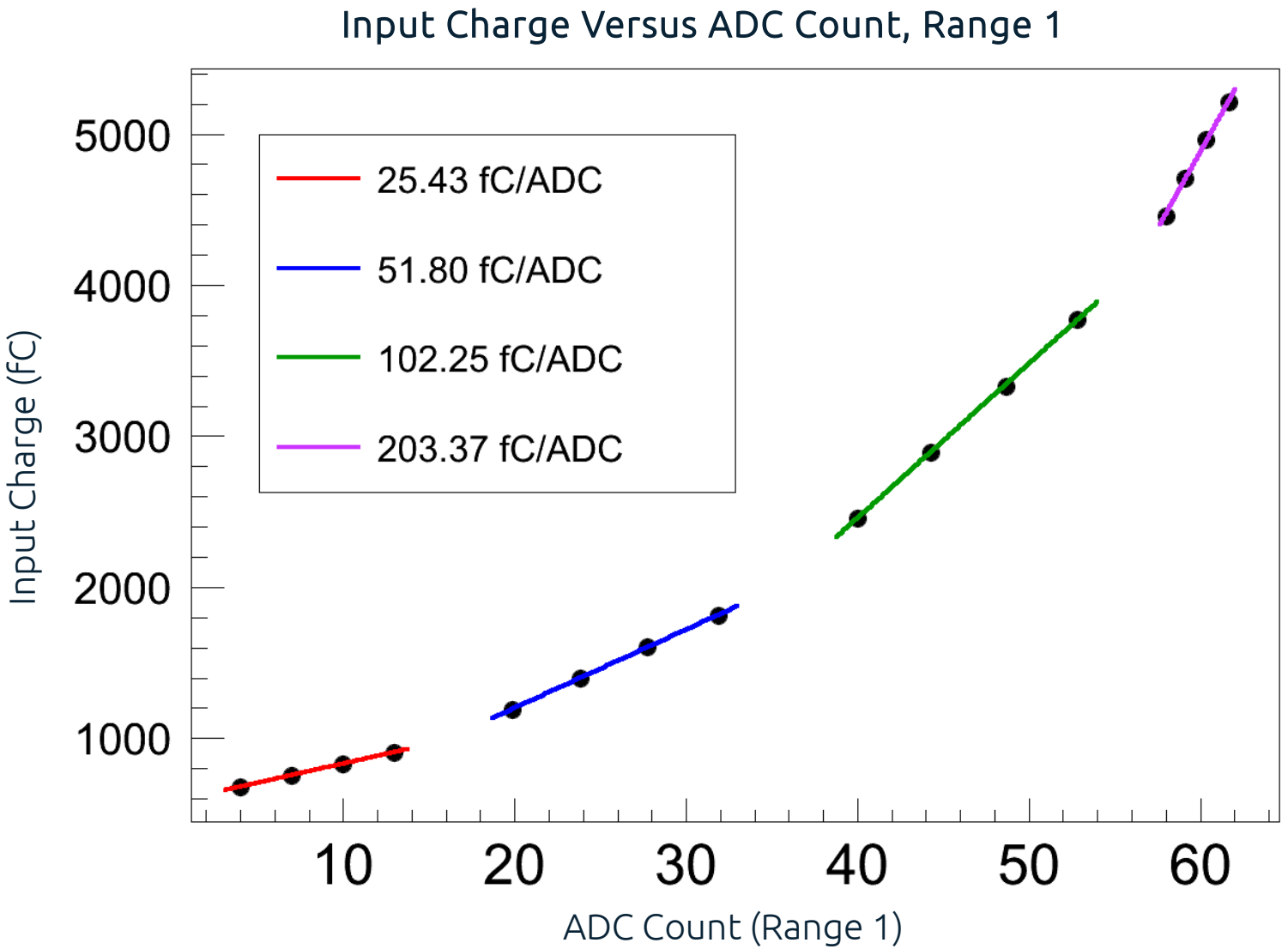
(-1) Extra

Why different bin sizes are necessary:



(-1) Extra

How to coarsely measure bin widths:



(-1) Extra

This is how we measure the range overlap: