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Triroc: 64-channel SiPM read-out ASIC for PET/PET-ToF application

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Triroc is the latest addition to SiPM readout ASICs family developed at Weeroc, a start-up company from the Omega microelectronics group of IN2P3/CNRS. This chip developed under the framework TRIMAGE European project which is aimed for building a cost effective tri-modal PET/MR/EEG brain scan. To ensure the flexibility and compatibility with any SiPM in the market, the ASIC is designed to be capable of accepting negative and positive polarity input signals.

This 64-channel ASIC, is suitable for SiPM readout which requires high accuracy timing and charge measurements. Targeted applications would be PET prototyping with time-of-flight capability. Main features of Triroc includes high dynamic range ADC up to 2500 photoelectrons and TDC fine time binning of 40 ps. Triroc requires very minimal external components which means it is a good contender for compact multichannel PET prototyping.

Triroc is designed by using AMS 0.35 μ m SiGe technology and submitted in March 2014. The detail design of this chip will be presented.

Summary

Triroc is a 64-channel silicon photomultiplier (SiPM) readout ASIC targeted for Time-of-Flight Positron Emission Tomography (TOF-PET) application. This chip developed for TRIMAGE project which is aimed for building a cost effective tri-modal PET/MR/EEG brain scan.

The low-noise, DC-coupled front-end amplifiers of this ASIC accept both negative and positive input signals thus making it suitable for reading out any SiPM in the market. Moreover, individual input DC level adjustment is available for correcting the non-uniformity of SiPM gain.

In each ASIC channel, the incoming signals will be sent into two different paths: for energy and time measurements. A variable gain semi-gaussian shaper is used for shaping the input signal in energy measurements. The energy conversion is handled by a 10-bit Wilkinson ADC. This ADC is a proven design and it is expected to be linear up to 2500 photoelectrons. Additionally, a charge trigger is available and can be used for events validation at required energy such as 511 keV.

Signal from high speed input pre-amplifier is fed into a discriminator in order to provide a fast trigger for time measurements. A TDC module with coarse and 40 ps fine time is used to time-stamp this trigger.

The digitized data are collected by the digital part which is also capable to validate 511 keV events and reject noise. Running at 80 Mhz, data will be transmitted through 4-bits parallel links. Other features on the digital side are zero suppress readout and TDC data compression. In all, the ASIC should be able to process up to 30k events per second.

Triroc can be operated with minimal external components, since most of the components for SiPM readout are packed internally. This feature makes the ASIC is a good contender in compact multi-channel PET applications. Triroc is designed by using AMS 0.35 μ m SiGe technology and will be submitted in March 2014.

Author: Dr AHMAD, Salleh (Weeroc SAS)

Co-authors: Dr DE LA TAILLE, Christophe (OMEGA-Ecole Polytechnique-CNRS/IN2P3); Mr THIENPONT, Damien (OMEGA-Ecole Polytechnique-CNRS/IN2P3); Mr DULUCQ, FREDERIC (OMEGA-Ecole Polytechnique-CNRS/IN2P3); Dr MARTIN CHASSARD, Gisele (OMEGA (FR)); Mr FLEURY, Julien (Weeroc SAS); Mr RAUX, Ludovic (OMEGA-Ecole Polytechnique-CNRS/IN2P3); Mrs SEGUIN-MOREAU, Nathalie (OMEGA-Ecole Polytechnique-CNRS/IN2P3); Mr CALLIER, Stephane (OMEGA-Ecole Polytechnique-CNRS/IN2P3)

Presenter: Dr AHMAD, Salleh (Weeroc SAS)

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