

Monolithic pixel detectors fabricated with single and double SOI wafers

T. Miyoshi, Y. Arai, Y. Fujita, Y. Ikemoto, K. Hara¹, S. Honda¹, Y. Ikegami, S. Mitsui, A. Takeda², K. Tauchi, T. Tsuboyama, Y. Unno

High Energy Accelerator Research Organization (KEK)

¹Univ. of Tsukuba

²Kyoto University

Thursday

I.b Semiconductors

11:00 - 12:40

Berlagezaal

@Beurs van Berlage

Outlines

INTPIXh2
MX1594
6mm-sq.

Introduction

Test results of “INTPIXh2” SOI sensors
(Integration-type pixel sensor)

Future plan and summary

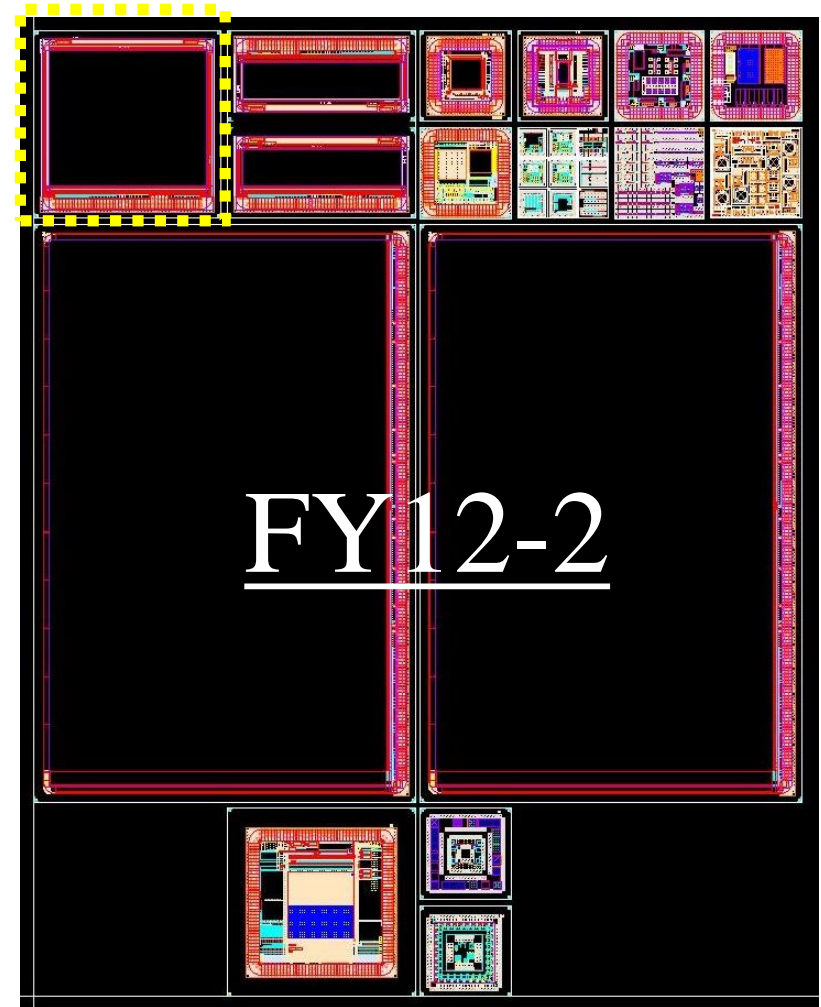
Related slides:

II.b Astro & Space

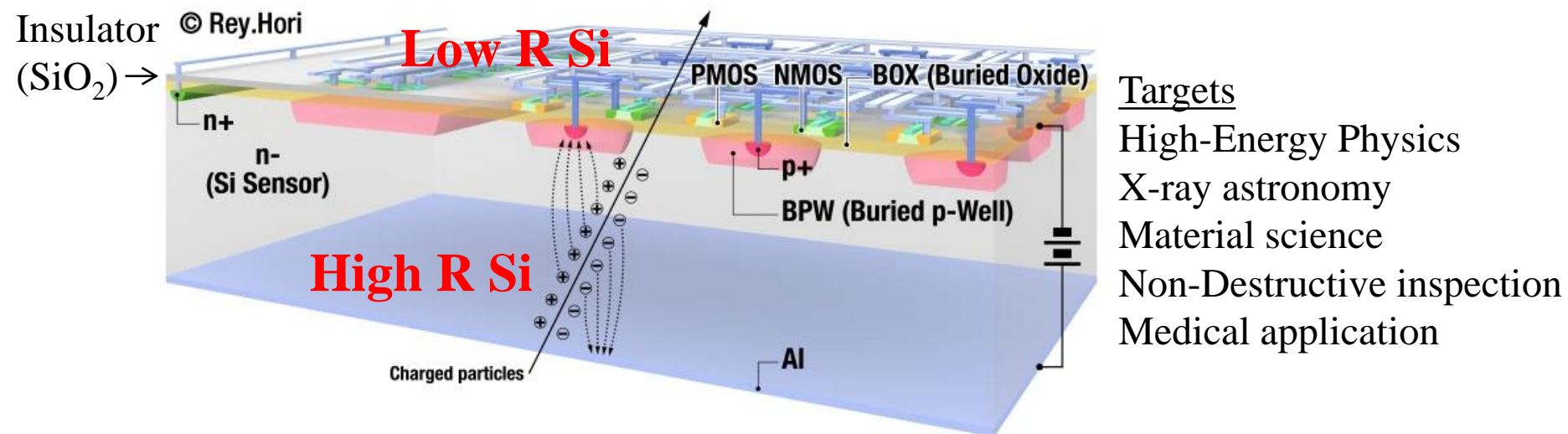
11:20 Development and Evaluation of Event-Driven SOI Pixel Detector for X-ray Astronomy

11:40 Development of X-ray SOI Pixel Sensors: Investigation of Charge-Collection Efficiency

→XRPIX (Integration type pixel sensor)



SOI Monolithic pixel detector



The features of SOI monolithic pixel detector

- No mechanical bump bonding. Fabricated with semiconductor process only
→ high reliability and low cost
- Fully depleted (thick & thin) sensing region
with low sense node capacitance ($\sim 10\text{fF}@17\mu\text{m}$ pixel) → high sensor gain
- Wide temperature range (1-570K)
- Low single event cross section
- Technology based on industry standards

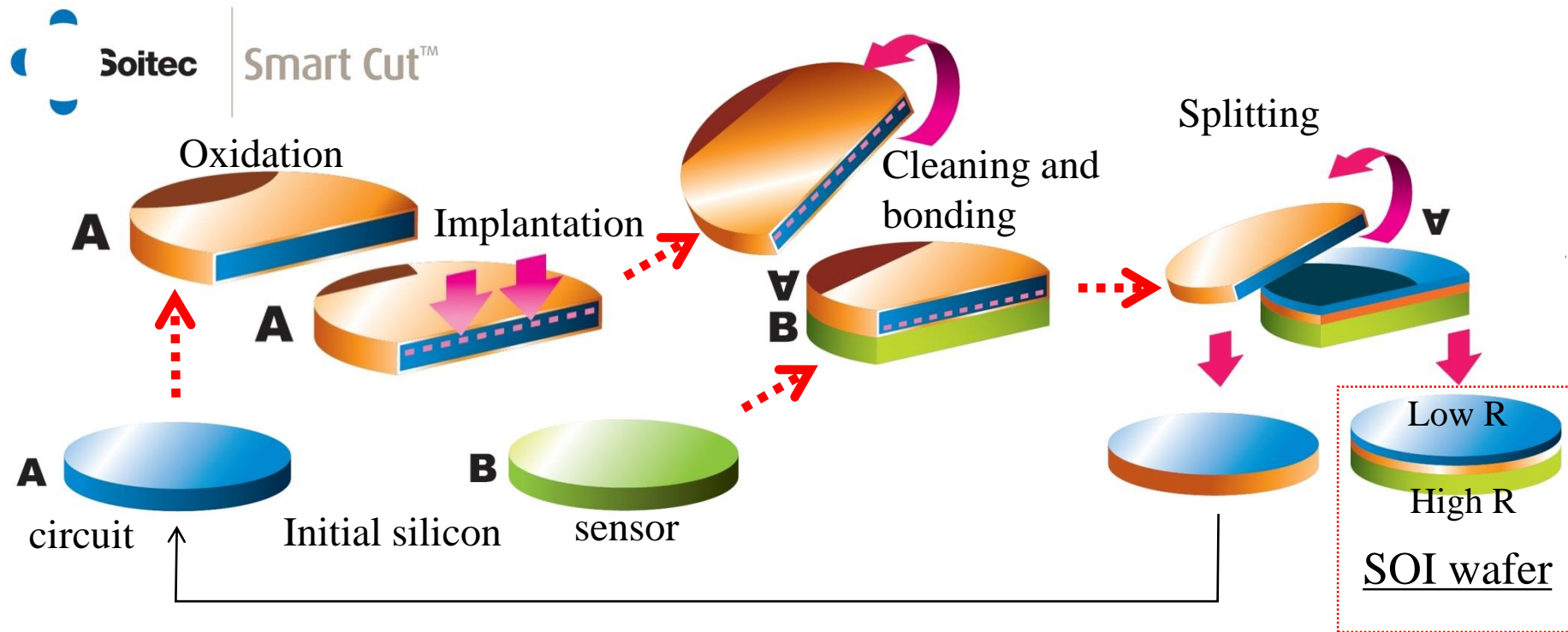
Process Summary

- KEK organizes MPW runs twice a year
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip

Process (Lapis Semiconductor Co. Ltd.)	0.2 μ m Low-Leakage Fully-Depleted (FD) SOI CMOS 1 Poly, 5 Metal layers (MIM Capacitor and DMOS option) Core (I/O) voltage : 1.8 (3.3) V
SOI wafer (200 mm ϕ =8 inch)	Top Si : Cz, ~18 Ω -cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer thickness: 725 μ m \rightarrow thinned up to 300 μ m (Lapis) or ~50 μ m (commercial process) (Handle wafer type: see the following slides)
Backside process (2011~)	Mechanical Grind \rightarrow Chemical Etching \rightarrow Back side Implant \rightarrow Laser Annealing \rightarrow Al plating

SOI Wafer Production

Smart cut™ by Soitec

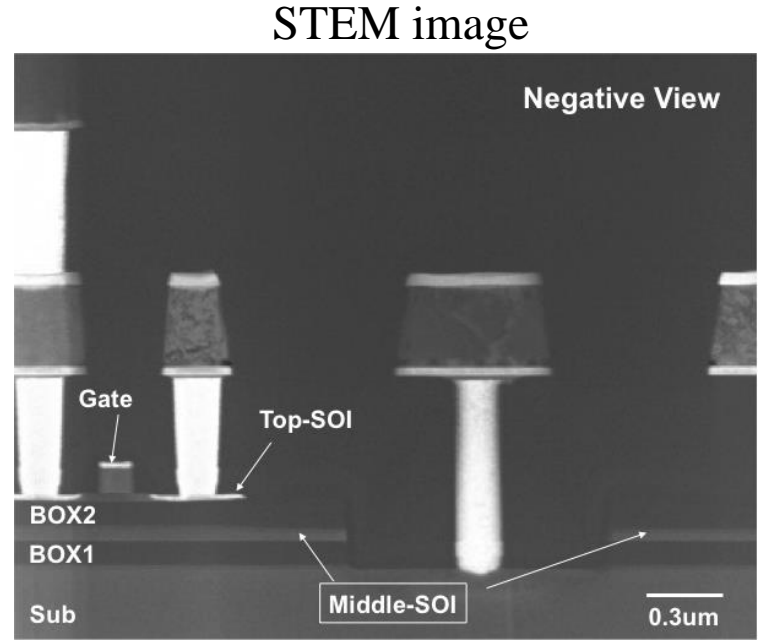
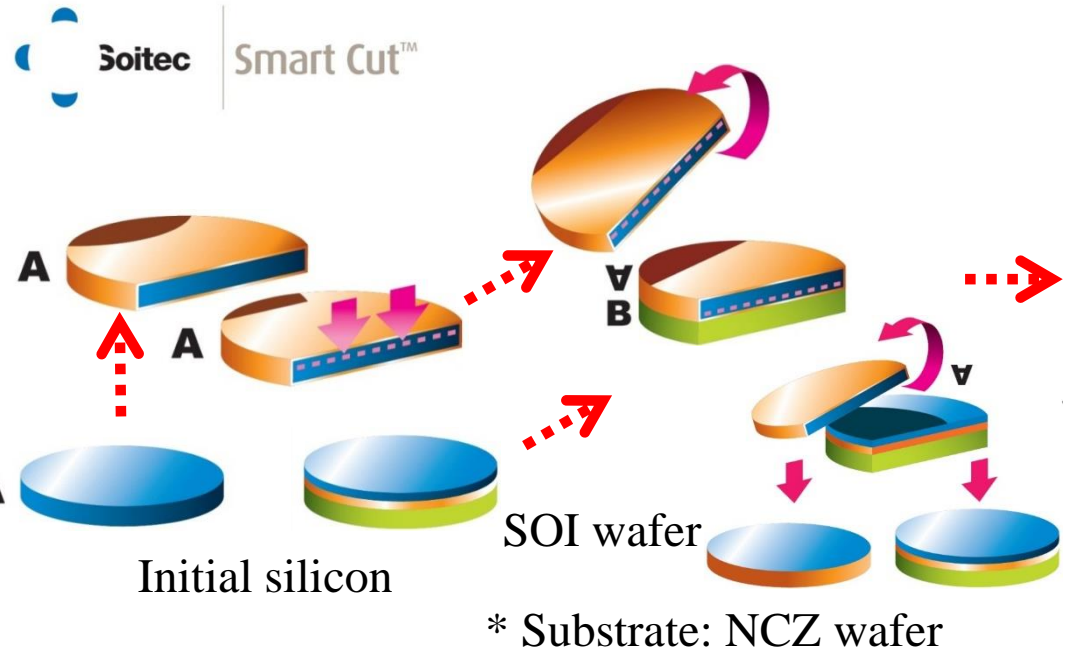


High Resistivity Silicon: Two choices

N-type Czochralski, NCZ, 700 Ohm-cm, 300um-thick

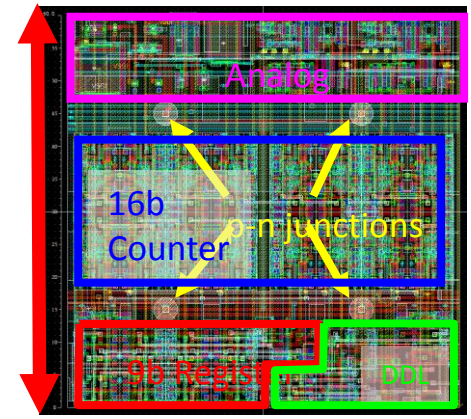
N-type Float Zone, NFZ, 2-7k Ohm-cm, 500um-thick

Double SOI pixel sensor



Additional shield layer

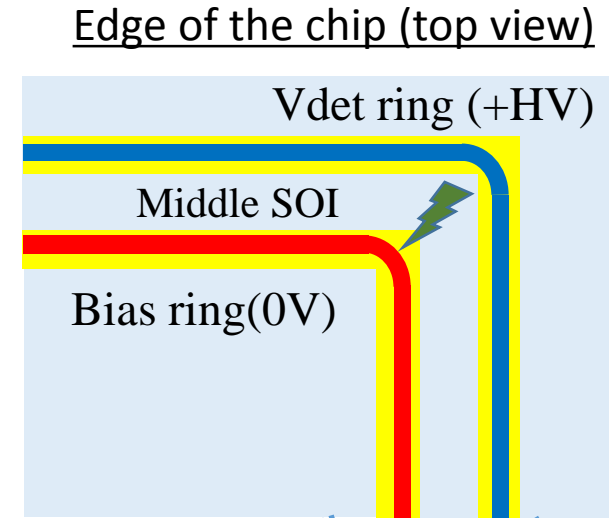
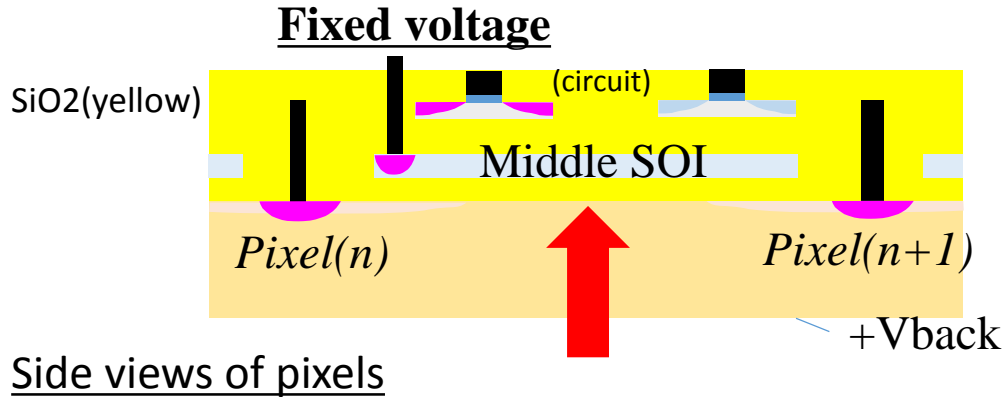
Shield the back gate effect
 Compensate effect of box charge
 Shield the sensor to circuit crosstalk
 → counting-type pixel (CNTPIX) with double SOI wafer is now being developed.



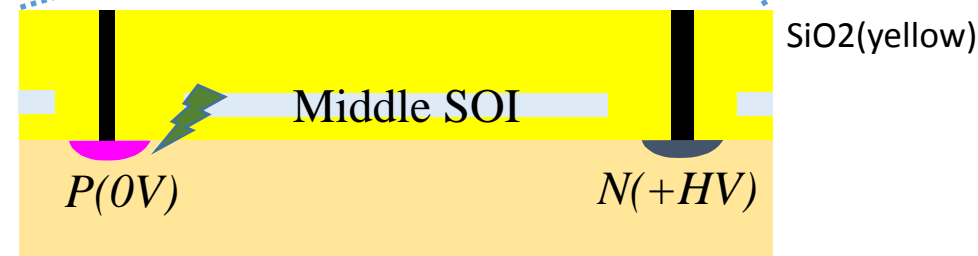
64um-sq. counting-type pixel

Double SOI sensor development

The 1st trial in MPW FY11 Mask layout : Draw etching region of the middle SOI



- potential between pixels is flat.
- Affects charge collection efficiency
- micro discharge at the edge of outer guard ring occurred due to potential change by the floating middle SOI
- Lower breakdown voltage

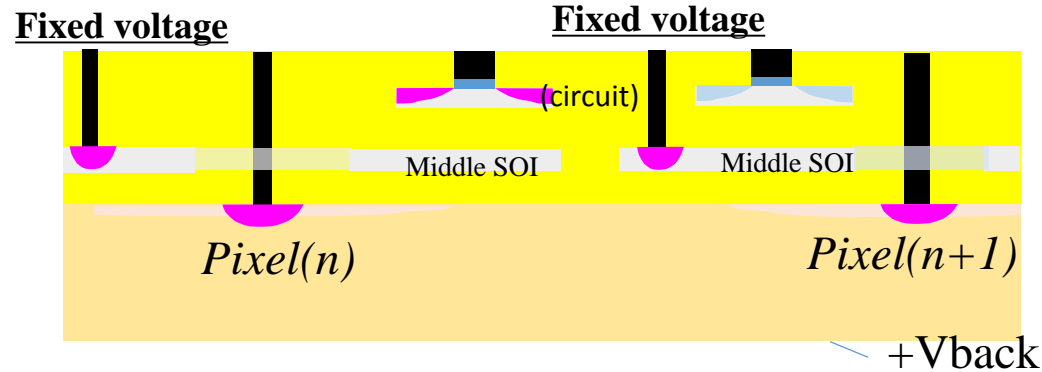


Edge of the chip (side view)

Double SOI sensor development

The 2nd trial in MPW 12-1 & 12-2

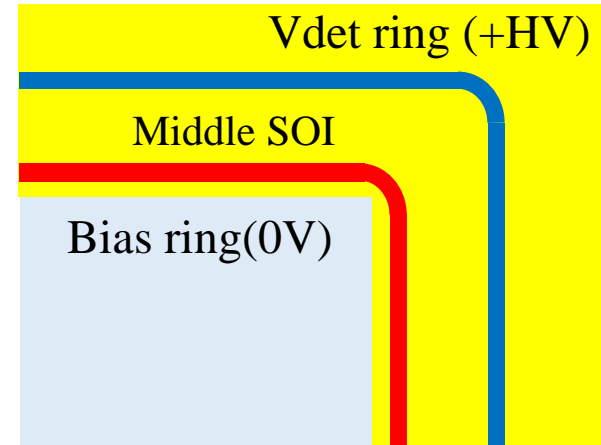
Layout rule was changed to draw middle SOI region directly



The side view of pixels

- potential between pixels is not flat
→ spatial resolution study
- recover high breakdown voltages
→ I-V measurement

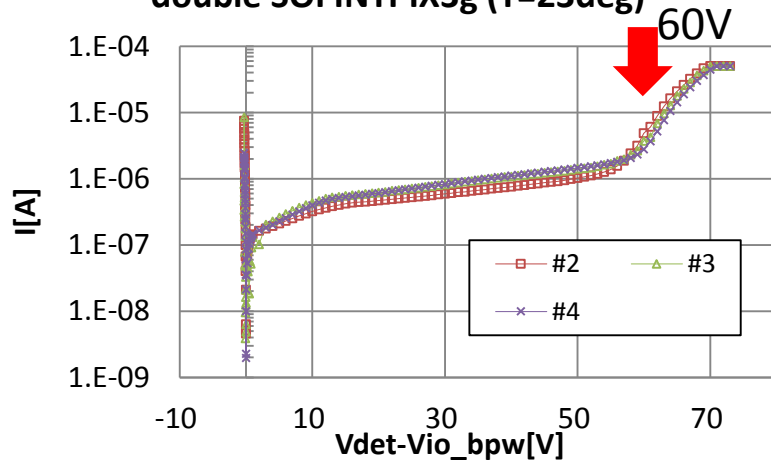
Edge of the chip (top view)



Double SOI sensor I-V measurement

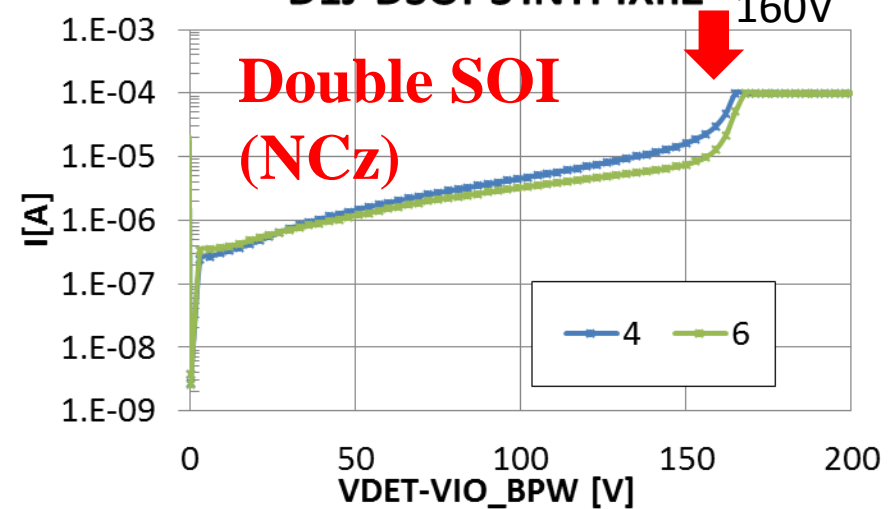
Double SOI 1st trial

double SOI INTPIX3g (T=23deg)



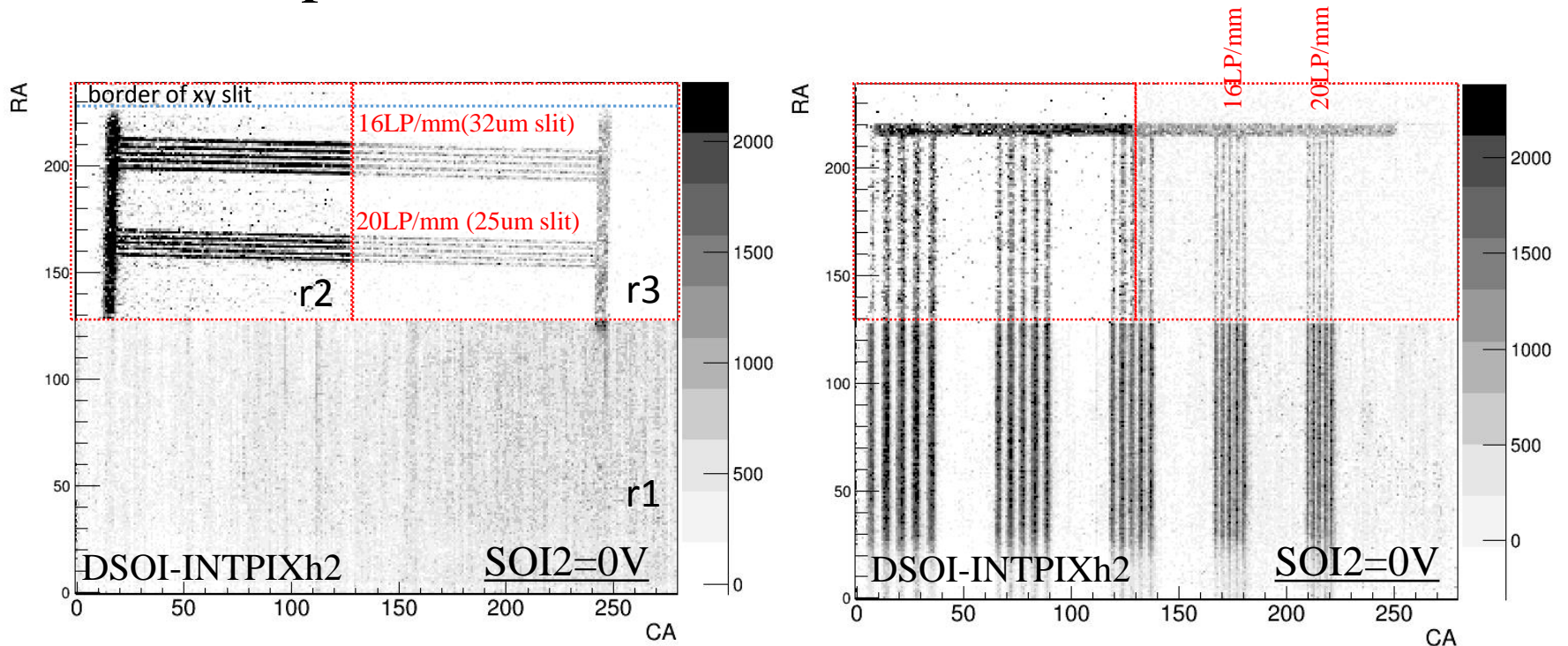
Double SOI 2nd trial

D1J-DSOI-3 INTPIXh2



Breakdown voltage is recovered similar to the single SOI case

Spatial resolution in Double SOI sensor



X-ray test chart

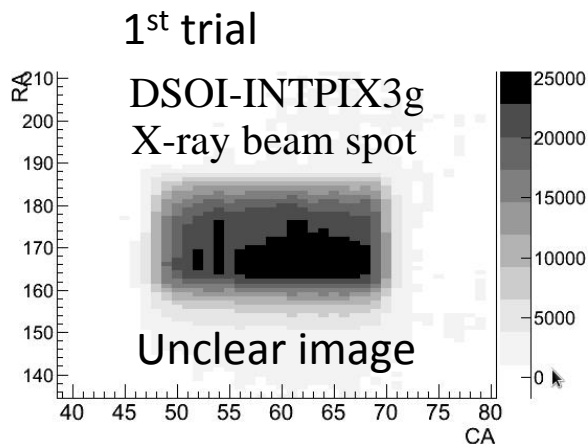
Mo Target X-ray (17.5keV)

Vdet +50V

Integration Time 50us/image x 1000 frames

25um slit can be resolved.

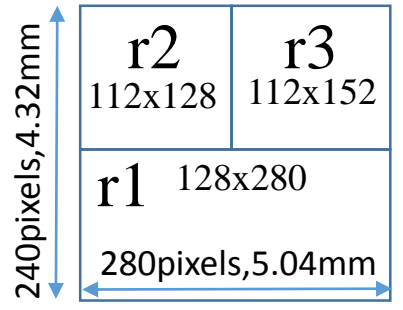
Effective to remove double SOI layer between pixels.



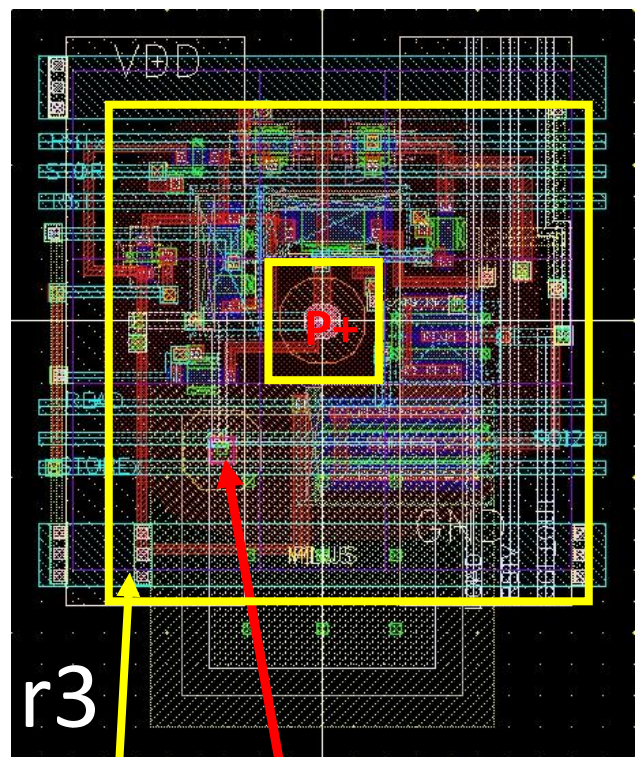
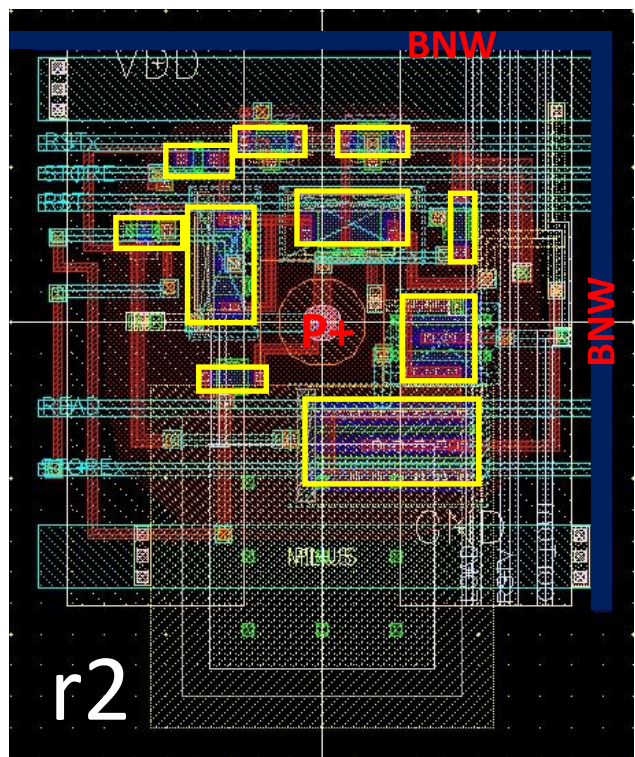
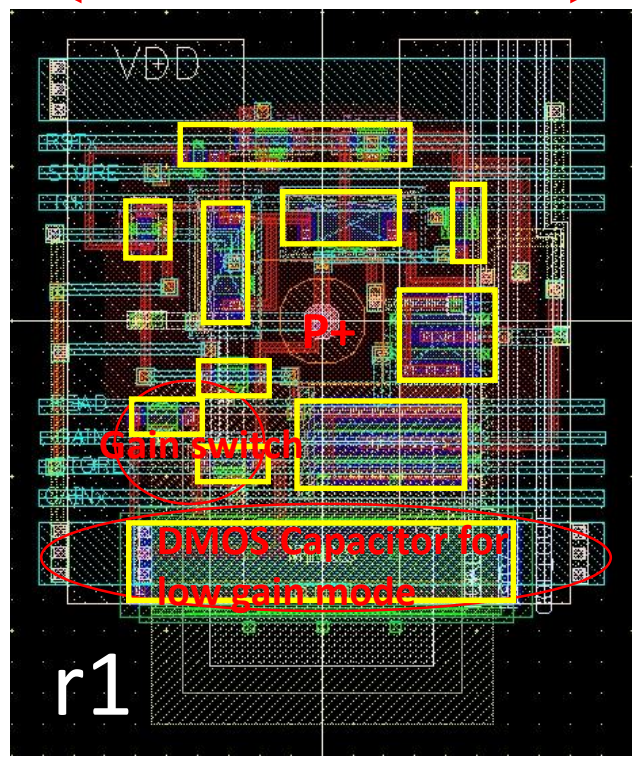
Sensor study

Top View of 3 Pixels

INTPIXh2
MPW12-2 MX1594
6mm-sq chip



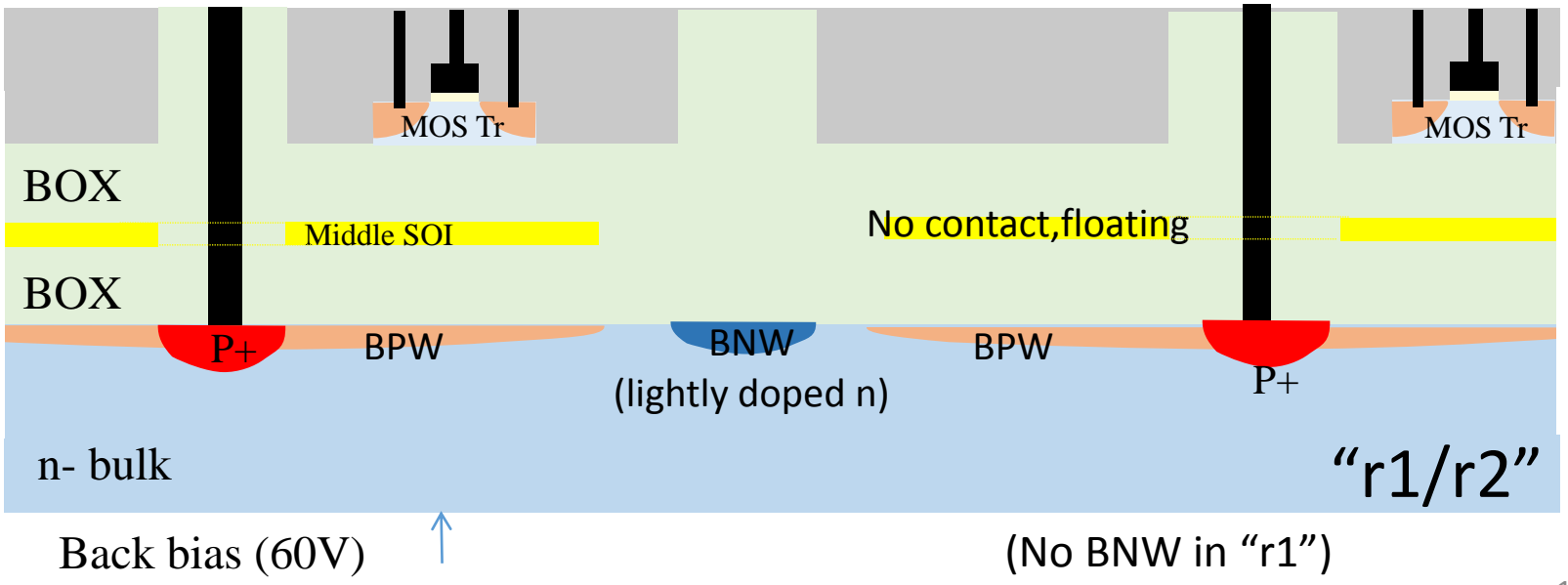
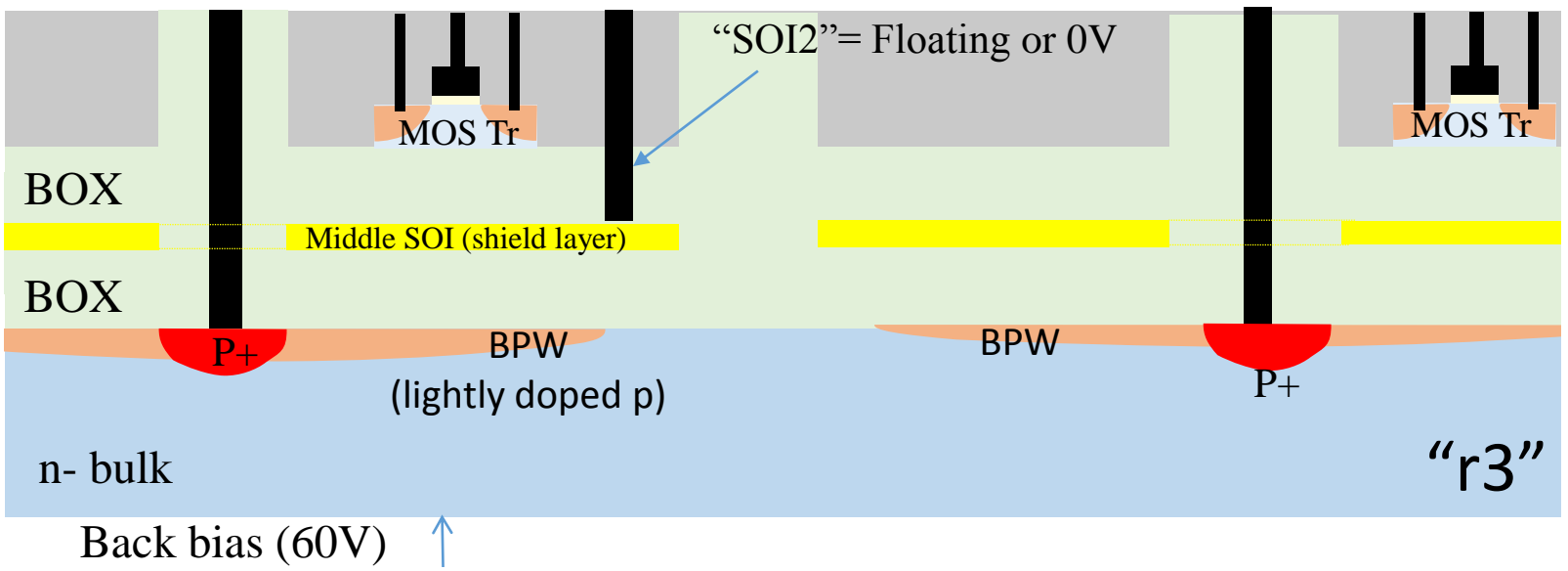
Pixel size 18um-sq



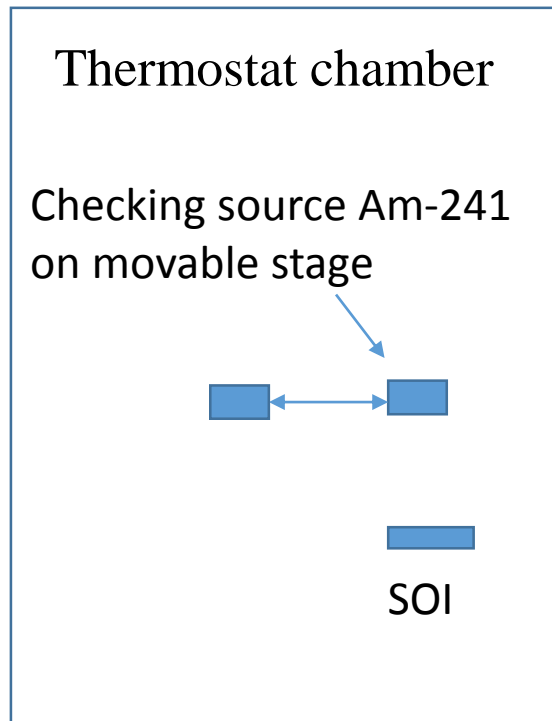
SOI2 layers are kept only Below the active area

SOI2 (rectangle) 16um x 16um

Side view of Pixels



Low temperature test of noise and energy resolution



Min. -60 degC ~ Room temp.

- Leakage current
- Am-241 X-ray spectrum
- Noise, Gain, Energy resolution

Settings:

1: NCZ

Thickness 300um, 700 Ohm-cm

Depletion ~ 150um (back bias 100V)

2: NFZ

Thickness 500um, ~ 4 kOhm-cm

Depletion ~ 300um (back bias 100V)

3: DSOI(NCZ)

Thickness 300um, 700 Ohm-cm

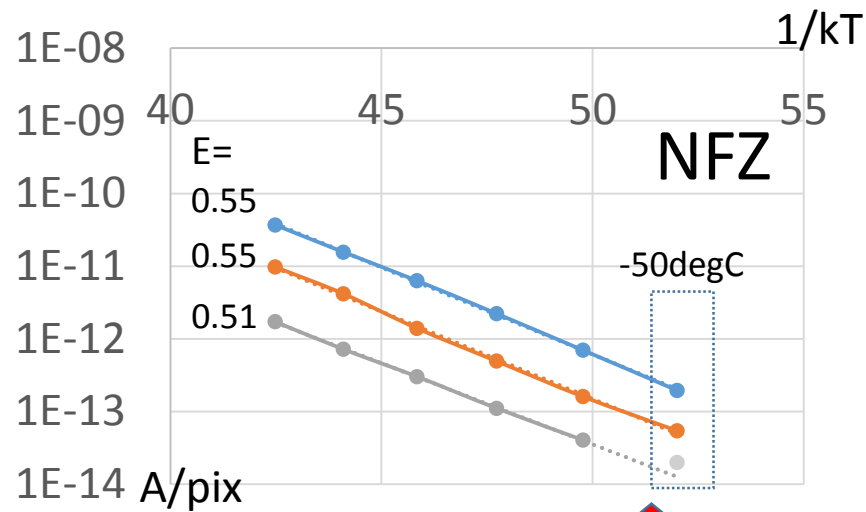
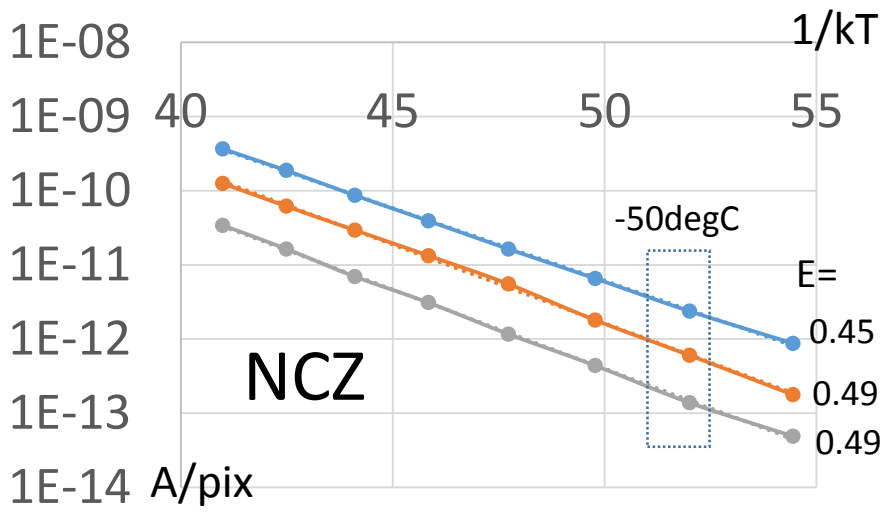
Depletion ~ 100um (back bias 60V)

Middle SOI floating

* Middle SOI floating or fixed to 0V → no difference in the sensor gain

Pixel leakage current

r1 --- r2 --- r3 ---

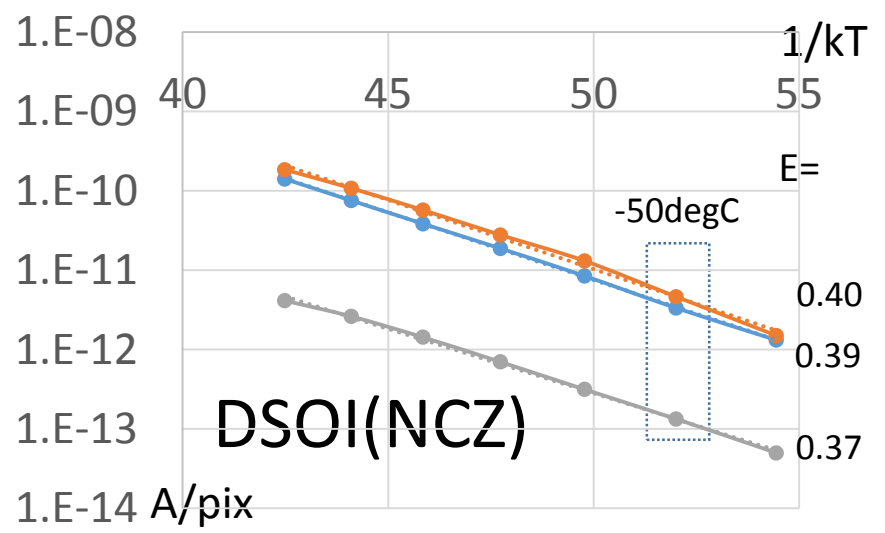


$EXP[-E \times (1/kT)]$

Arrhenius plot
 E Activation Energy (E_g (bandgap)/2=0.56(Si))
 $E \sim 0.56$; Generation current

NFZ $E \sim E_a$
 NCZ, DSOI $E < E_a$

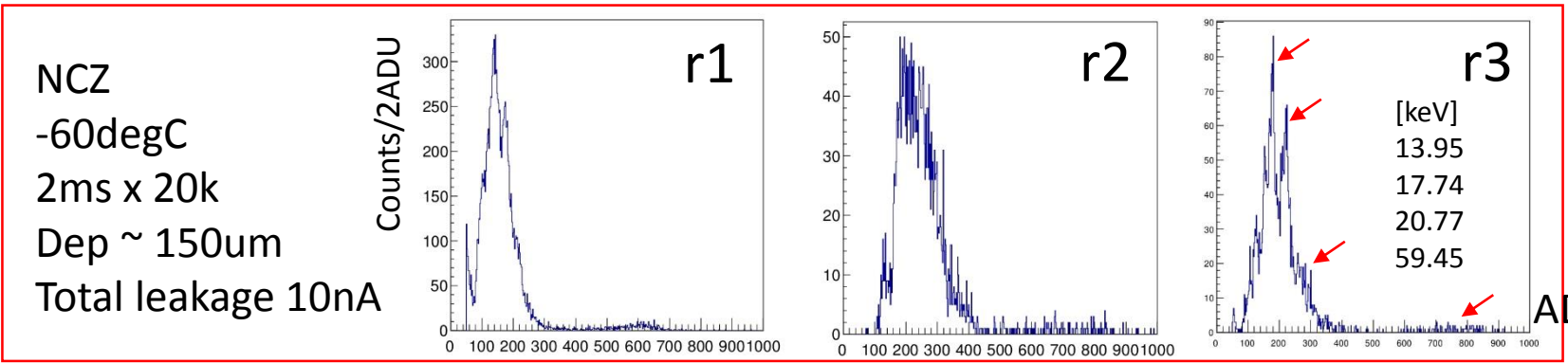
$I[NFZ]/pix \sim 10nA/cm2 @ -50deg.$



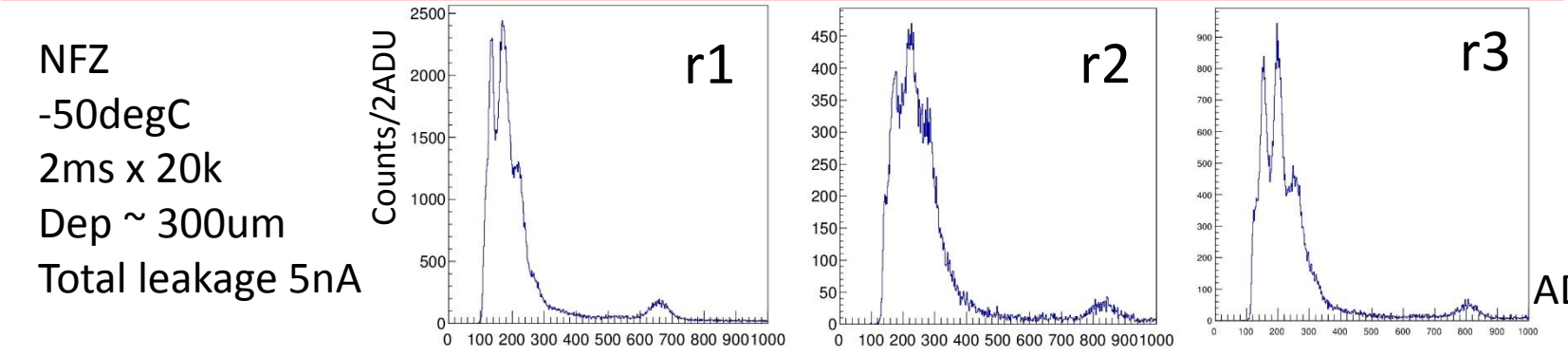
$10^{-13} \text{ A} / [\text{pixel} = 18 \text{ um} \times 18 \text{ um}] \times 3 \times 10^5 = 30 \text{ nA/cm}^2$

Am-241 spectrum

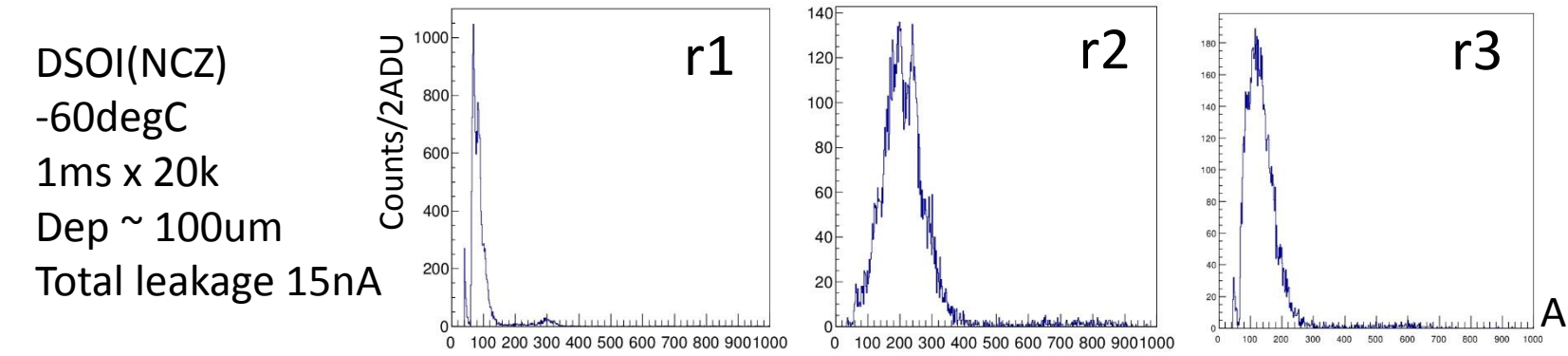
X:ADU, Y:Counts/2ADU



Memo:"a3"
Reset 400mV



Memo:"a2"
Reset 400mV



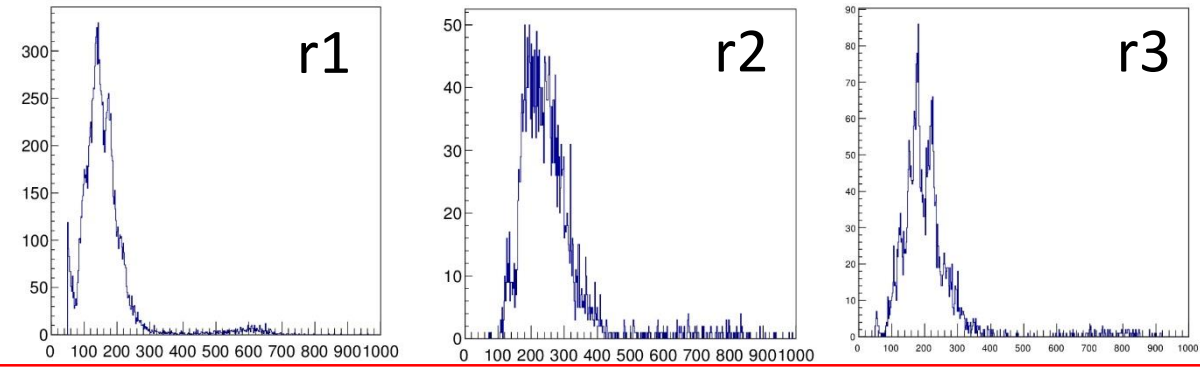
Memo:"a3"
Reset 400mV
BGonly

NCZ: Noisy (High leakage current), low efficiency

Am-241 spectrum

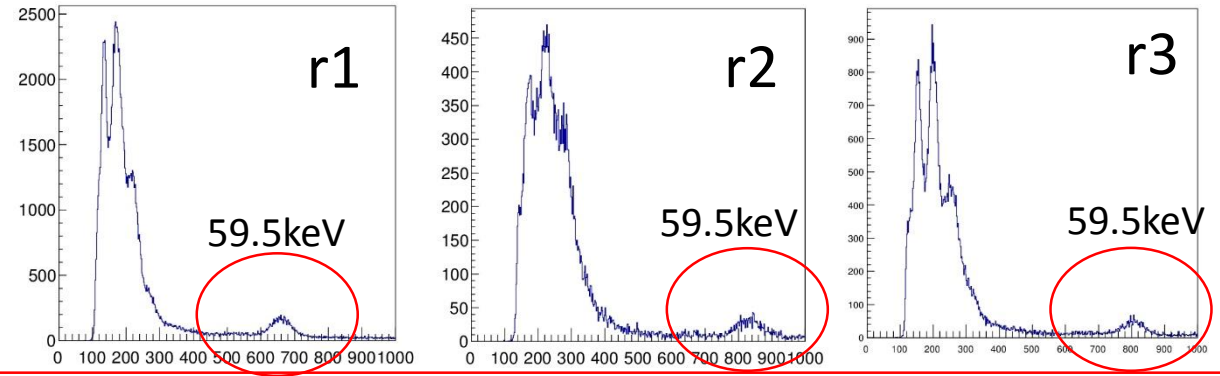
X:ADU, Y:Counts/2ADU

NCZ
 -60degC
 2ms x 20k
 Dep ~ 150um
 Total leakage 10nA



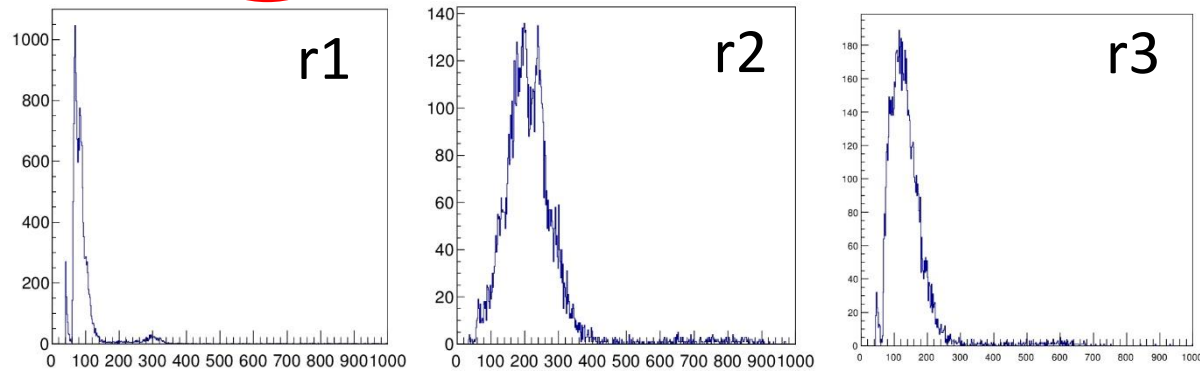
Memo:"a3"
 Reset 400mV

NFZ
 -50degC
 2ms x 20k
 Dep ~ 300um
 Total leakage 5nA



Memo:"a2"
 Reset 400mV

DSOI(NCZ)
 -60degC
 1ms x 20k
 Dep ~ 100um
 Total leakage 15nA



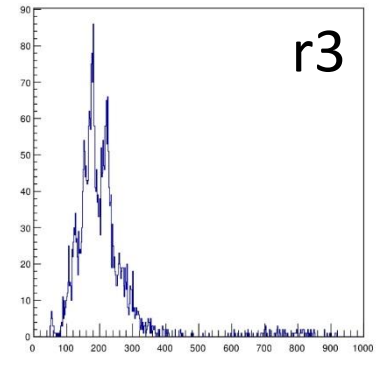
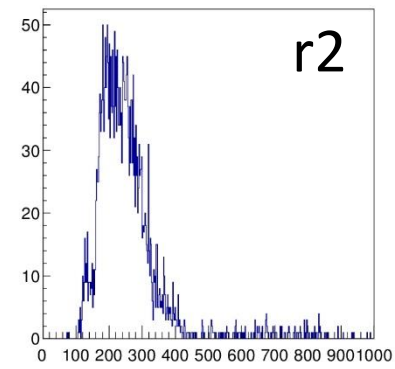
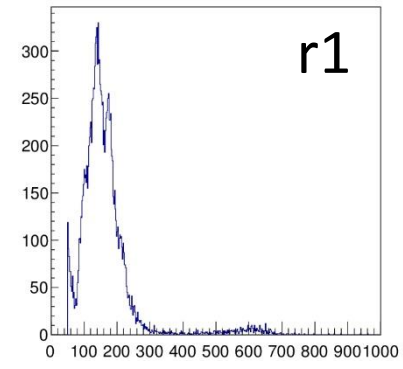
Memo:"a3"
 Reset 400mV
 BGonly

NFZ: Low noise (Low leakage current), High efficiency

Am-241 spectrum

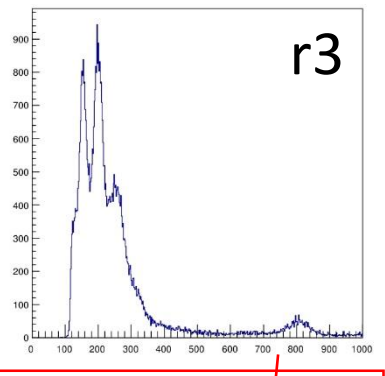
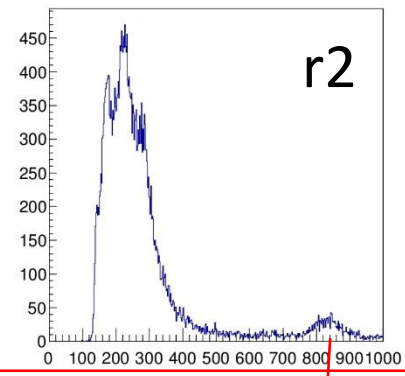
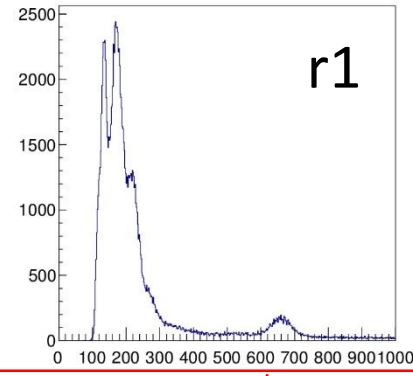
X:ADU, Y:Counts/2ADU

NCZ
 -60degC
 2ms x 20k
 Dep ~ 150um
 Total leakage 10nA



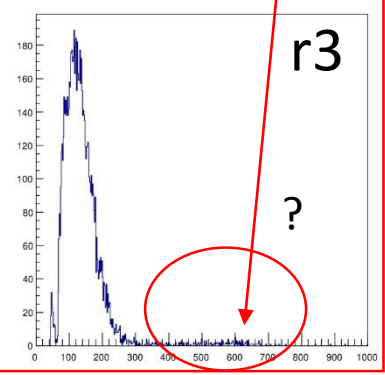
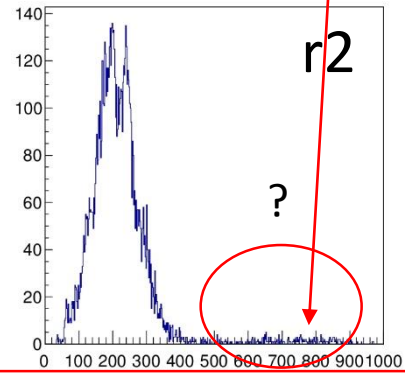
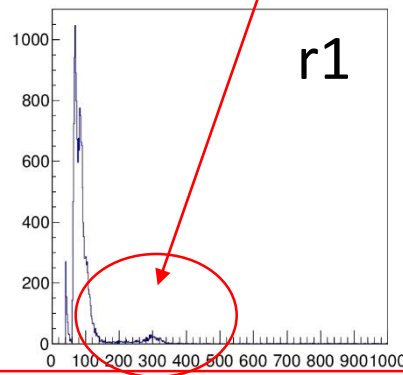
Memo:"a3"
 Reset 400mV

NFZ
 -50degC
 2ms x 20k
 Dep ~ 300um
 Total leakage 5nA



Memo:"a2"
 Reset 400mV

DSOI(NCZ)
 -60degC
 1ms x 20k
 Dep ~ 100um
 Total leakage 15nA

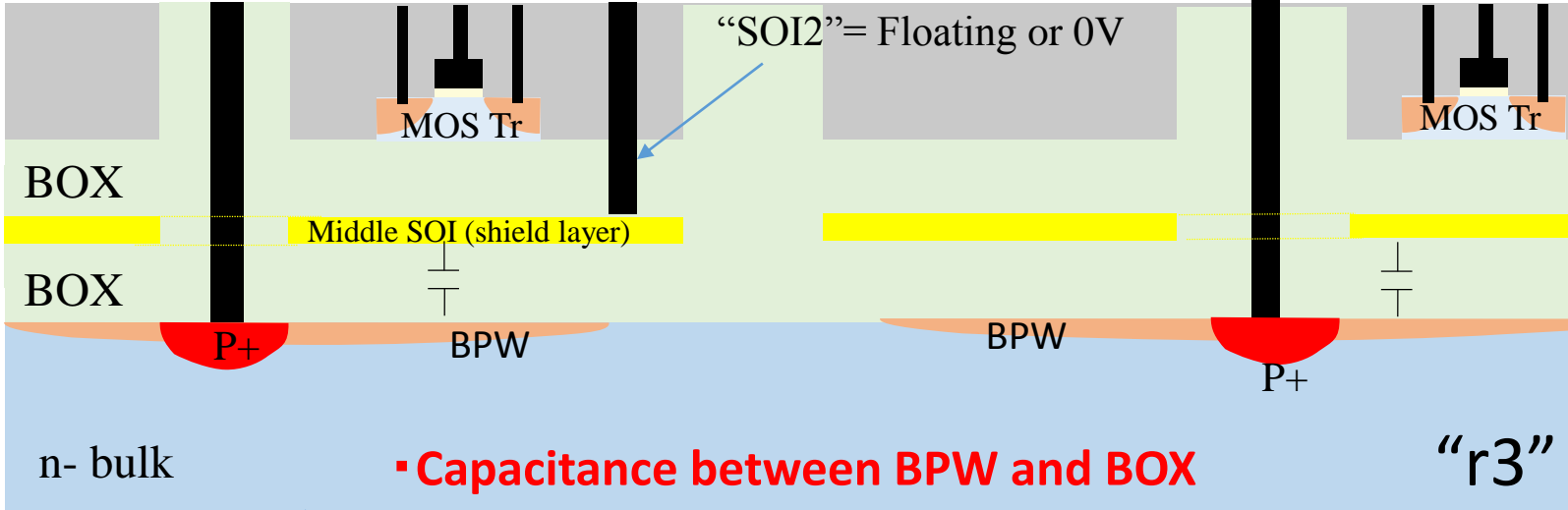


Memo:"a3"
 Reset 400mV
 BGonly

DSOI(NCZ): Noisy (High leakage current), Low efficiency,
 Low gain (Except Region 2)

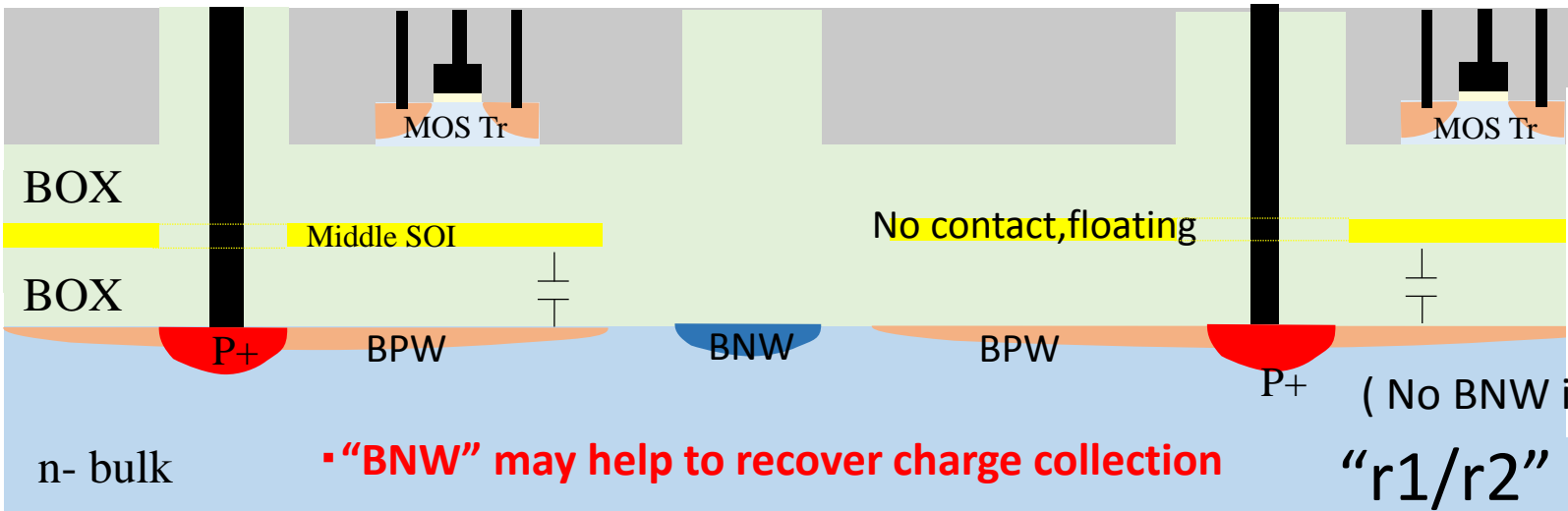
Why the gain is low?

Side view of Pixels



- Capacitance between BPW and BOX
- Charge doesn't go to p+

Back bias (60V) ↑



- “BNW” may help to recover charge collection

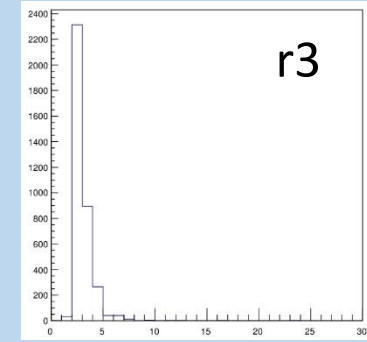
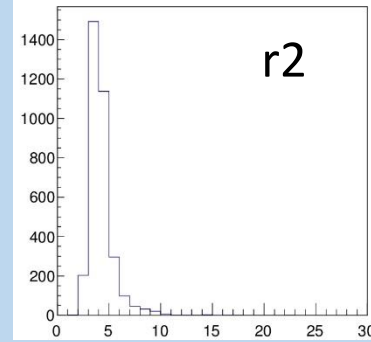
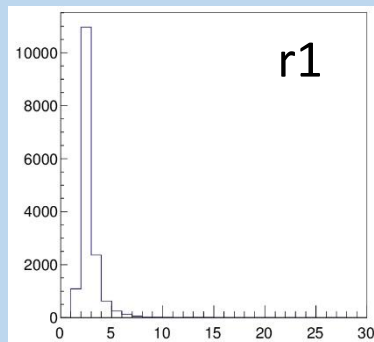
Back bias (60V) ↑

Cluster size distribution

X: cluster size Y:# of cluster

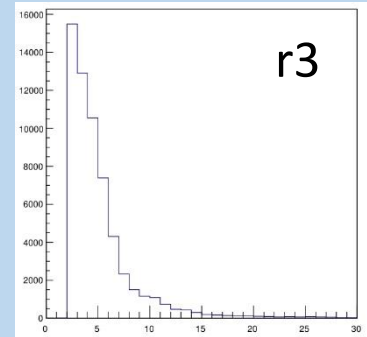
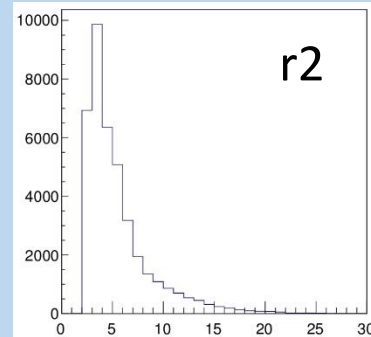
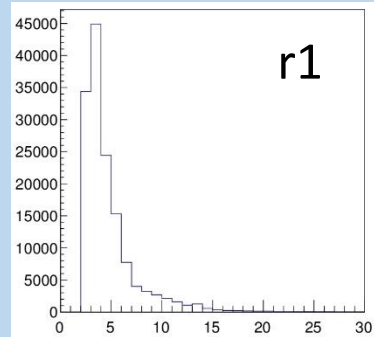
NCZ
(300um)

Depletion depth
~150um



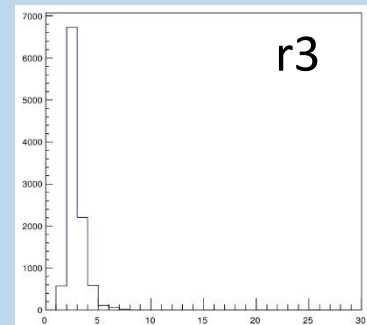
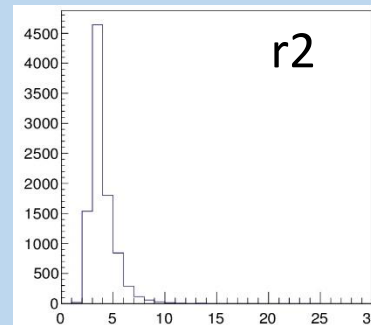
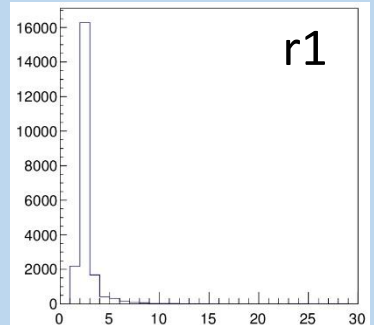
NFZ
(500um)

Depletion depth
~300um



DSOI
(300um)

Depletion depth
~100um

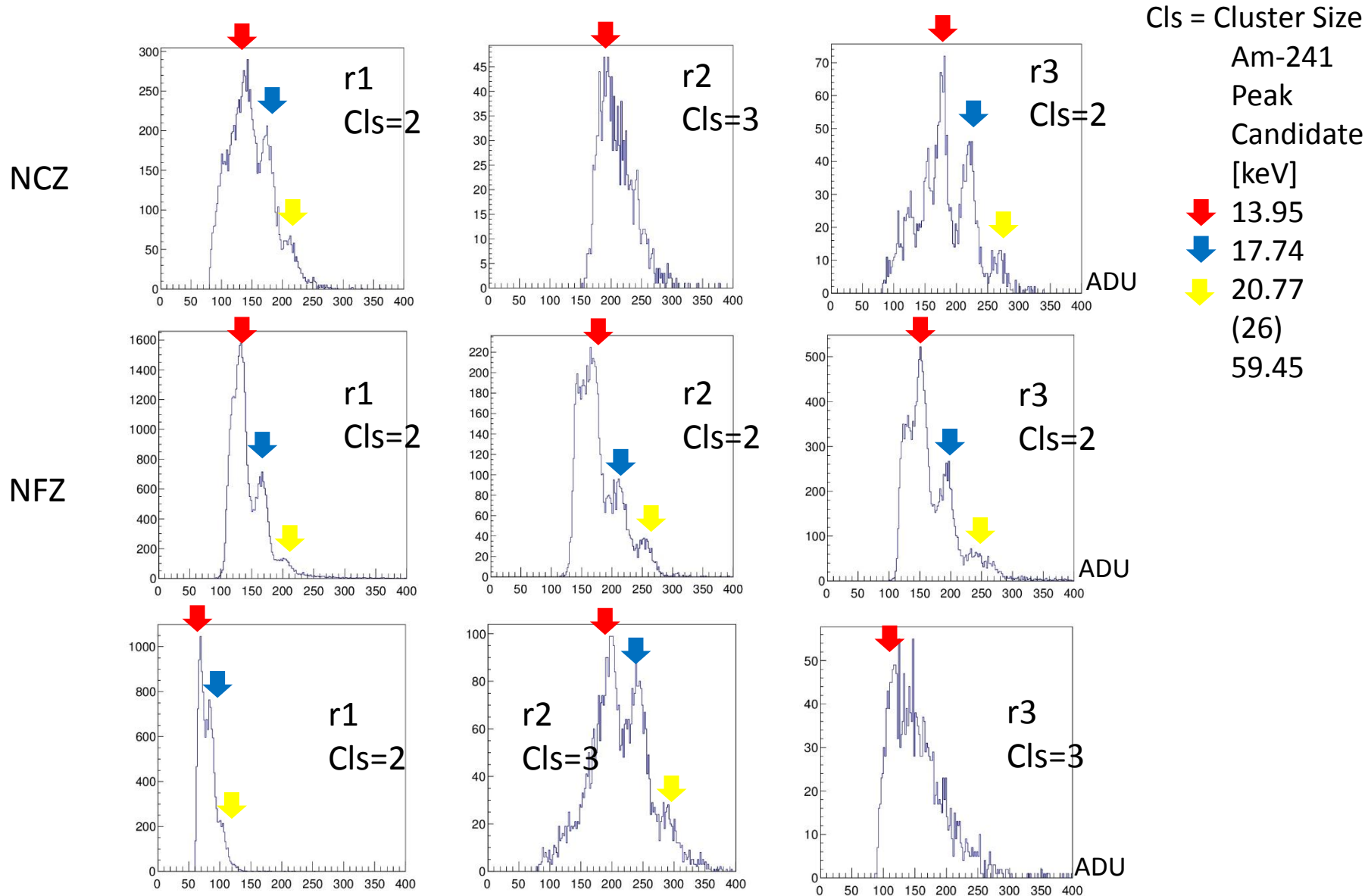


Peak: r1, r3 cluster size = 2

Peak: r2 cluster size = 3 (larger compared with r1&r3)

NFZ larger cluster size compared with NCZ&DSOI(NCZ)

Some X-ray spectra with selected cluster size



Each cluster plot was checked one by one, then the gain was evaluated.

Summary of source test (Am-241)

-50degC,2ms(NFZ)
 -60degC,2ms(NCZ)
 -60degC,1ms(DSOI)
 *Integration time

		r1	r2	r3
Gain NCZ	[uV/e-]	5.35	7.13	6.65
Gain NFZ	or	5.04	6.73	6.51
Gain DSOI	[mV/ke-]	2.45	7.09	4.70
E.Resolution NCZ	keV[FWHM] @13.95keV	4.07	4.95	1.93
E.Resolution NFZ		2.39	5.23	2.81
E.Resolution DSOI		4.03	7.80	14.5
Dark Noise NCZ	keV [FWHM]	1.39	2.29	0.62
Dark Noise NFZ		0.71	0.72	0.72
Dark Noise DSOI		1.29	0.84	1.21

E.Resolution=Energy Resolution

Sensor gain

- low for Double SOI sensor except region 2
- require BNW between pixels (or remove BPW? → to be studied)

Energy resolution

- NFZ r1&r3, NCZ r3 : good

Dark noise

- NFZ, NCZ r3, DSOI r2 : good

* Gain is not corrected in pixel by pixel

Summary

Double SOI sensor has successfully been fabricated

Breakdown voltage & Spatial resolution

seems to be the same as the case of single SOI with proper design

Difference in wafers;

- NCZ low R, low eff. with lower back bias V_b , high leakage current

- NFZ high R, high eff. with lower back bias V_b , low leakage current

DSOI(NCZ) low R, low eff. with lower back bias V_b , high leakage current,
partially low gain

DSOI(NCZ):

Charge collection issue

- Find better pixel structure

The 3rd trial: optimize pixel design with p-type DSOI sensors (2014 July)

Total Ionization Damage Compensations in Double Silicon-on-Insulator Pixel Sensors

S. Honda et al., 6/6/2014 14:00 - 14:20

Tomorrow!

SPRiT (SOI Portable Radiation imaging Terminal)

Thank you!

<http://rd.kek.jp/project/soi/>

Supplement

Future Plan

INTPIXh2 measurement

- NFZ-INTPIXh2 Am-241 spectrum @ -60degC
 - Cd-109 spectrum @ -60degC
 - DSOI-INTPIXh2 Am-241 spectra
- :Dependence of the middle SOI potential (-1V~+1V)
- KEK-PF monochromatic X-ray

New design for double SOI p-wafer (p-type sensor)

The 3rd trial will be completed hopefully in July

Optimize pixel structure

- Utilize BPW and/or BNW (nested structure etc...)
- Double SOI pixel without BPW (in-pixel)
- Separate mid.SOI(PMOS) with mid.SOI(NMOS)

Development of counting-type double SOI sensor

- Reduce sensor-circuit crosstalk

Some other plots...

Peak(59.5keV) is very useful

Cls = Cluster Size

Am-241

Peak

Candidate

[keV]

↓ 13.95

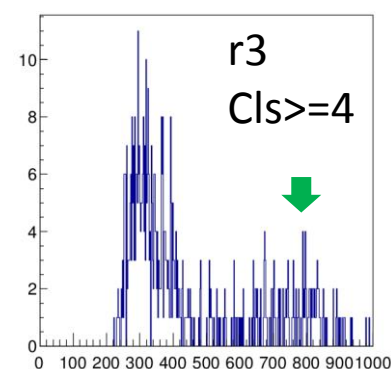
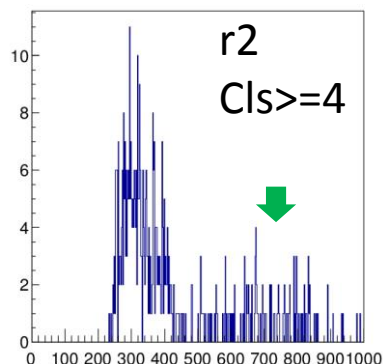
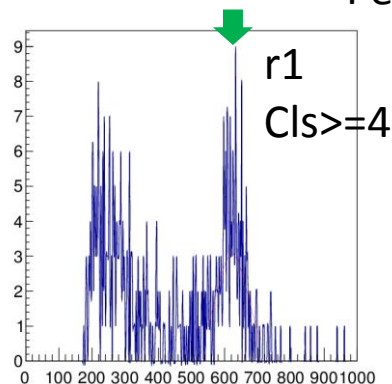
↓ 17.74

↓ 20.77

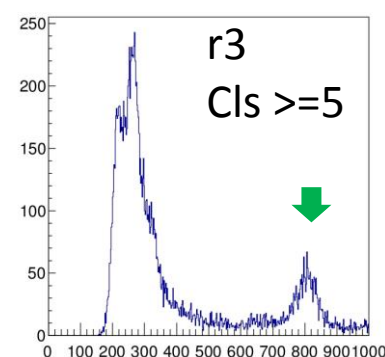
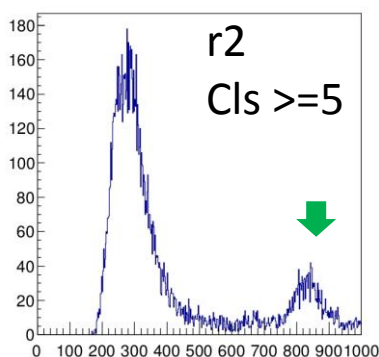
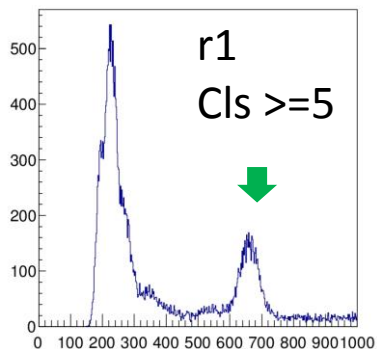
(26)

↓ 59.45

NCZ



NFZ



DSOI

