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## Monolithic pixel detectors fabricated with single and double SOI wafers

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Monolithic pixel detectors using 0.2  $\mu\text{m}$  FD-SOI pixel process have been developed since 2006. An SOI wafer is utilized for sensor and electronics. The top silicon is used for SOI-CMOS circuit, and the substrate is used for a radiation sensor. There is a buried oxide layer between two silicon materials, and these are connected each other through Tungsten via. SOI-CMOS circuit has smaller parasitic capacitance compared with bulk CMOS, and therefore high-speed, low noise and low power circuits can be fabricated. Since a bump bonding is not used, the sensors have high gain with smaller pixel size. Double SOI wafers are also available. In this case, the middle SOI layers are used for shield layer against the back-gate effect and cross talk. When the voltages are applied in the middle layer, the distribution of charge traps caused by radiation in the silicon oxide can be controlled which helps to enhance radiation tolerance. KEK has organized Multi Project Wafer (MPW) runs twice a year and several types of SOI detectors has been developed and evaluated using IR laser and radiation sources. We are also trying to solve existing problems such as sensor-circuit crosstalk and radiation hardness by utilizing double SOI wafers. In this presentation, evaluation test results of up-to-date SOI pixel detectors will be shown.

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