Development and test of a versatile DAQ system based on the ATCA standard

M.Bianco[a], P.J. Loesel[b], S. Martoiu[c], O. Sidiropoulou[a,d], A. Zibell[e]

[a] CERN
[b] Ludwig-Maximilians-Univ. Muenchen
[c] IFIN-HH Bucharest
[d] Aristotle University of Thessaloniki
[e] Bayerische Julius Max. Universitaet Wuerzburg
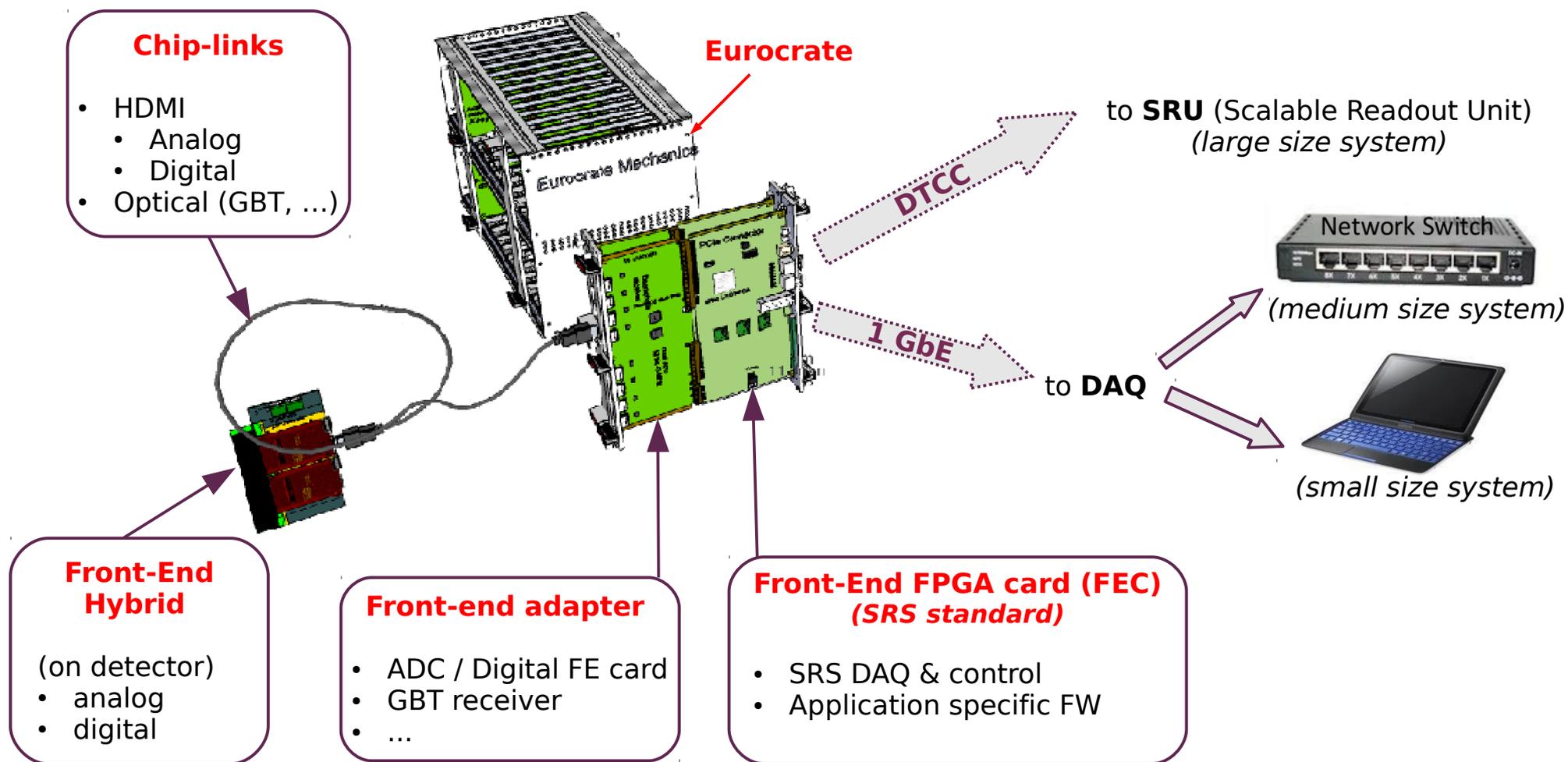
June 6, Amsterdam

Overview

- The Scalable Readout System (SRS)

  - Concept and layout

- Front-end hybrids used in the SRS system

  - APV25 (Analogue ASIC) and VMM2 (Analogue ASIC with digital transmission)

- Development of a SRS based on the ATCA format

  - A commercial framework for the SRS system

- Use of the SRS-ATCA system to readout:

  - Micromegas chambers in test stands

  - Micromegas quadruplet installed on one of the ATLAS Muon Small Wheels (summer 2014)

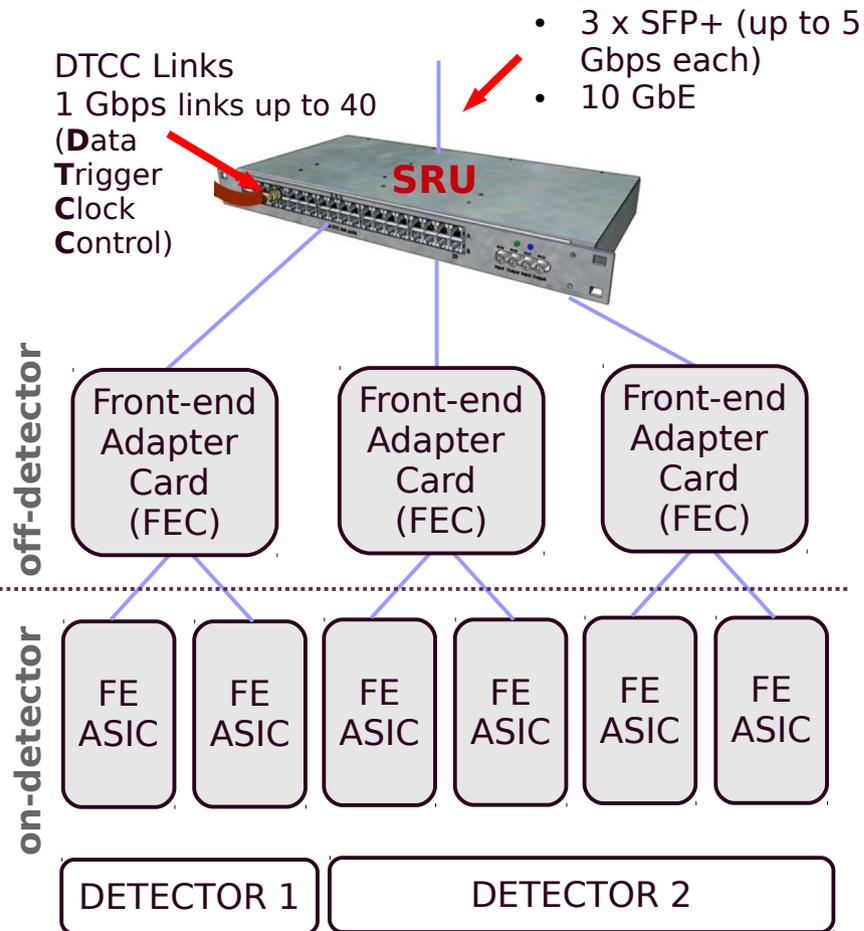- Conclusions

The Scalable Readout System

- Collective effort within the RD51 collaboration started for the R&D of the Micro-Pattern Gaseous Detector (MPGD) technologies and the associated readout electronics

- General purpose multichannel readout solution for a wide range of detector types, detector complexities (e.g. discharge protection) and different experimental environments

- Powerful and flexible platform for detector readout and control, based on Xilinx Virtex-5 and Virtex-6 FPGAs

- In the ATLAS Muon community it is used:

    - for Micromegas detector certification (small-medium sized labs and test beam setup)

    - to readout a Micromegas prototype (4096 channels), installed on to the present ATLAS Muon Small Wheel (summer 2014)

Classical SRS DAQ unit – Scalability Concept

Chip-links

- HDMI
  - Analog
  - Digital
- Optical (GBT, …)

Eurocrate

to **SRU** (Scalable Readout Unit)
(large size system)

DTCC

1 GbE

Network Switch

(medium size system)

to **DAQ**

(small size system)

Front-End Hybrid

(on detector)
- analog
- digital

Front-end adapter

- ADC / Digital FE card
- GBT receiver
- …

Front-End FPGA card (FEC)
(SRS standard)

- SRS DAQ & control
- Application specific FW

- Scalability to use different front-end hybrids - *APV25 (analogue) and VMM (digital transmission) commonly used* - and as many FEC cards as needed.

- The FE hybrids can be connected to SRS readout via a common interface, the FEC card

- Only point-to-point serial links (no buses) ➜ longer distance, more bandwidth

SRU for Large System Size

DTCC Links
1 Gbps links up to 40
(**D**ata
Trigger
Clock
Control)

off-detector

on-detector

- 3 x SFP+ (up to 5 Gbps each)
- 10 GbE

SRU

Front-end Adapter Card (FEC)

Front-end Adapter Card (FEC)

Front-end Adapter Card (FEC)

FE ASIC | FE ASIC | FE ASIC | FE ASIC | FE ASIC | FE ASIC

DETECTOR 1 | DETECTOR 2

SRU (Scalable Readout Unit)

➧ Readout cluster concentrator which aggregates both event and trigger data from up to 40 FEC card via DTCC links

➧ Xilink Virtex-6 FPGA-powered event building:
  - ➧ can act as a ReadOutDriver (ROD) to maintain data acquisition compatibility
  - ➧ Event data is buffered, formatted, optionally compressed and retransmitted via SFP+ ports

➧ For LHC applications, SRU has a TTCrx (Trigger, Timing and Control) receiver to pick up LHC clock (40MHz) and triggers (up to 100 kHz) via the TTC network of LHC experiments

Advantages of DTCC links over Ethernet

➧ Low (fixed) latency bidirectional channels for TTC info and trigger primitives

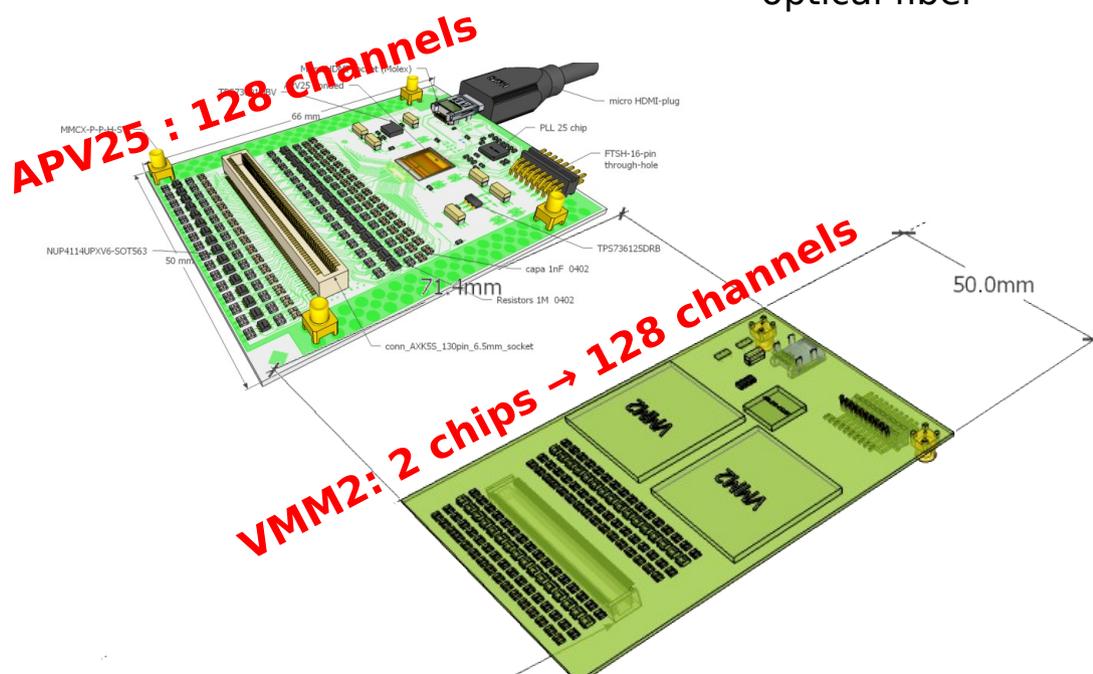➧ No data interference (e.g. all FECs talk at same time)

Possible front-end hybrids used in the SRS system

APV25

- Analogue pipeline ASIC
- 128 front-end channels
- Pipeline buffer of 192 cells depth for each input channel
  - filled consecutively with every clock cycle
  - Blocks of one or more pipeline columns can be read out for each trigger
- Spark-protected
- Powered via HDMI (2 chips master/slave powered and controlled by the same cable)

VMM2

- Analogue ASIC with digital output
- 64 front-end channels
- Provides charge and timing measurements along with:
  - The address of the first event in real time for trigger information
  - Time-over-Threshold measurements with zero suppression
- Spark-protected
- Preliminary version readout by HDMI cable, later via optical fiber

Advanced Telecommunications Computing Architecture:

- A modern standard originated from telecom industry based on high bandwidth switched fabric technology
- Adopted to replace VME off-detector equipment in LHC experiments

Advantages with respect to standard SRS

- Certification (mechanical, electrical e.t.c)
- High integration of electronic components
- Higher channel density / Reduced cost for F.E. Readout channels
- High data bandwidth on full mesh switched fabric (> 10 Gbps/fabric channel)
- In-built remote management and diagnostic (IPMC) (power, temperature, cooling, alarms, etc)
- No external cables (maintenance, assembly)

Moving from classic SRS to ATCA SRS

SRS in Eurocrate

SRS Eurocrate
- Up to 8 FECs/crate
- Up to 8 HDMI/FEC
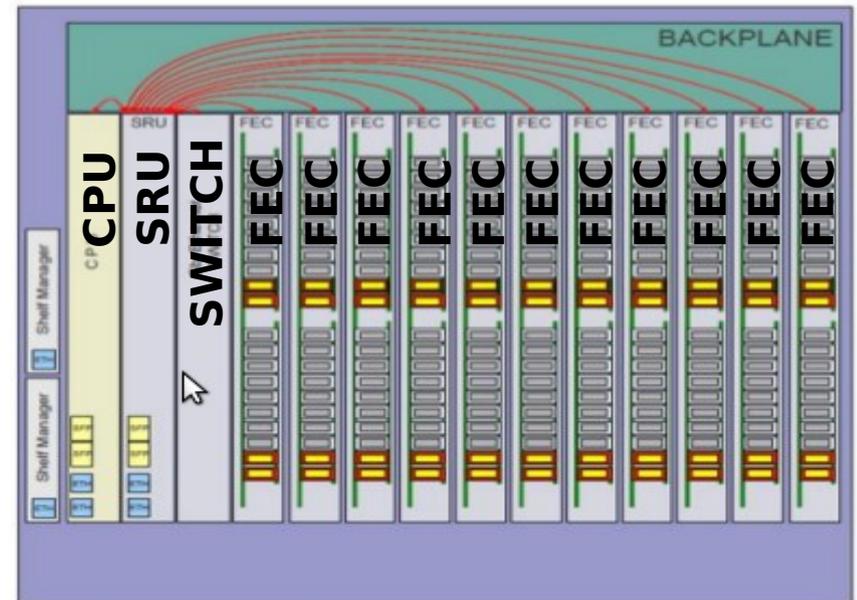- Up to 16k channels/crate

Rack System
- Up to 5 crates/**82k** channels
- **1 SRU/rack** for parallel FEC readout with 40 DTCC links

ATCA - SRS

shelf = crate
blade = module

- 11 FEC-ATCA blades
- 1 SRU blade in the self
- **67k** channels per self
- Point-to-point (multi-) gigabit link between FEC and SRU boards (DTCC speed can reach 10Gbps and more)

+ 2 FEC-ATCA if no CPU & Switch

- Possible to readout up to 20 FEC Blades using an external SRU
  - Channels can be increased to **128k**
  - Speed limited to 1 Gbps

ATCA SRS for analogue (APV25) front-end chip
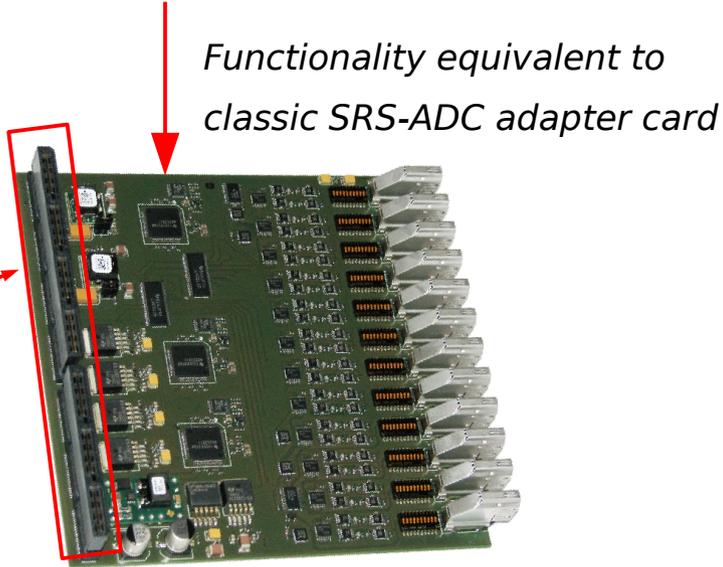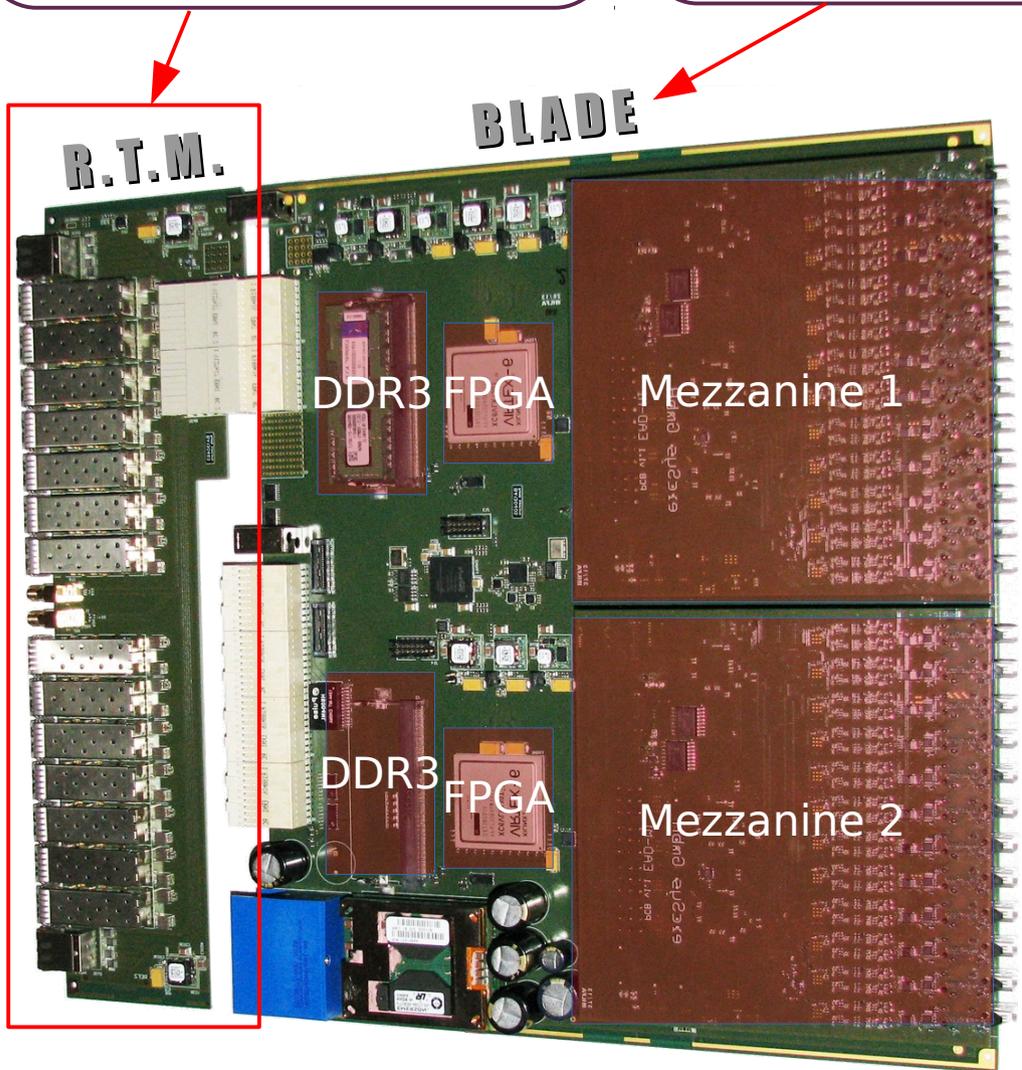
**Rear Transition Module (RTM)
I/O extension card**

- 2 x 7 SFP+
  (up tp 5Gbps at the moment)
- 2 x Rj45 (DTCC)
- 2 x NIM (LEMO 00)

Blade main board

- 2 x Virtex-6 FPGA
- 2 x DDR3 up to 4GB
- 2 x Mezzanine ports
  (work independently)
- → *The 2 FPGAs can also be
  interconnected*

ADC HDMI Mezzanine

- 12 x HDMI ports (cable length
  selection)
- 24 channel 12-bit ADC card
- CLK & TRG distribution to
  front-ends via HDMI

R.T.M.

BLADE

DDR3 FPGA

Mezzanine 1

DDR3 FPGA

Mezzanine 2

Samtec
QTE/QSE
connector

Functionality equivalent to

classic SRS-ADC adapter card

ATCA-FEC vs FEC-SRS:

- → ~ 3x in logic resources
- → ~ 5x in memory
- → ~ 2x in performance (speed)

Integration of VMM2 (HDMI output) into ATCA SRS

1) Using Optical Converter (OC) box and connect the optical cables to the SFP+ ports on the RTM
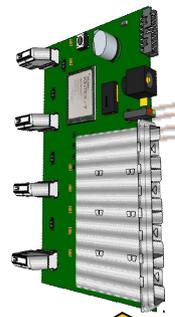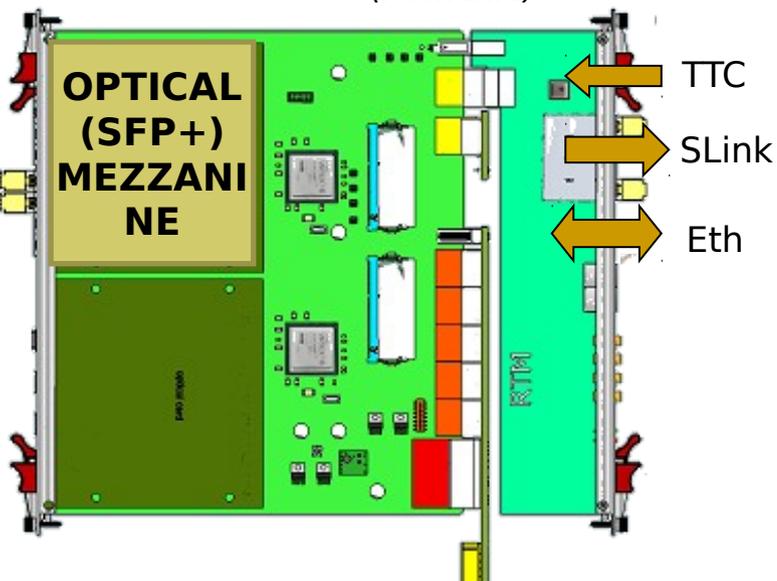
Under design at CERN

HDMI cables

Compatible with classic SRS
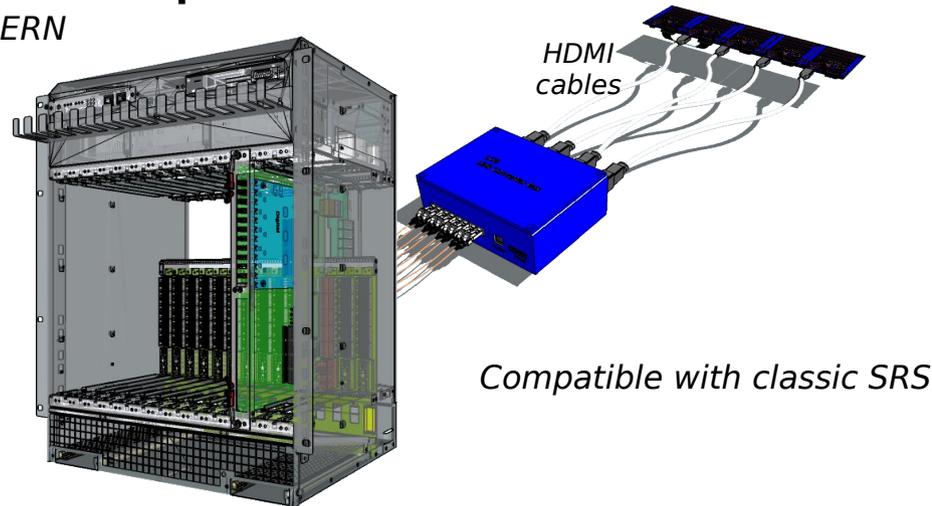
2) Using an Optical Mezzanine

Under design at IFIN-HH (Romania)

Concentrator (optical I/F)

OPTICAL (SFP+) MEZZANINE

TTC

SLink

Eth

POWER

3) Using a Digital-HDMI Mezzanine

Under design at UPV (Spain)
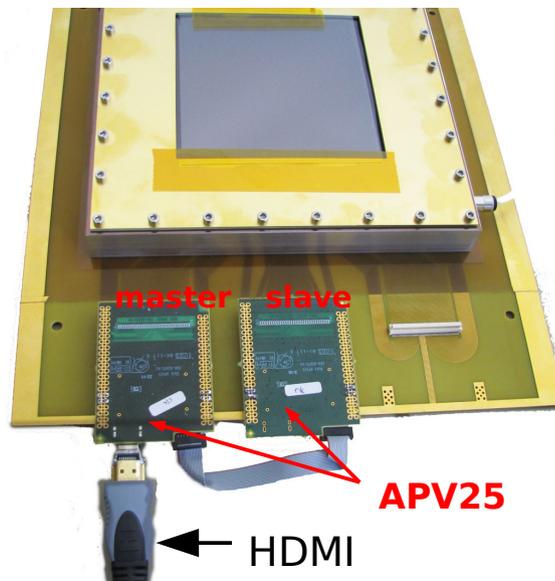
DIGITAL-HDMI MEZZANINE

TTC

SLink

Eth
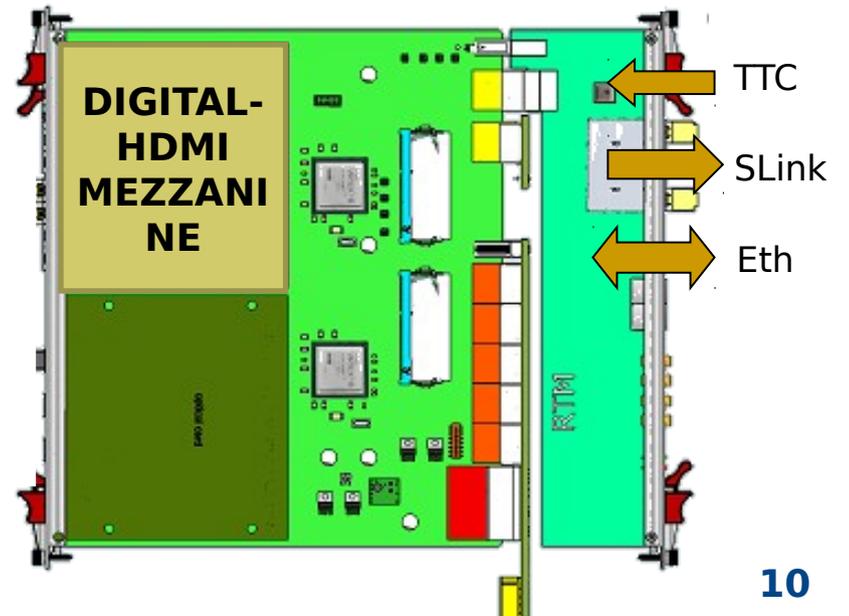
Test stand at CERN RD51 lab

- ATCA crate, with new FEC Blade (with the ADC HDMI mezzanine) and standard SRS crates with old ADC/FEC version hosted in the same rack (left)
- Cosmic stand able to host several Micromegas test chambers (right)

→ **Analogue front-end chips (APV25) used in both readout technologies**

Cosmic stand with Micromegas chambers

2 slot ATCA self

SRS Mini crate

SRS Eurocrate

master   slave

APV25

HDMI

MMDAQ: a Micromegas software for SRS ATCA system

➔ **During the design of the MMDAQ no assumptions were taken on electronics type or readout configuration.**

- **Any combination of data sources (APV25 or VMM Chips, FEC, SRU)**

    - (multi-threading, dynamic dispatch)

- **Event building on available variables**

    - (Trigger Number, SRS Time Stamp)

- **Client - Server and detached GUI**

    - (by interprocess communication)

- **Scalability**

    - (multi-threading, data buffering design limiting locking)

- **System configuration using XML**

MMDAQ: a Micromegas software for SRS ATCA system

MMDAQ Graphical User Interface (GUI)

- Fully configurable system through the GUI
- Online monitoring to check main detector and electronics property during the run
  - Monitoring available at channel level
- Same software used for fast offline check
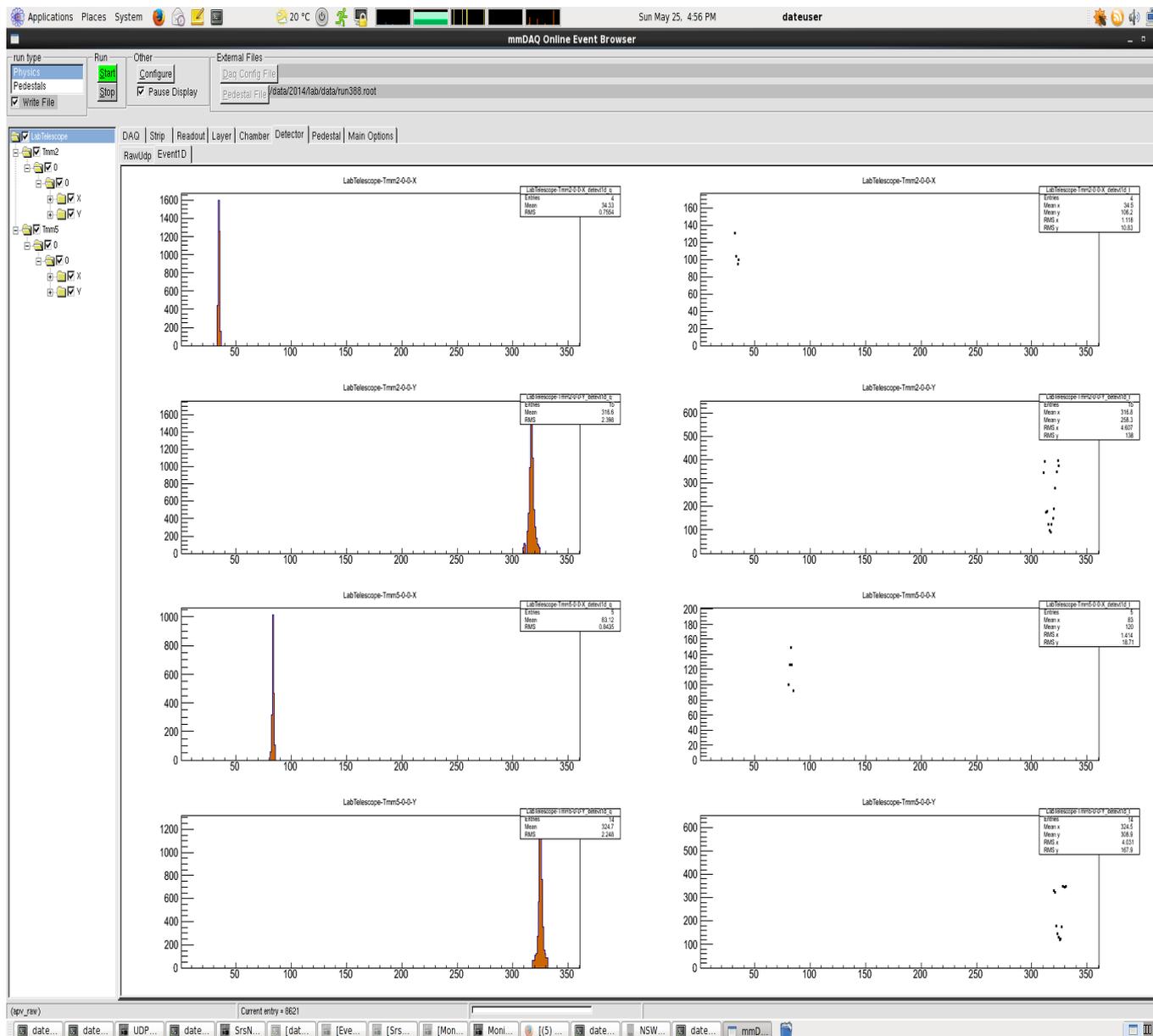
Integration of a Micromegas (MM) quadruplet into the ATLAS DAQ system

Detector specifications

- MM quadruplet with an active area of 0.5 m^2/layer
- 1024 channels/layer → **4096 channels** in total
- 16 VMM2/layer → 64 hybrids in total

DAQ System

- 1 ATCA shelf with 1 ATCA blade
- 1 standard SRU as ROD, to generate valid event fragments
- Data transmitted to a Read Out System (ROS) using standard read-out link (S-Link)
- ATLAS Run Control used for configuration and system control

DAQ Software

- A Micromegas segment has been implemented using the ATLAS Online TDAQ Software in order to be attached to the main ATLAS DAQ partition

ROS
S-Link
TTC signals
Configuration
slow control
SRU
DTC links
VMM2
OC box
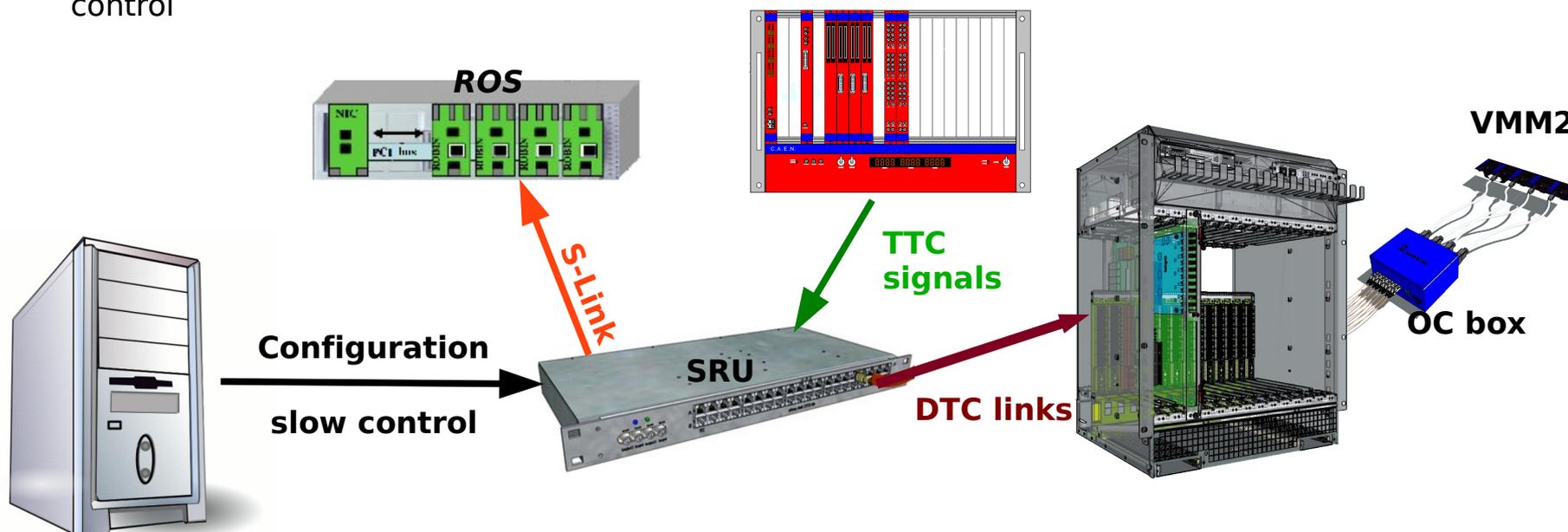
Conclusions

- The SRS DAQ system developed inside RD51 community has been moved from classic SRS (Eurocrate format) to standard ATCA technology

- All the electronics components (ADC, FEC) have been adapted and upgraded to the ATCA layout

- A dedicated software (MMDAQ) to readout the SRS system at small-medium size test stands and beam tests has been developed

- A dedicated test setup has been built inside the RD51 lab for the integration of the Micromegas quadruplet into the full ATLAS readout chain in summer 2014

Thank you!