Test for the mitigation of the Single Event Upset for ASIC in 130 nm technology

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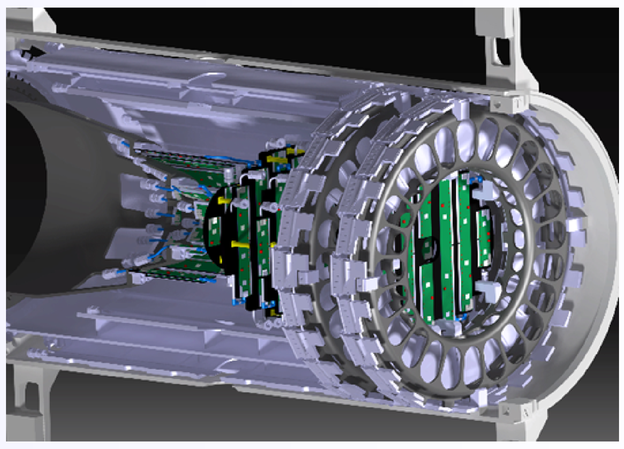
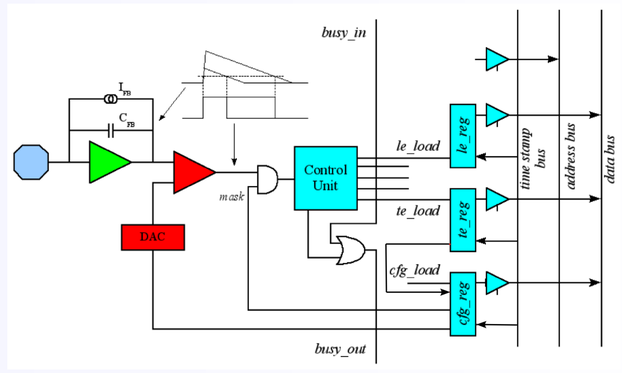
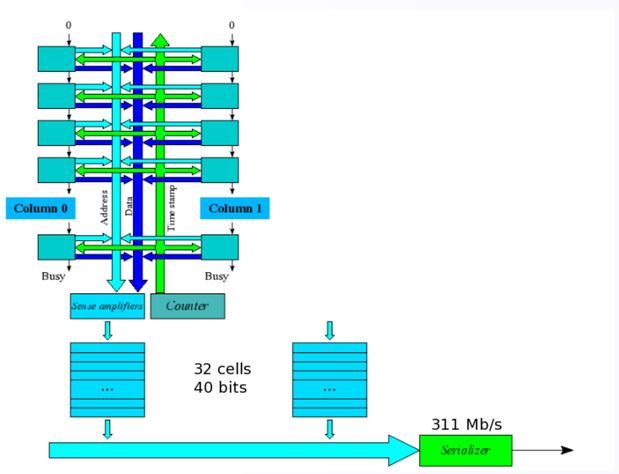
The antiProton ANnihilation at DArmstadt ($\overline{P}$ANDA) is a new experiment under development, with fixed target layout. It exploits the antiproton beam that will be available at the Facility for Antiproton and Ion Research (Fair). The Micro Vertex Detector (MVD) is at few centimetres from the interaction point, and it is composed of 4 coaxial barrels, and 6 forward disks. Pixels were chosen for the internal layers to cope with the high event rate, while strips for the external ones to cover large areas. A 100 kGy TID and a 1 MeV equivalent neutron fluence of 10^{14} n/cm^2 is expected, in 10 years lifetime with a 50 % duty cycle. The front end electronics allows to acquire information as the position, time and energy of the incoming particle.

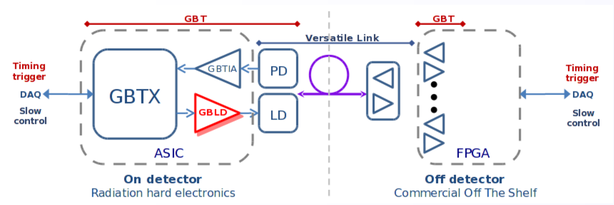


The readout electronics for the pixel sensor is a custom project, called Topix, in a 130 nm CMOS technology. The size of the pixel is 100 × 100 μm^2 and contains the analogue section with the amplifier, and the digital part with registers. There is a couple of 12 bit registers to store the leading and trailing edges, which define the TOT. Then there is an 8 bit configuration register for the pixel setting, as the local threshold, the masking and others controls. The device under test was a reduced scale prototype with 640 cell instead of 12.8 × 10^3 cell, as in the final ASIC. Due to the limited area, the registers are implemented with latches. They are protected against the Single Event Upset (SEU), by the Triple Modular Redundancy (TMR).



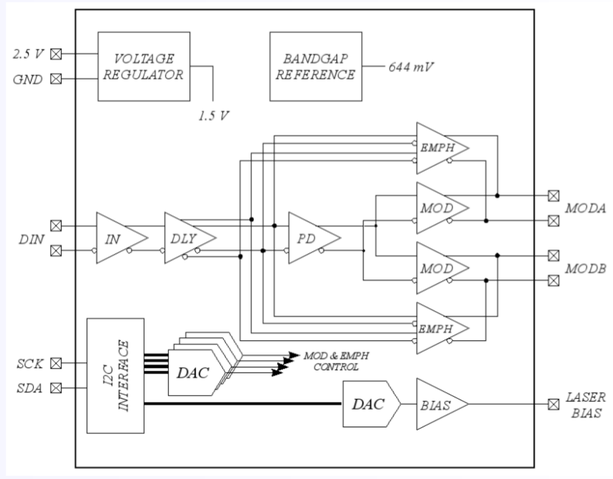


In Topix the pixels are organized in columns, with some electronics to store the events before the serialization. The present design foresees 110 column, each one arranging 116 cell. To save room on the layout, the same bus serves two adjacent columns transferring data towards the output FIFO. These end of column structures are made of 32 word, each one 40 bit long. The stored information are the time stamps for the leading and the trailing edges, and the hit pixel address. In this region the SEU protection is implemented by the Hamming code, that allows the detection and correction of one bit error. At present, a failure may only happen when 3 bit flip in the same word.

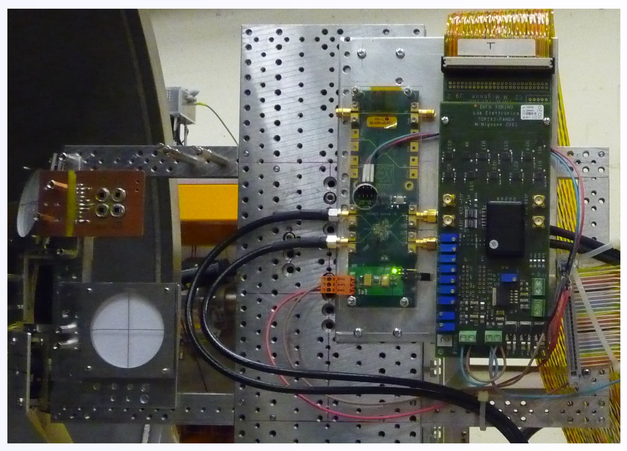


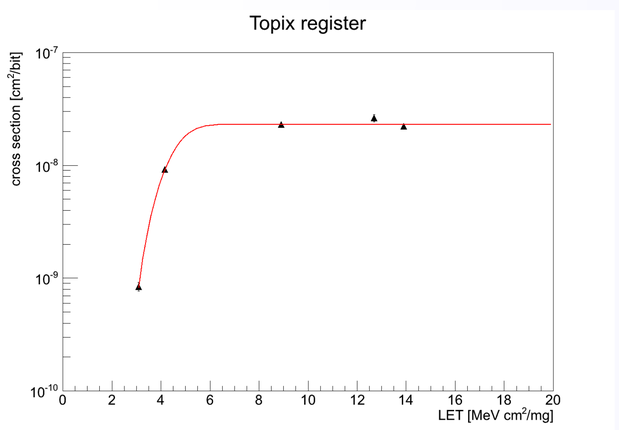
The GBT chip set is a large project, developed at CERN, for the data transmission. It is envisaged for the next generation experiments, working with a high luminosity beam. The aim is to provide a bidirectional serial link for data acquisition and slow control, which is able to work in a radiation environment. The activity foresees also the development of the electronics on the other end of the optical fibre, typically implemented on an FPGA. The INFN Torino department was involved in the design of the GigaBit Laser Driver (GBLD), to control the laser diodes. This chip set represent the current solution, for the MVD, to send the data towards the counting room.

The GBLD circuit is made in a 130 nm CMOS technology, as well Topix. It features a data rate up to 5 Gb/s, and the capability to drive both VCSEL and EEL diodes. To manage a high capacitive load, a pre emphasis circuit is available. The bias and modulation setting, can be done via an I^{2}C interface. The configuration is stored in 7 register 8 bit wide implemented with D type flip flops, and the SEU protection is performed by the TMR. Due to power consumption optimization, two versions has been designed and tested. They differ also for the metal stack: v4 used 8 metal layers, while v5 employed 9 metal layers.

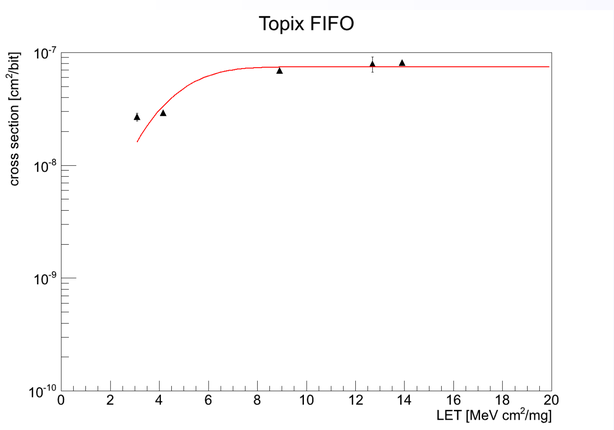


The SEU measurements were performed at the Sirad facility, in the INFN Legnaro Laboratory. Several ions at different energies are available, to test the devices placed in a vacuum chamber. The facility provides also a system for the evaluation of the dosimetry, performed acquiring the flux and the fluence with monitoring diodes. The measurements were accomplished with ions in the range from O at 101 MeV, up to Cl at 197 MeV. The device was set in a working state and checked every 2 s, when an error occurs it is counted and the circuit is configured again.



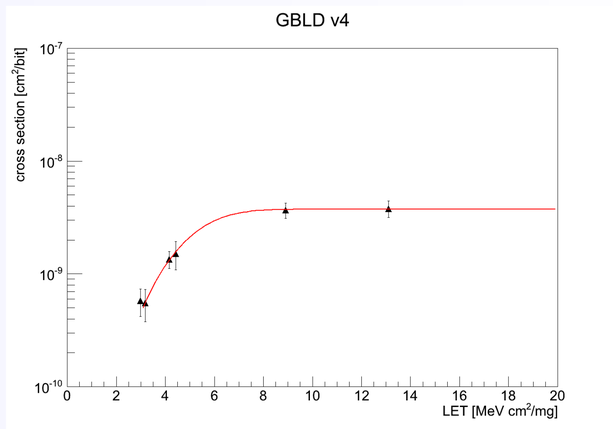


From the ratio, between the errors and the incident ions, the frequency of the upset can be evaluated. Normalizing these ones, to the number of bits for the configuration registers in the Topix prototype (5.12 × 10^3), the cross section can be estimated. The points are fitted with a Weibull function, that is currently used to model this quantity. For the Topix configuration register, a saturated cross section of about 2 × 10^{-8} cm^2/bit is obtained. This structure, protected with TMR, becomes sensitive to the upset above a LET of 2 MeV cm^2/mg.



Since the prototype under test contains only 4 columns with output FIFO, the related number of bit to use in the normalization is again 5.12 × 10^3. In that case the saturated cross section for the output FIFO buffer, protected with Hamming code, is roughly 7 × 10^{-8} cm^2/bit. The threshold, where the upset effect becomes evident, is around a LET of 1 MeV cm^2/mg. The comparison, from Topix configuration register, shows that the TMR protection looks more effective than the Hamming code.

For the circuit GBLD v4, which is able to drive VCSEL and EEL, the total number of bits dedicated to the storing of the configuration is 56. The layout featuring 8 metal layers is the same of the final ASIC, and foresees D type flip flop. The measurement for the structure, protected with TMR, shows a saturated cross section of around 4 × 10^{-9} cm^2/bit. Regarding the threshold, the upset effect starts to arise for a LET of about 2 MeV cm^2/mg.



The GBLD v5 is the low power version, designed for driving the VCSEL. The circuit has a similar interface composed of 56 bit, but with 9 metal layers. The register structure, protected again with TMR, has a saturated cross section of 3 × 10^{-9} cm^2/bit. The upset threshold is at a LET of around 2 MeV cm^2/mg, as for the GBLD v4. Since the circuits are similar, the lower cross section is due to the thicker metal stack.