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## Test for the mitigation of the Single Event Upset for ASIC in 130 nm technology

The Micro Vertex Detector (MVD) is the innermost sensitive layer of the PANDA experiment at the new Facility for Antiproton and Ion Research (Fair). The MVD will be composed of two kind of sensors: hybrid pixels and double sided strips. The front end electronics of the MVD will be placed at a few centimetres from the interaction point, where high radiation levels are expected. Therefore the ASIC have to be designed with radiation tolerant techniques, both in terms of Total Ionizing Dose (TID) and Single Event Upset (SEU). The TID issue has been addressed using a sub micron technology as the CMOS 130 nm, which has proven an intrinsic good tolerance to radiation damage. On the other hand these technologies are very sensitive to SEU, due to the reduced size of the active devices. Therefore SEU mitigation techniques have to be applied at circuit level, in order to prevent data corruption and failure of the control logic. Various architectures and techniques are proposed in literature, which essentially show a trade off between protection level and area penalty. Some of these techniques have been implemented in the prototypes for the readout of MVD pixel sensors, based on space constraints. The prototypes have been then tested at the Legnaro INFN facility with ions of various species, in order to asses the effective capability of SEU mitigation. The obtained results have shown some limitation in the implementation of these techniques, which will serve as a guideline for the design of the final ASIC.

### Summary

The Micro Vertex Detector (MVD) is the innermost sensitive layer of the PANDA experiment at the new Facility for Antiproton and Ion Research (Fair) in Darmstadt. The MVD will be composed of two kind of sensors: hybrid pixels and double sided strips. The front end electronics of the MVD will be placed at a few centimetres from the interaction point, which is constituted by a fixed target, where high radiation levels are expected. Therefore the ASIC have to be designed with radiation tolerant techniques, both in terms of Total Ionizing Dose (TID) and of Single Event Upset (SEU). The TID issue has been addressed using a deep sub micron technology as the CMOS 130 nm, which has proven an intrinsic good tolerance to radiation induced damage. On the other hand these technologies have increased their sensitivity to SEU, due to the reduced size of the active devices. Therefore SEU mitigation techniques have to be applied at circuit level, in order to prevent data corruption in the registers and failure of the control logic. Various architectures and techniques are proposed in literature, which essentially show a trade off between protection level and area penalty. Some of these techniques have been implemented in the circuit prototypes for the readout of the MVD pixel sensors, based on the space

constraints. The prototypes have been then tested at the Legnaro INFN facility with ions of various species and energies, in order to assess the effective capability of SEU mitigation. The obtained results have shown some limitation in the implementation of these techniques, which will be used as a guideline for the design of the final ASIC.

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