The CERN NA62 experiment: Trigger and Data Acquisition

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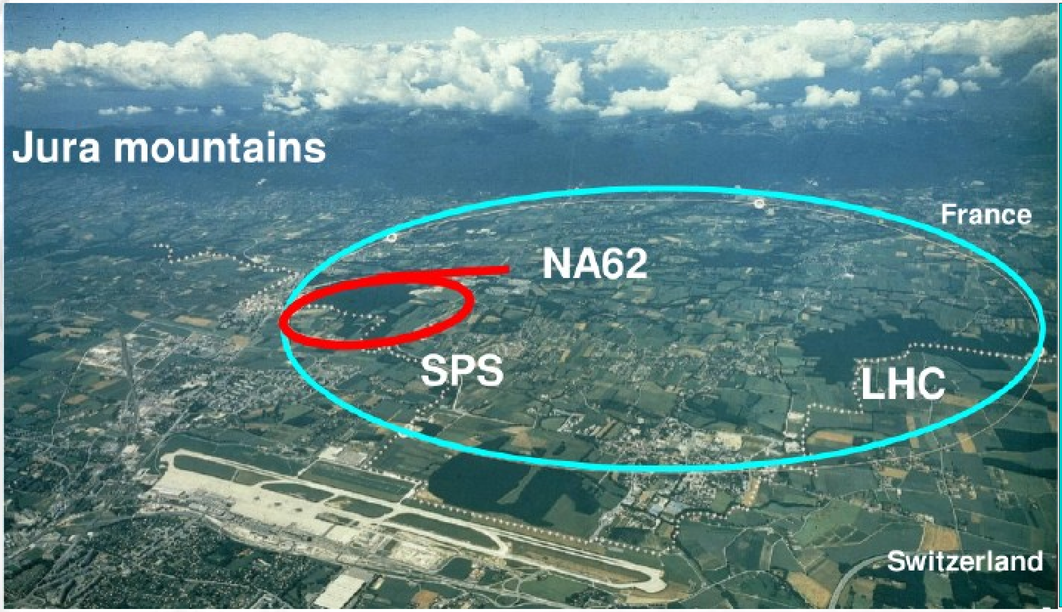
Outline

- The NA62 experiment
- The NA62 TDAQ system
  - TEL62 board
  - TDCB
  - Trigger Distribution
  - LKr trigger system
  - Gigatracker readout

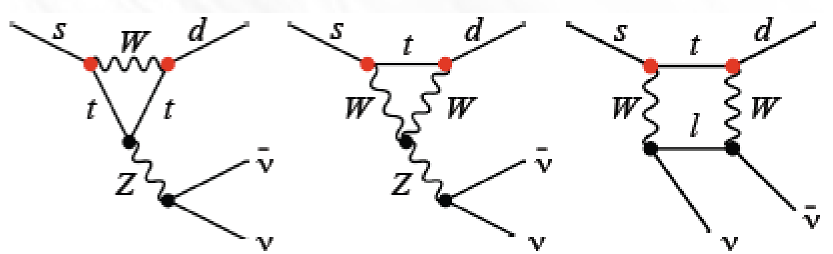
The NA62 experiment



NA62 main goal:
measure the BR of an ultra-rare FCNC process with 10% accuracy to test the standard model and search for new physics. This can be achieved collecting O(100) events in 2 years of data taking.

The process offers an highly sensitive test of the Standard Model

- SM Prediction: $BR(K^+ \rightarrow \pi^+ \nu \bar{\nu}) = (0.781 \pm 0.075 \pm 0.029) \text{x} 10^{-10}$
  Brod Gorbahn Stamou PRD 83 (2011) 034030
- Experimental result: $BR(K^+ \rightarrow \pi^+ \nu \bar{\nu}) = (1.73 + 1.15 - 1.05) \text{x} 10^{-10}$
  E787/E949, Phys.Rev.Lett. 101, 191082 (2008)



$K^+ \rightarrow \pi^+ \nu \bar{\nu}$: Main Backgrounds

$K^+ \rightarrow \pi^+ \nu \bar{\nu}$ signature:
Kaon track +
Pion track +
NOTHING ELSE

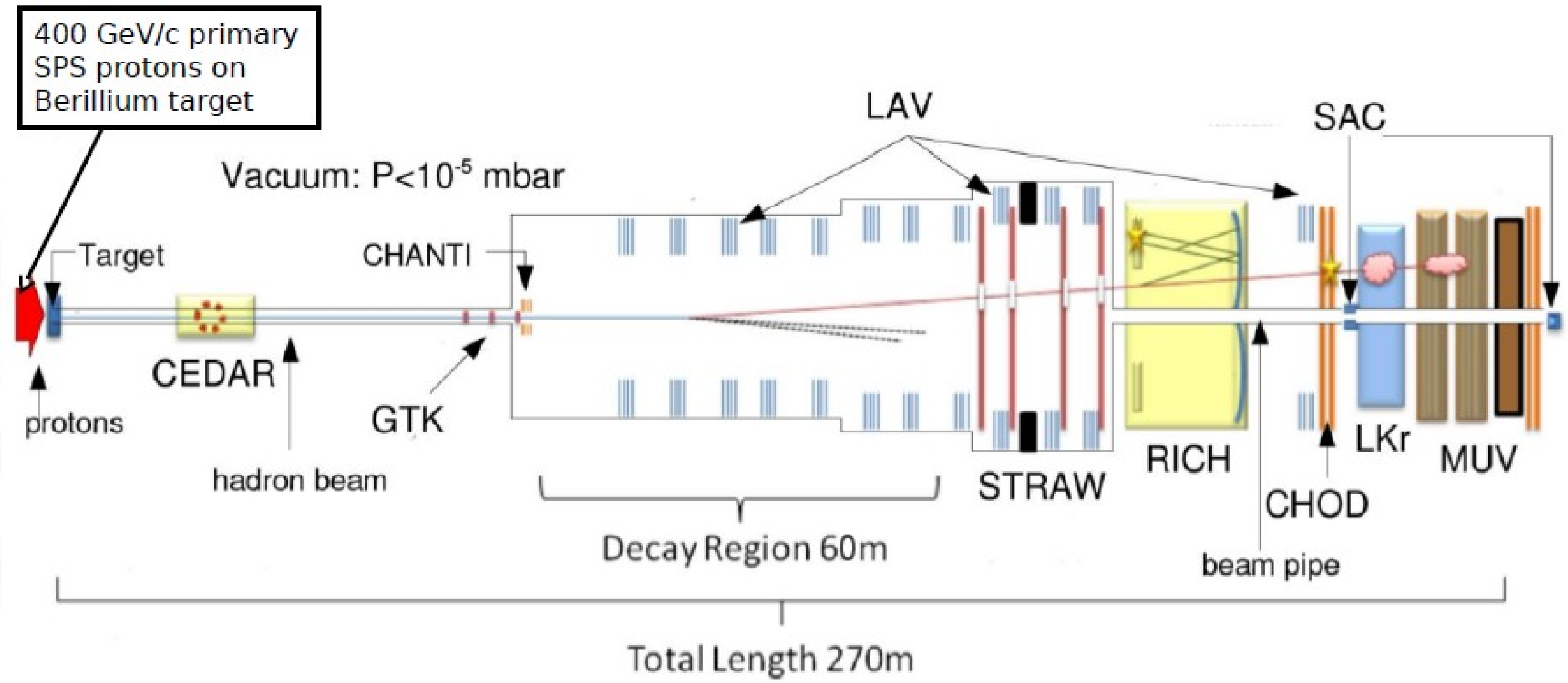
Main background	(BR)
$K^+ \rightarrow \pi^+ \pi^0$	63.55%
$K^+ \rightarrow \mu^+ \nu_\mu$	20.66%
$K^+ \rightarrow \pi^+ \pi^0 \pi^0$	1.76%
$K^+ \rightarrow \pi^+ \pi^+ \pi^-$	5.59%
$K^+ \rightarrow \pi^0 e^+ \nu_e$	5.07%
$K^+ \rightarrow \pi^0 \mu^+ \nu_\mu$	3.35%
Signal: $K^+ \rightarrow \pi^+ \nu \bar{\nu}$	0.78×10^{-10}

Experimental strategy:

- 10^{13} K decays (2 years)
- Acceptance ~10%
- Background rejection:
  - 10^4 from kinematics
  - 10^8 from particle veto and particle identification

Many other rare or forbidden K and π^0 decays can be studied

The na62 experiment



- Secondary charged beam (K^+) of 75±1% GeV/c
- Rate at GTK 750 MHz (6% K^+, 94% π^+ and protons)
- Expected rate on downstream detectors 10 MHz
- Up to 3 MHz (MUV3) and 5MHz (CEDAR) per single channel
- O(100ps) time resolution needed to correctly match decay π and beam particle
- 60 m long decay volume in vacuum, starting at 105 m from target
- First commissioning run in fall 2014

TDAQ requirements

- Ultra-rare decays
- Reliability of vetoing power
- Large amount of output data

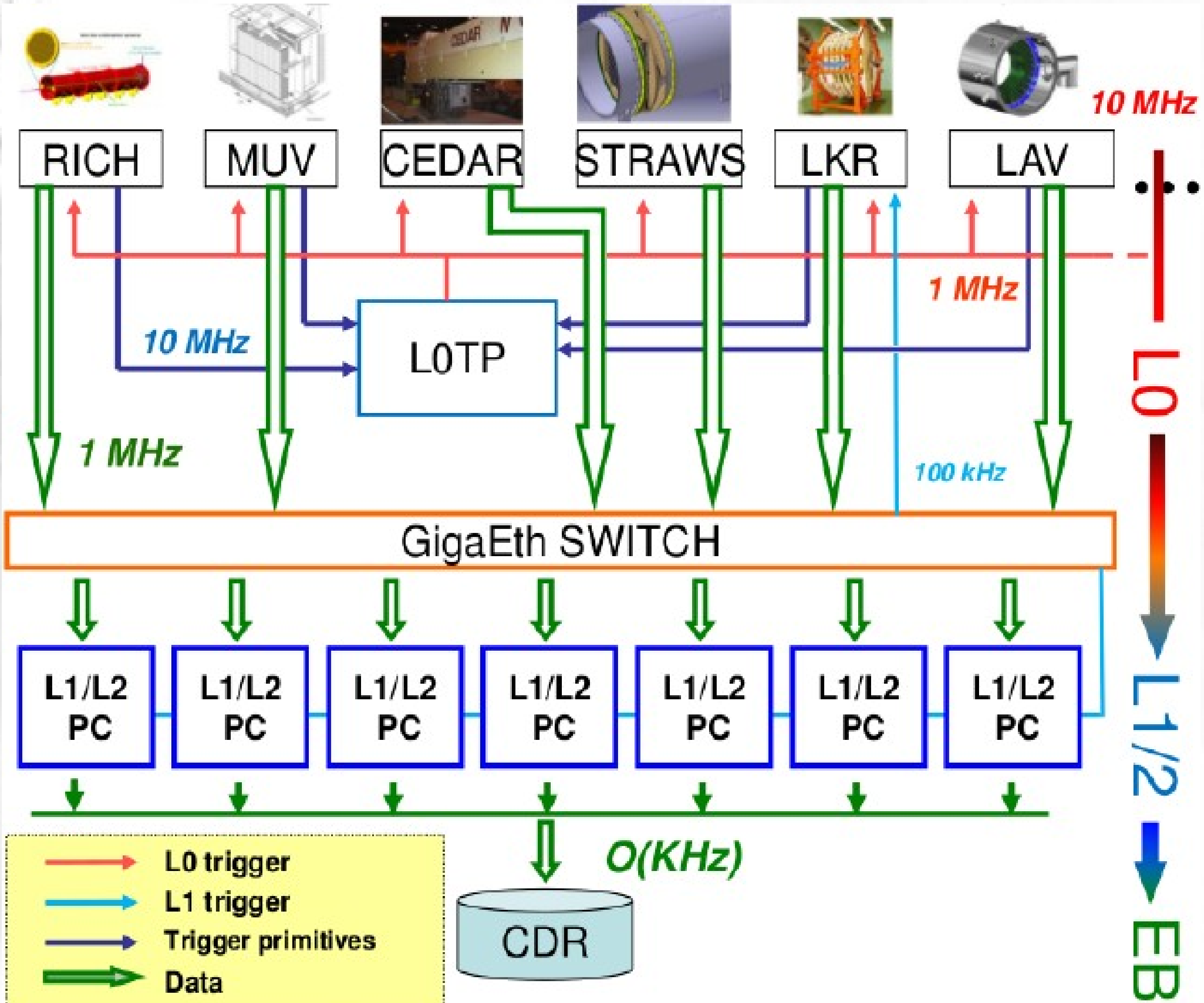
- High trigger efficiency (>95%)
- Low random veto (<5%) and dead-time
- High data bandwidth

DAQ Reliability
(undetected losses < 10^{-8})

- **Unified** trigger and data acquisition system
- **Completely digital** from FE to TDAQ
- Fully **monitored** system (inefficiency and flow control recording)
- **Uniformity** for most sub-detectors
- **Flexibility**: additional physics channels, custom hardware minimized

TDAQ system

12 subdetectors, ~80000 channels, 25 GB/s raw data



- L0: hardware level synchronous, based on trigger primitives from fast subdetectors
  10MHz → 1MHz
  1ms latency

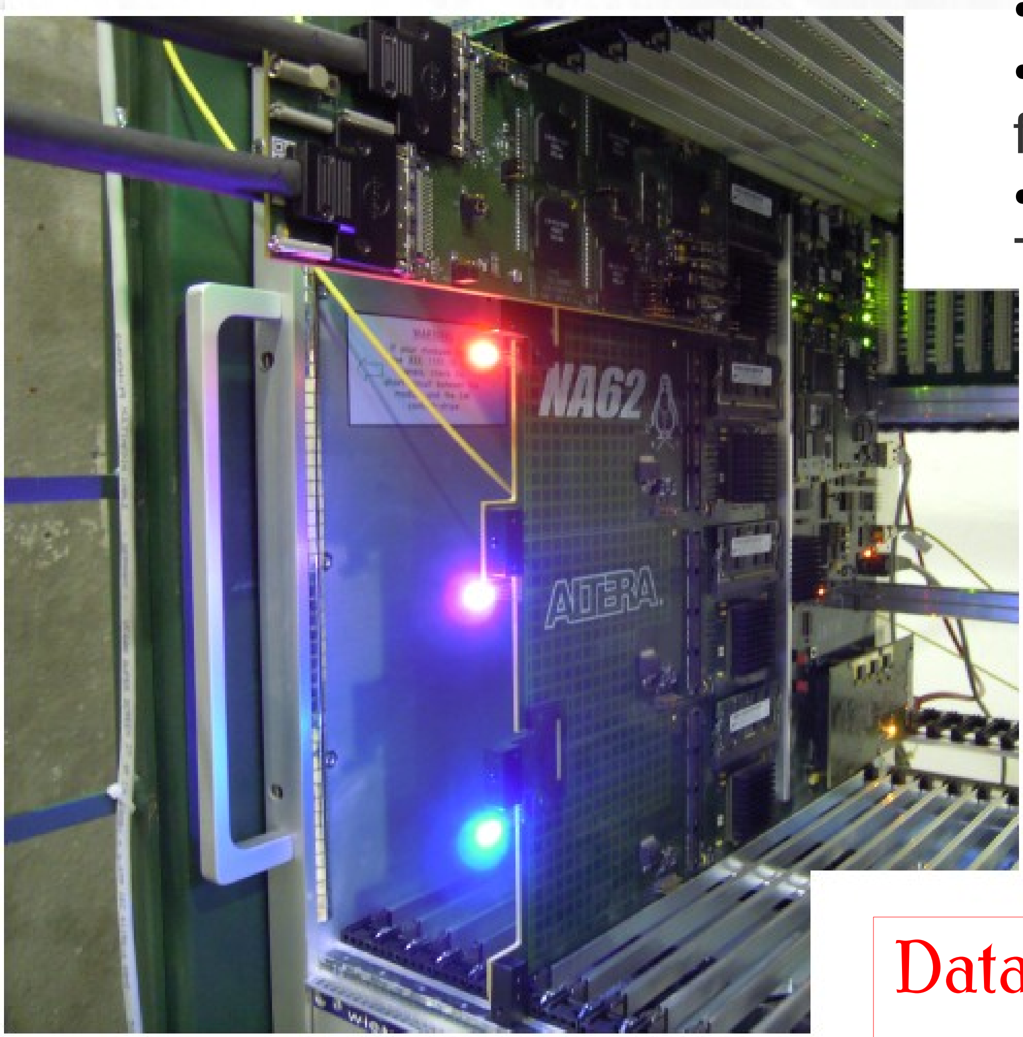
- L1: software level on single detector data
  1MHz → 100kHz

- L2: software level with complete information
  100kHz → 10kHz
  L1/L2 latency: spill

The TEL62 board

Trigger ELectronics for NA62

the common FPGA-based motherboard for trigger generation and data acquisition



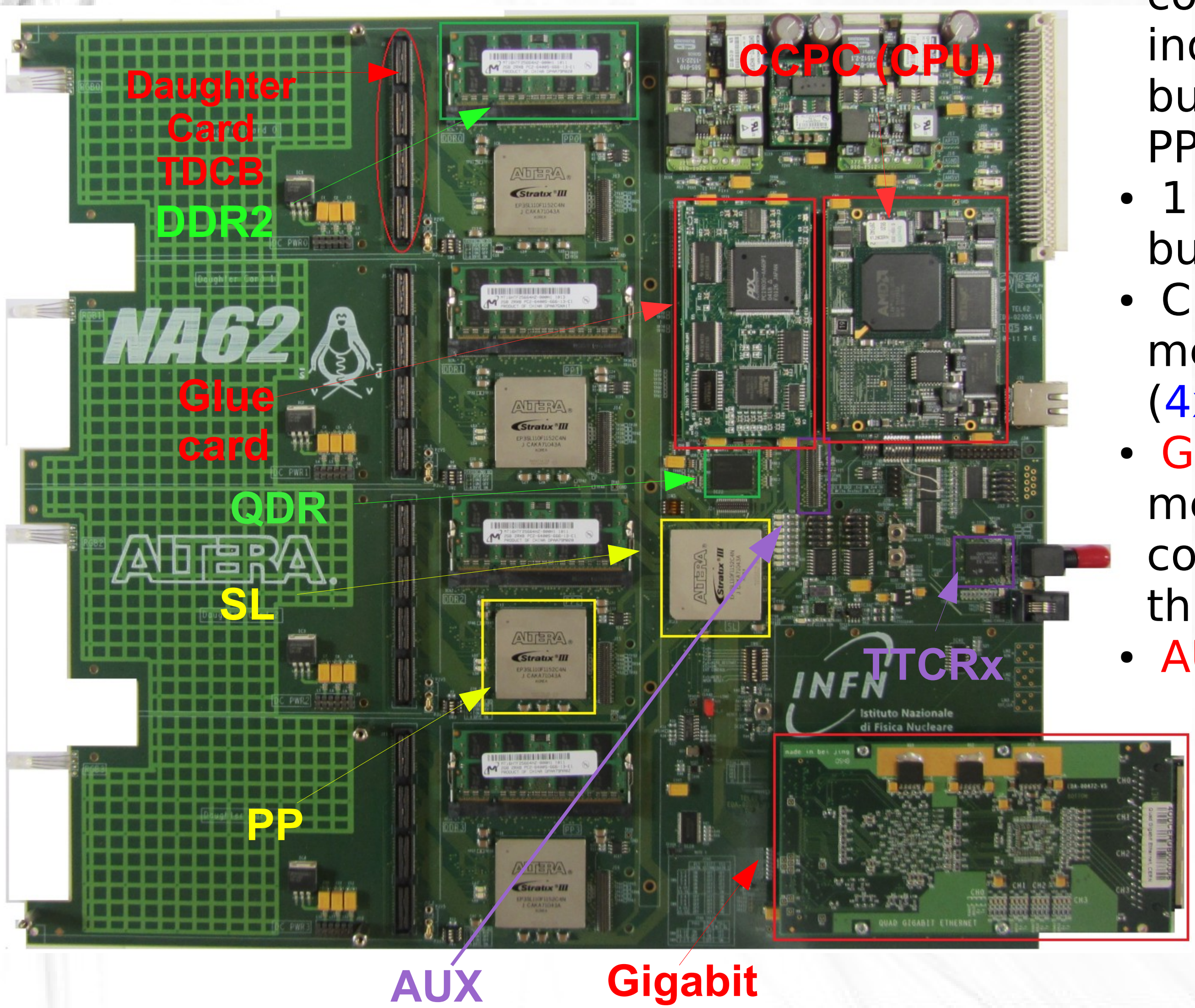
- Developed at INFN Pisa
- Total production O(100) boards used for many sub-detectors
- TEL62 is a major upgrade of the TELL1 (EPFL Lausanne) used in the LHCb experiment
  - 8x computational power
  - 20x buffer memory
  - Improved connectivity

- 9U Eurocard standard
- 16-layers printed circuit board with impedance-controlled lines
- Special routing of clock tree to avoid signal jitter

Data and L0 trigger primitives flow handler

The TEL62 board

- 4 PP-FPGAs (Altera Stratix III) each handling data from a digitizing daughter cards through a 200-pin connector
- 4 DDR2 memory buffers (2GB)



- 1 SL-FPGA (Altera Stratix III) connected to PPs through two indipendent 32-bit data buses at 160 MHz (5Gb/s per PP)
- 1 QDR RAM as temporary data buffer
- Custom Quad-GBE mezzanine as output board (4x 1Gbit Ethernet channels)
- GLUE card and Credit-Card PC mezzanines for slow control and configuration, connected through PCI bus
- AUX connector for TEL62 boards interconnection
- Clock and L0 trigger information received from an optical TTC link. TTCrx chip on board to decode them

The TDCB

The TDC Board is a Custom TEL62 mezzanine developed in Pisa for time and time-over-threshold measurements

Characteristics:

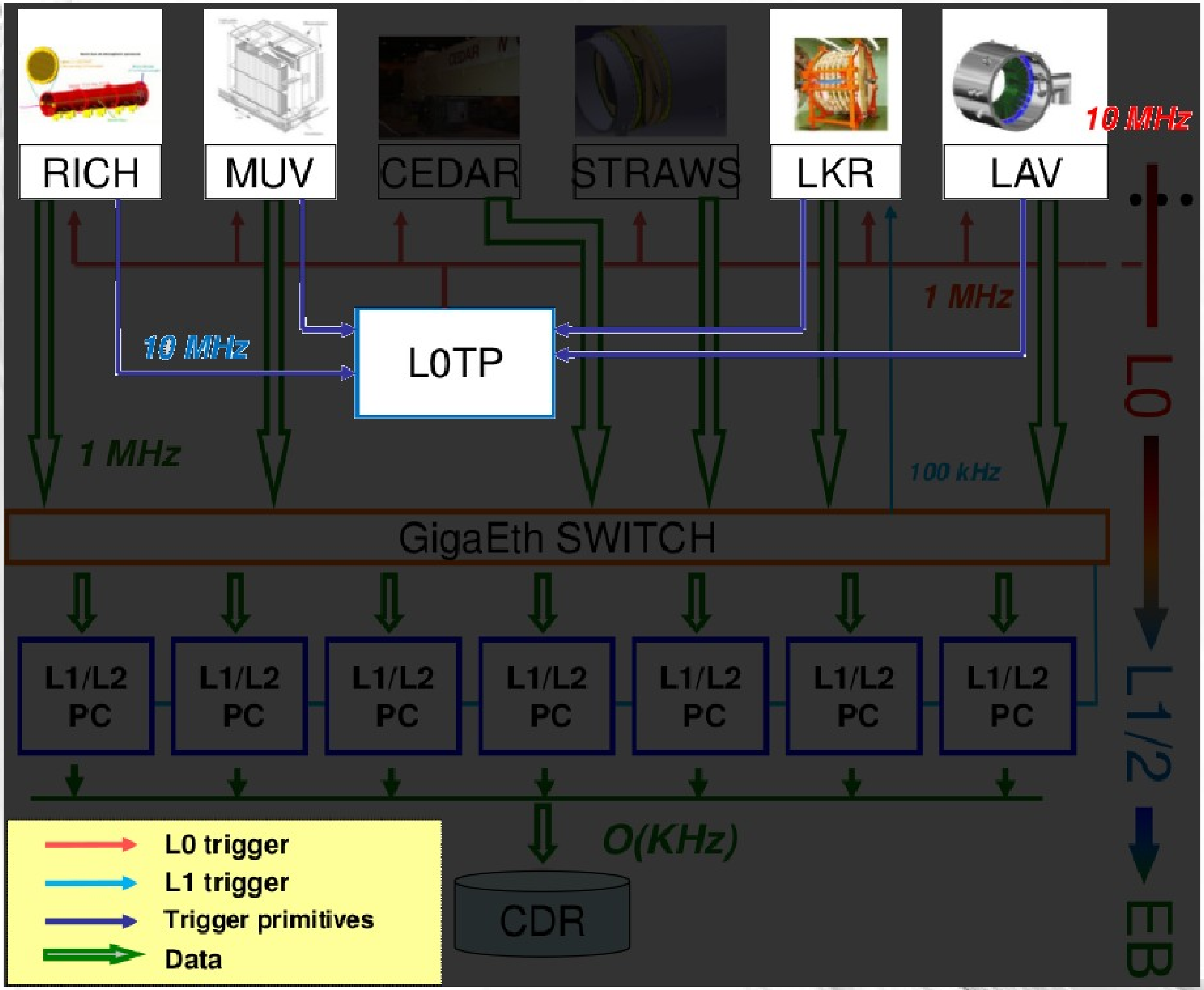
- 10 layers PCB
- 4 High Performance Time to Digital Converter (HPTDC) developed at CERN
- 4x32 LVDS input channels
- 19 bit leading and trailing time measurements with 100 ps LSB
- 1 TDCC-FPGA (Altera Cyclone III)
- 2 MB SRAM
- QPLL (clock jitter < 40 ps)

Functionalities of TDCC-FPGA:

- Data from TDC read periodically and then buffered
- Data packed with timestamp and counter
- TDC data emulator for testing and debugging
- Calibration trigger to front-end boards
- on-the-fly data pre-processing capability

L0 Trigger Processor

TEL62 produce L0 trigger primitives at the firmware level, directly from data. If certain logical conditions are fulfilled, the primitive is sent to L0 Trigger Processor.



Functionalities:

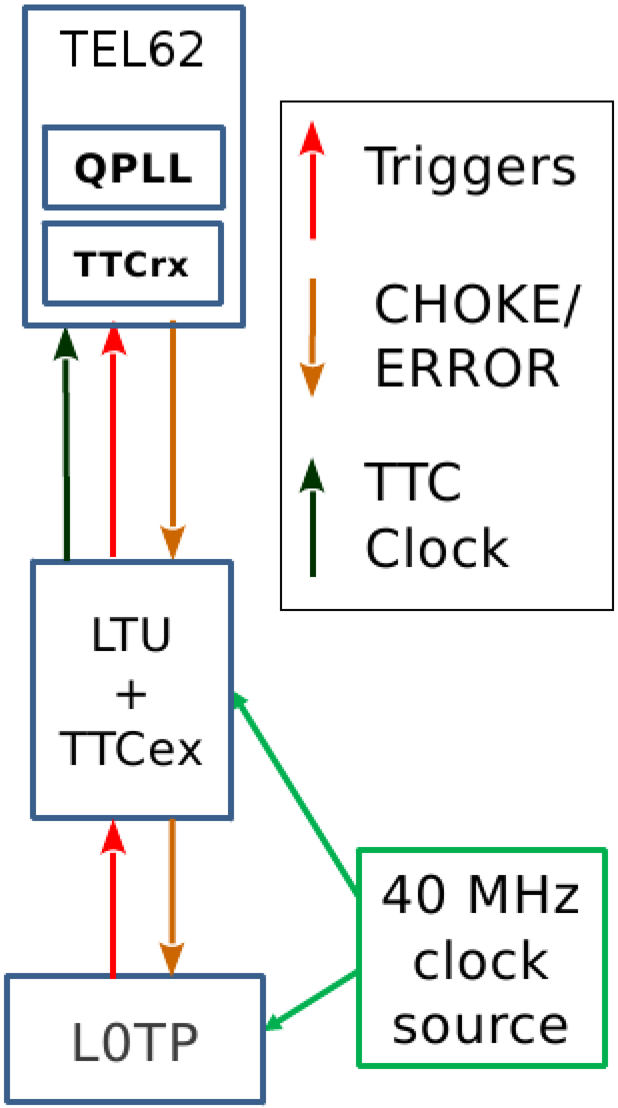
- Merge in time the information from all trigger primitive and take a decision
- Send back a L0 request through TTC system to TEL62s to collect data on PC farm
- Two implementations fully FPGA-based and FPGA-PC hybrid
- Maximum latency 1 ms

L0 Trigger Distribution

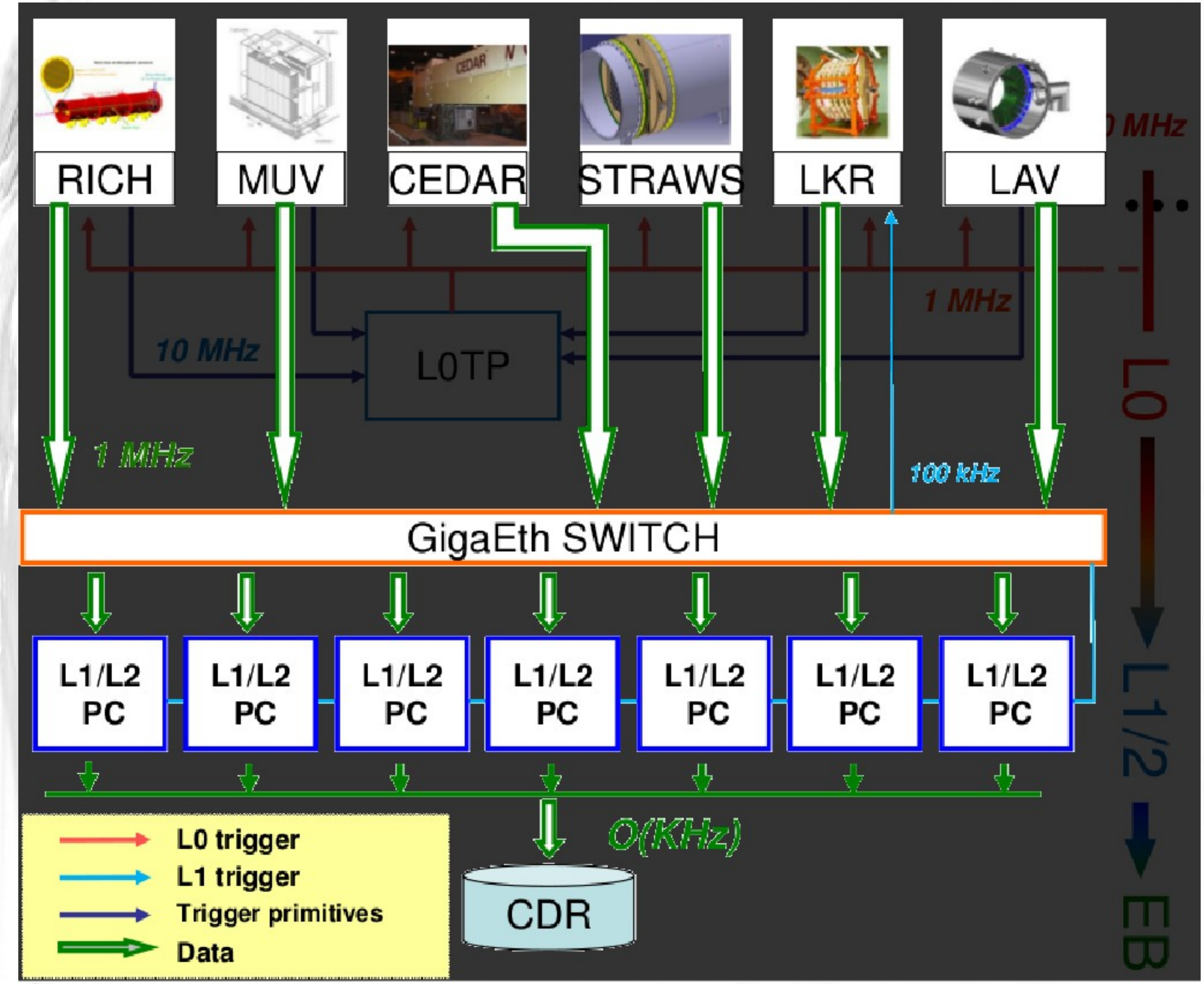
Local Trigger Unit (LTU) (ALICE development, Birmingham):

- Receive trigger from the L0 Trigger Processor
- Encode triggers and send to TTCex
- Receive CHOKE/ERROR backpressure signal from detector and propagate it to L0 Trigger Processor

TTCex (CERN development) is an encoder and laser trasmitter module with 10 optical outputs

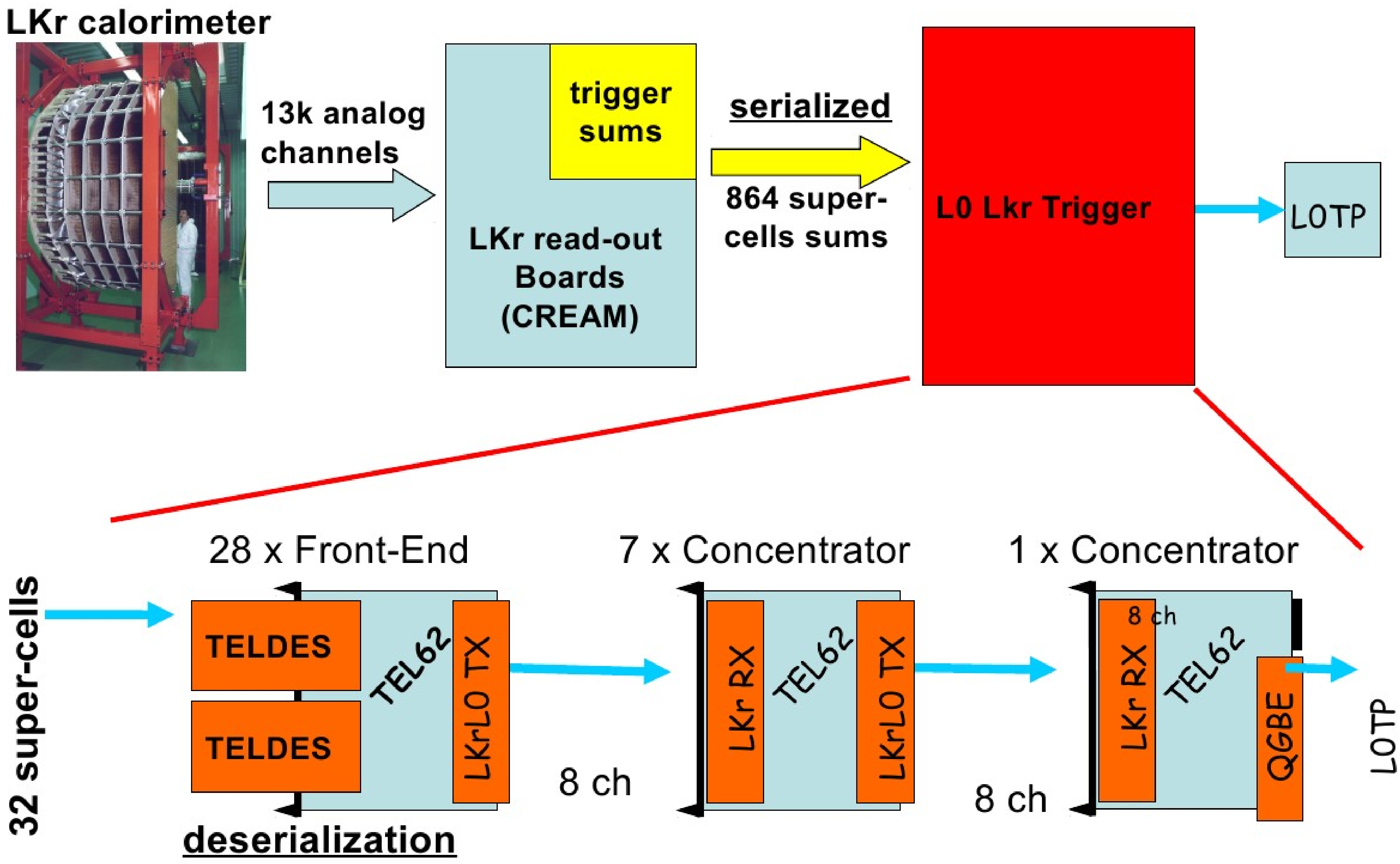


L1/L2 Trigger System



L1/L2 is a software trigger implemented on a farm of PCs and based on algorithms too slow for L0 and on detectors not available at L0

LKr L0 trigger system

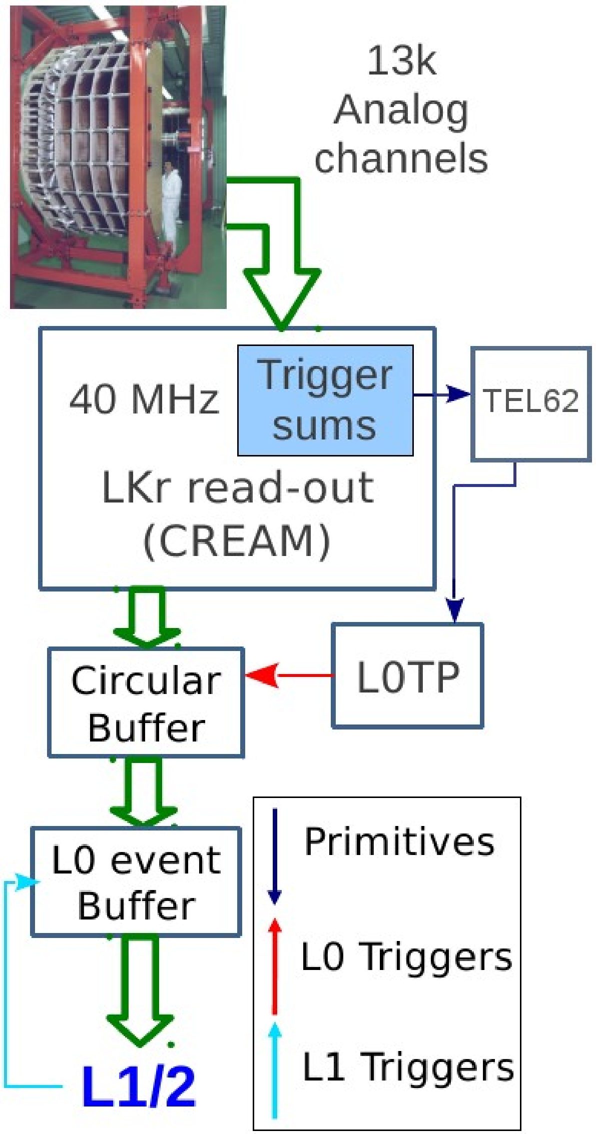


The LKr readout chain

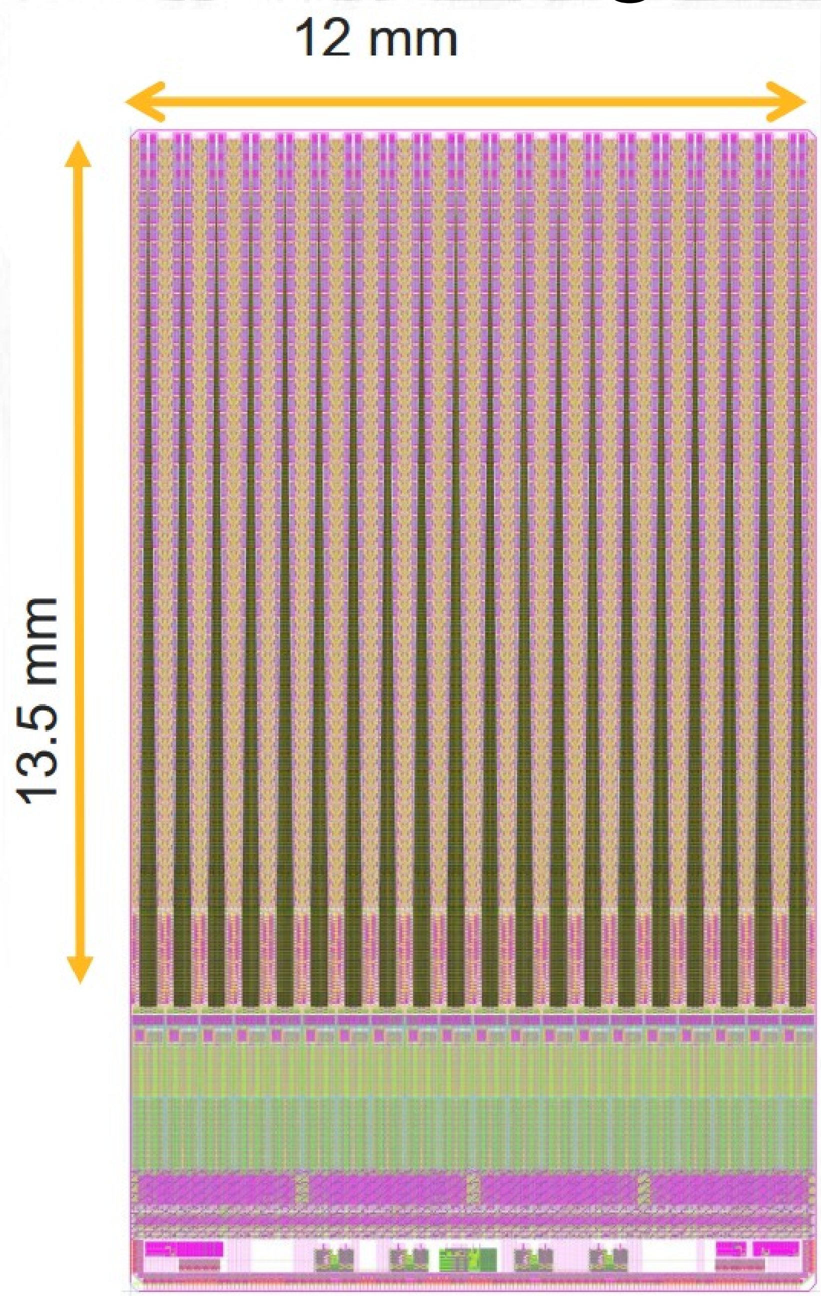
The Calorimeter REAdout Module (CREAM) is the readout board of the Lkr calorimeter developed to cope with the experiment's demanding requests

- VME 6U module
- Able to digitise 32 Lkr channels with 40 Mhz FADCs
- Select data upon reception of the L0 and L1 trigger signals

Lkr (electromagnetic) calorimeter data are read out only after L1 trigger



The Gigatracker Readout

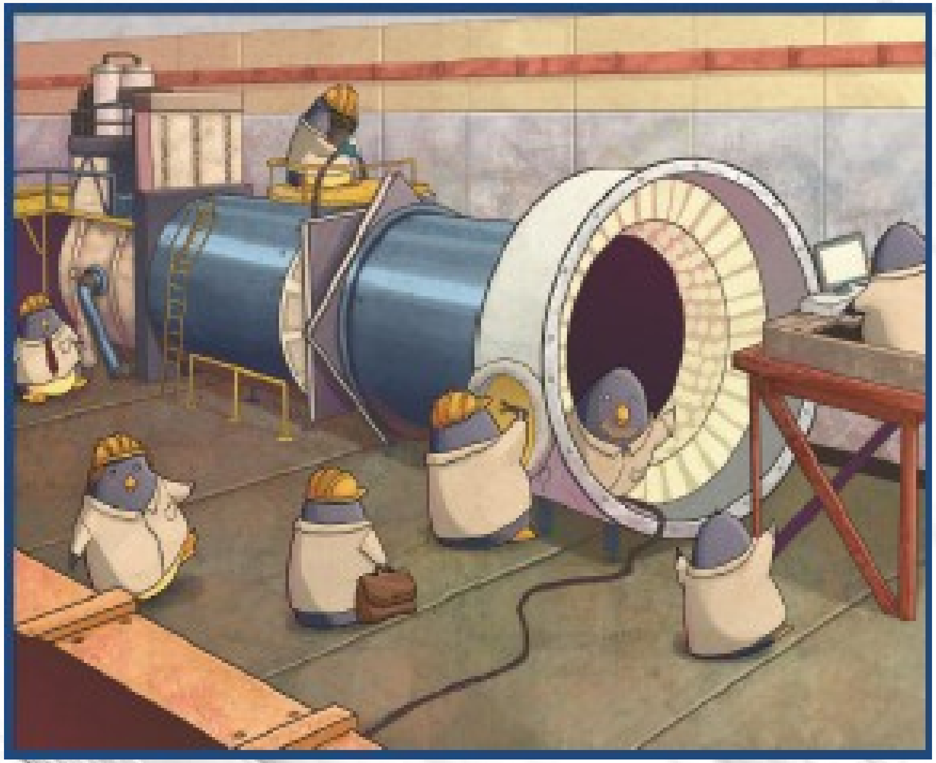


- The system is composed by 54000 TDC pixel channels silicon detectors over 3 station
- measure position (300 μm x 300 μm pixel size)
- measure arrival time with 200 ps resolution
- Readout efficiency is expected to be larger than 99%
- Offline custom electronics developped in Ferrara

conclusion

The NA62 Trigger and Data AcQuisition is being finalized and installed:

- A general purpose motherboard (TEL62) was developed as integrated trigger and data acquisition system for NA62
- A TDC based daughter-board (TDCB) has been designed for digital time and ToT measurements needed by NA62
- Some special digitizing and readout systems were developed for LKr calorimeter and GTK
- 2 options for the L0 Trigger Processor are being studied
- The software trigger algorithms are under study



We look forward to the 2014 data!

Spares

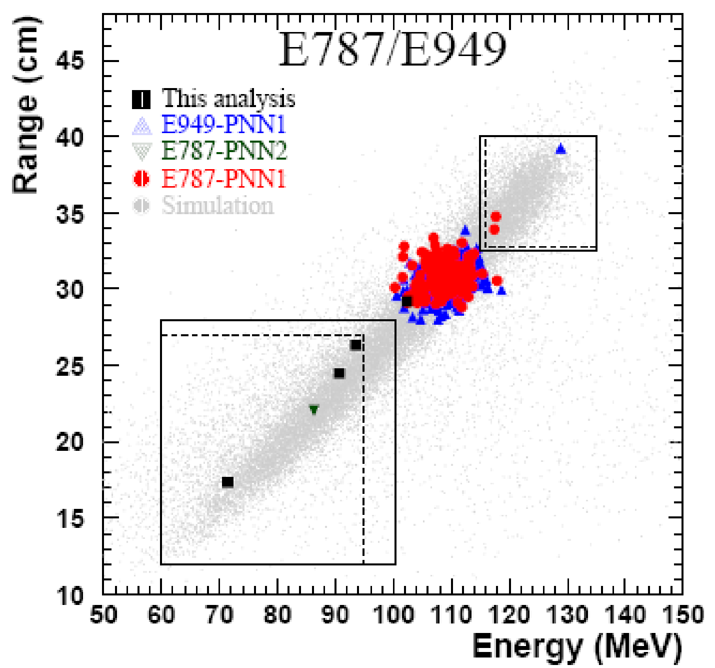
Experimental result

E787 and E949 at BNL:

- collect 7 events of $K^+ \to \pi^+ \nu \bar{\nu}$
- BR $(K^+ \to \pi^+ \nu \bar{\nu})$ (E787+E949) = $(17.3_{-10.5}^{+11.5}) \cdot 10^{-11}$

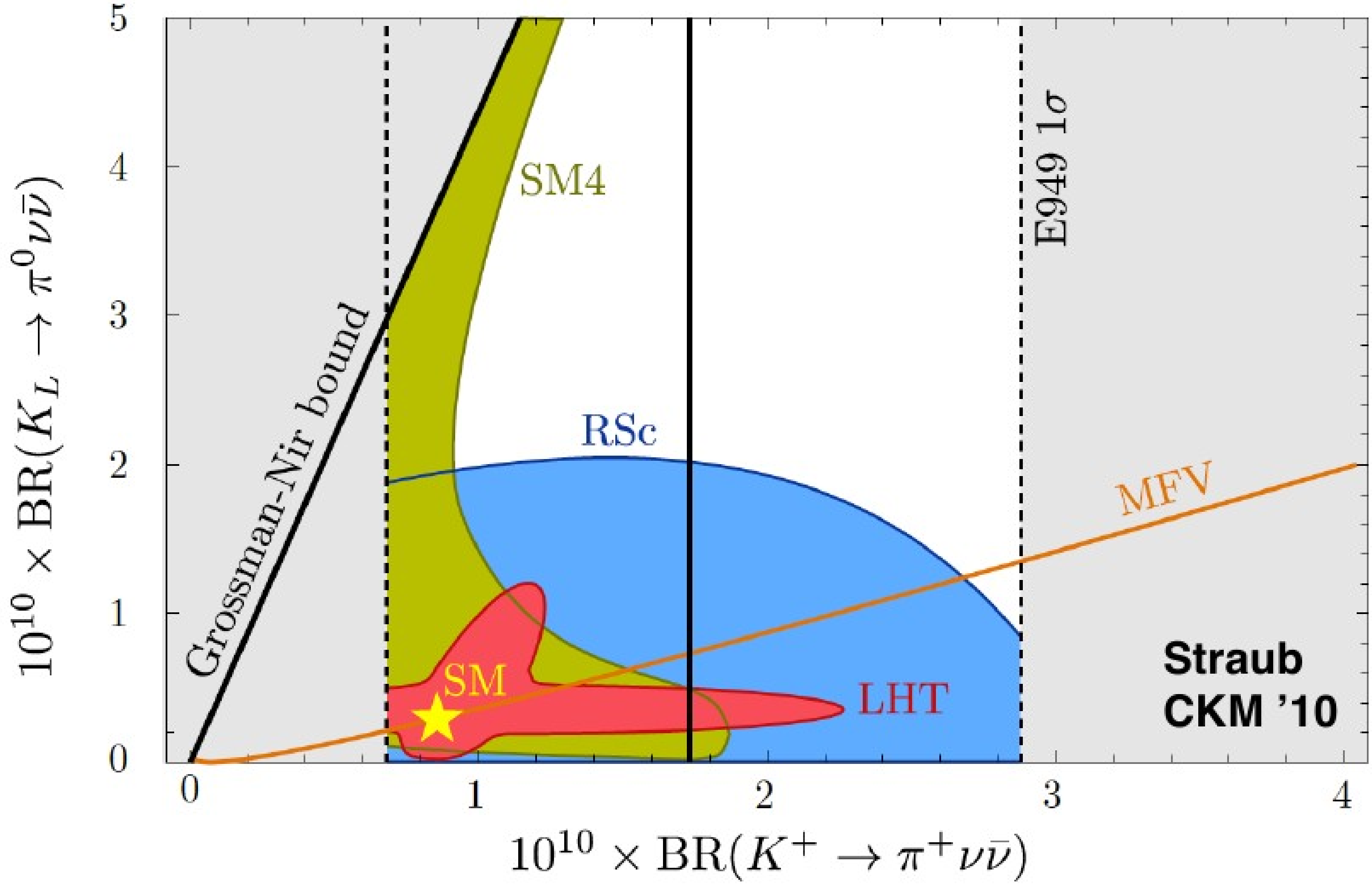
[Artamonov et al., Phys.Rev.Lett. 101 (2008)]

- Low energy proton (21.5 GeV/c) → K^+ decay at rest



$K^+ \to \pi^+ \upsilon \bar{\upsilon}$ and new physics

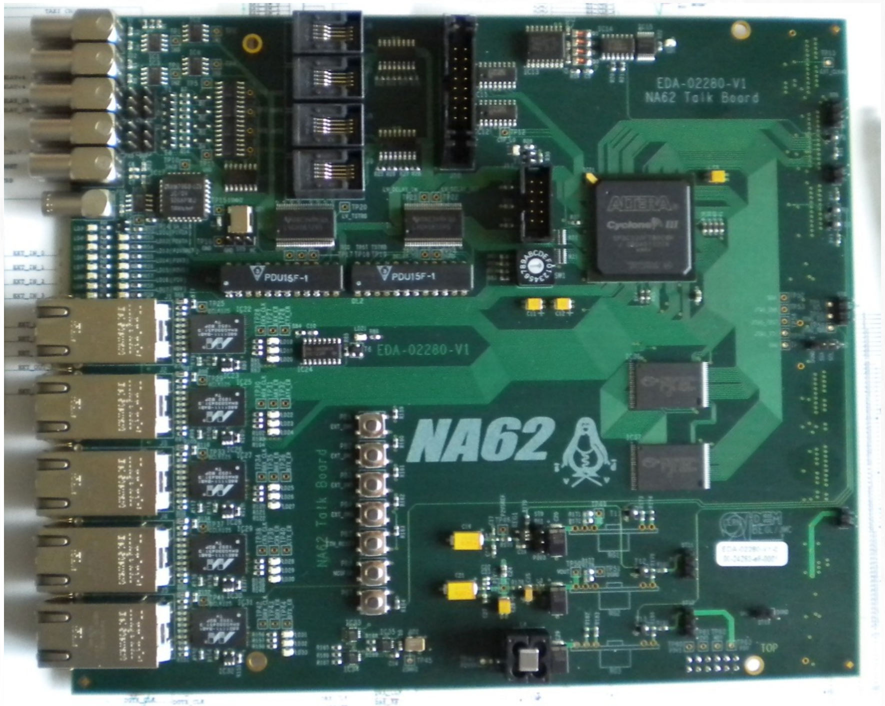
New physics affects BRs differently



SM4: SM with 4th generation (Buras et al. '10)
RSc: Custodial Randall-Sundrum (Blanke '09)
LHT: Littlest Higgs with T parity (Blanke '10)
MFV: Minimal flavor violation (Hurth et al. '09)

TALK Board

The **T**rigger **A**dapter for **L**iquid **K**rypton calorimeter is a multipurpose daughter board for the TEL62 developed at CERN



Characteristics:

- 6U VME
- PCB 10 layers
- 1 FPGA Cyclone III
- 1 Taxi chip
- 5x32 bit buses to the TEL62
- Many I/O connectors

TALK purpose:

- Interface between old Lkr readout and TTC system for NA62 Tecnical Run in 2012 (before the development of the CREAM)
- During the Tecnical Run was used even as proto L0 Trigger Processor
- Lkr calibration logic and test bench for CREAM modules
- Synchronization of the timing signal from the SPS