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The CERN NA62 experiment: Trigger and Data Acquisition

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The main goal of the NA62 experiment at CERN is to measure the Branching Ratio (BR) of the ultra-rare decay of a charged kaon into a charged pion and two neutrinos (K+⟶π+νν).
It aims to collect about 100 events in two years of data taking and to test the Standard Model of Particle Physics (SM), using the positive charged proton beam provided by SPS accelerator.
The key issues are readout uniformity of sub-detectors, scalability, efficient online selection and lossless high-rate readout. The TDCB and the TEL62 boards are the common blocks of the fully digital Trigger and Data Acquisition system (TDAQ) and they will be used for most sub-detectors in the high-flux rare decay experiment.
TDCBs measure hit times for sub-detectors, TEL62s process and store them in a buffer, extracting only those requested by the trigger system, which merges trigger primitives also produced by TEL62s.
The complete dataflow and firmware organization are described.

Summary

The NA62 experiment at the CERN SPS aims at measuring the ultra-rare kaon decay K+ ⟶ π+νν as a highly sensitive test of the Standard Model (SM) and a search for New Physics.
The detection of this process is very challenging due to the smallness of the signal and the presence of a very large background, therefore a very low undetected DAQ inefficiency, below 10−8, is an important issue. NA62 aims to collect about 100 signal events in 2 years of running.
There are several detectors distributed before, along and after the 65 m long fiducial decay region: among the main ones GTK and STRAW are used for K+ and π+ tracking, CEDAR and RICH for particle identification while LAV, LKR and MUV to veto photons, positrons and muons.
A scintillator hodoscope (CHOD) acts as a fast timing and trigger device.
The devices used for this purpose are a general-purpose trigger and data acquisition board (TEL62) and its mezzanine cards (TDCB) hosting high-performance TDC chips.
The TDCB houses 4 HPTDC chips developed at CERN, each HPTDC provides 32 TDC channels operating in fully digital mode at 98 ps LSB resolution, with some internal buffering for multi-hit capability and a trigger-matching logic allowing the extraction of hits in selected time windows.
The TDCs produce two 32 bit-long words for each LVDS signal in each channel, one word for the time of the leading edge of the pulse and one for its trailing edge.
The data are then buffered before being read periodically by the on-board FPGA, which adds a time-stamp and a counter to the data stream and addresses it to the TEL62.
Several other features are implemented in the TDCB firmware, including a TDC data simulator for testing purposes, the possibility of triggering front-end board calibration signals through an output line and the controller for two on-board 2 MB SRAM memories usable for monitoring or online processing.
The TEL62, a highly-improved version of the TELL1 board developed by EPFL Lausanne for the LHCb experiment, is the main device of the NA62 TDAQ: about 100 cards will be installed on the experiment. The board architecture is based on a star topology: 4 “Pre-Processing” (PP) Altera FPGAs are connected to a single “Sync-

Link" (SL) Altera FPGA. The 4 PPs are directly connected to the 4 mezzanines, for a total of 512 input channels. The amount of data arriving from the TDCs can be up to a few tens of MB/s per channel, depending on the sub-detector. Data are organized in packets, each one related to time frames of 6.4 us duration. The PP has the role of collecting and merging the data and later organizing them on the fly in a 2GB DDR2 memory, where each page is related to a single 6.4 us window. Inside the page data are packed using an optimized custom algorithm. Whenever a trigger arrives the data within a programmable number of 25 ns long time windows around the trigger timestamp are collected and sent to the SL. The data from the 4 PPs are merged and synchronized inside the SL, pre-processed and stored in a 1MB QDR SDRAM temporary buffer from which they are later extracted for formatting into data packets, which are sent through 4 Gigabit Ethernet links hosted on a custom daughter card to a computer farm that performs additional cuts and eventually writes events to permanent storage.

Some detectors don't use this common TDAQ system, like the Liquid Krypton (LKr) calorimeter and the silicon Gigatracker.

The Liquid Krypton calorimeter will be readout by Calorimeter REAdout Modules (CREAMs) which providing 40 MHz 14 bit sampling for all 13248 calorimeter channels, data buffering, optional zero suppression and programmable trigger sums for the L0 Lkr calorimeter trigger processor, also based on TEL62 boards.

The Gigatracker readout is based on the TDCpix ASIC designed to meet the requirements of the detector: the chip readout efficiency is expected to be larger than 99% and each of the readout hits needs to be time stamped with a resolution better than 200 ps rms.

The design rate for the Level 0 (L0) trigger output is below 1 MHz (with 1 ms latency). After L0, data are moved to PCs, and further trigger levels are implemented in software.

All electronic boards run on a common, centrally generated, free-running synchronous 40 MHz clock. The L0 trigger is fully digitally implemented, using the very same data which is subsequently read out, to avoid duplicating trigger and data acquisition branches and to allow accurate offline monitoring; a central trigger processor will asynchronously match the L0 trigger primitives generated with a good time resolution by a few fast sub-detectors, and dispatch a (synchronous) L0 signal to every board through the above mentioned clock distribution system.

The system has been extensively tested at the end of 2012 during a technical run at CERN.

The TALK board, a TEL62 multifunction daughter board, was used as L0 Trigger Processor (L0TP): it merges trigger primitives arriving from several subdetectors and sends trigger decisions back. The TALK board design was started by the need to provide a trigger interface between the TTC and the old NA48 trigger distribution system, in order to read the LKr calorimeter with the NA48 readout hardware during the technical run. Additional functions in the firmware have been added: driver for the calibration of the calorimeter, test bench controller for the characterization of the new CREAM boards for the LKr readout, and prototype of L0TP.

The prototype L0TP implements the logic to receive both triggers based on synchronous logic pulses and primitive packets generated by TEL62s, which are received through some of its five Ethernet channels. Communication with the PC is also done through an Ethernet interface. Besides the operation as a daughter board for the TEL62, a 6U VME frame to use the TALK board inside a VME crate was developed.

In normal running system operation is driven centrally by the TDAQ management system; L0
triggers are dispatched to sub-detectors by the L0TP, with its Local Trigger Unit (LTU), a slightly modified version of the ALICE LTU, that acts as transparent dispatcher of these triggers to the subdetector TTCex; the TTCex modules, built by CERN PH/ESE, do encode the clock and trigger signals onto optical fibres and send them to the readout modules.

Sub-detector data frames are sent to a farm of PCs for further data reduction.

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