TRB3 Platform
Time, Amplitude and Charge Digitisation

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on behalf of the TRB3 collaboration

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Jagiellonian University in Kraków

GSI

Johannes Gutenberg Universität Mainz

Goethe Universität Frankfurt am Main

Outline

- Motivation and Innovation
- TRB3 Platform: Hardware
  - Time digitisation with FPGAs
  - Amplitude digitisation with FPGAs
  - Charge digitisation with FPGAs
  - Integrated Trigger System
- Applications
- Conclusion & Outlook

What do we all want?

Motivation

We need

-high quality

-compact

-low cost

-fully configurable electronics.

Innovation

“misusing” digital FPGA in analogue domain for

-time

-amplitude

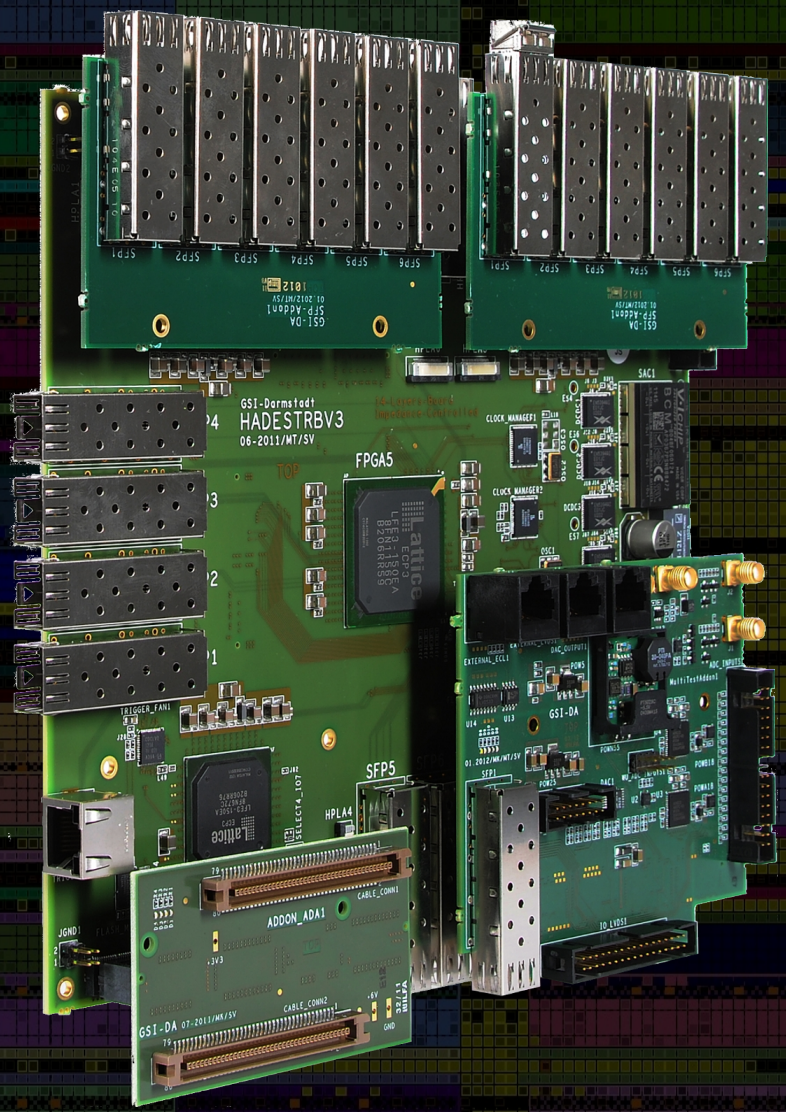
-charge

measurements.

Advantages of FPGA as FEE

- Off the shelf FPGAs as FEE
  - easily available, industrial quality in design and package
  - fully configurable - “Commoditization is the Future” G. Raven
  - high number of resources
- Possible to “misuse” resources
  - intrinsic delays for time measurements
  - LVDS receivers as discriminators
- Possible to alter the setup for different measurements
  - external pulser for amplitude measurements
  - signal integration for charge measurements

TRB3 Platform: Hardware

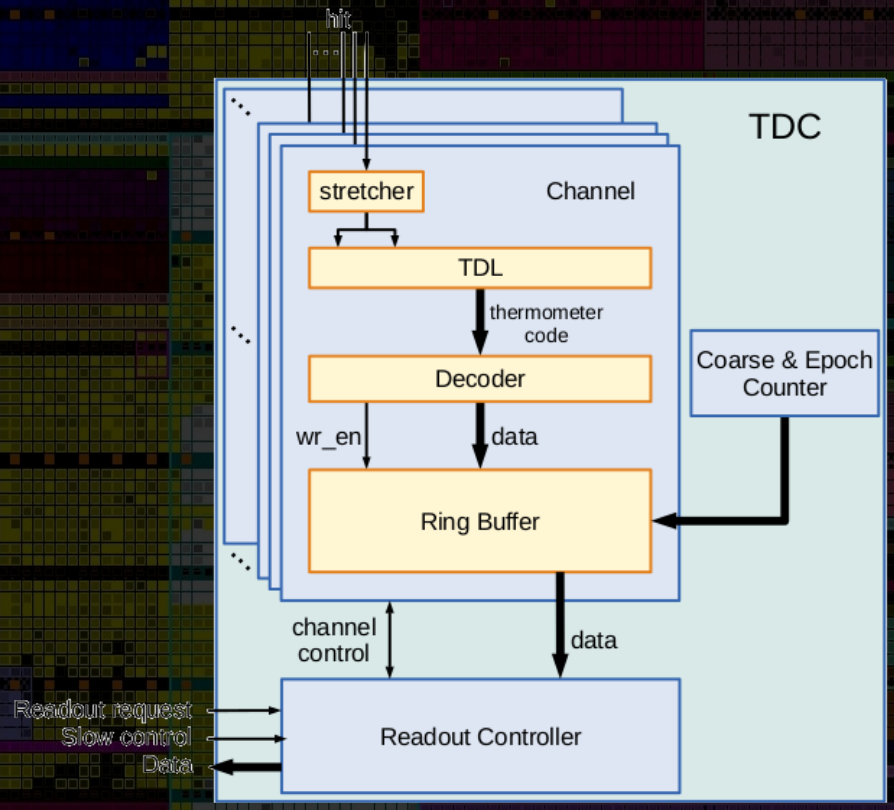


TRB3: the TRB3 collaboration
Photo by Gaby Otto, GSI Darmstadt, 06.09.2012.

- 5 Lattice ECP3-150EA FPGAs
- 4 peripheral TDCs with 256+4 channels
- useable as data hub as well
- central FPGA as CTS & GbE controller
- direct GbE connection for data and slow control; no CPU on board, all implemented in FPGA
- <20 ps time precision on every channel
- 50 MHz max. hit rate
- 700 KHz max. data readout trigger rate
- TrbNetwork for internal communication
- usable for large system as well as stand alone system: just 48V and GbE are needed to take data
- usable as a digital board, e.g. data/trigger hub
- applications: Leading edge and pulse width measurements

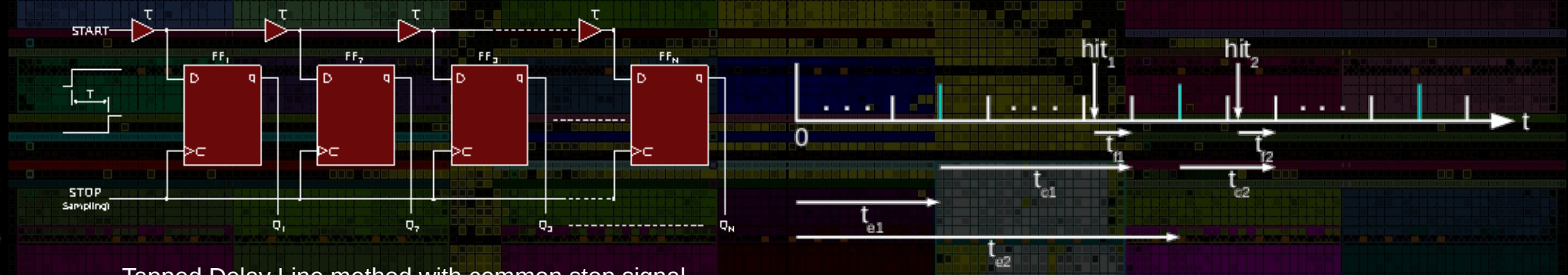
Time Digitisation

- Tapped Delay Line for fine time interpolator
- Coarse & Epoch counters for long measurement range
- Stretcher for short pulses
- Decoder: thermocode → binary
- Ring buffer
- Calibration hits from on chip oscillator



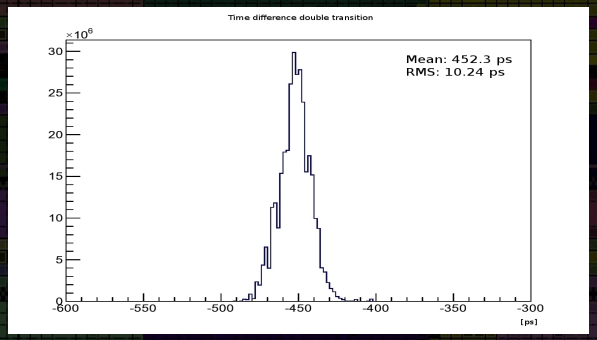
Simplified architecture of the TDC

Time Digitisation

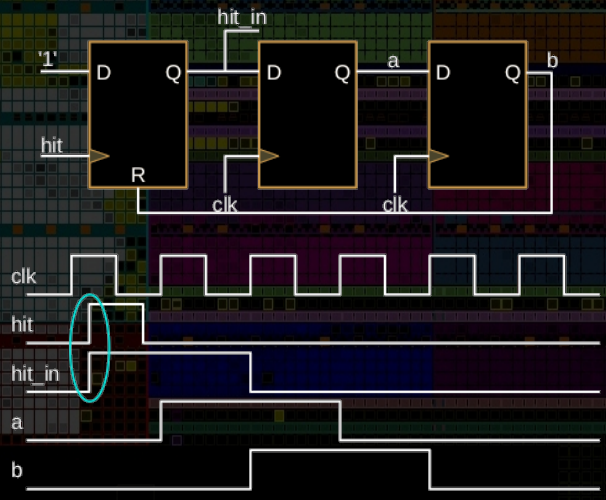


Tapped Delay Line method with common stop signal

- $\Delta t = (t_{e2} + t_{c2} - t_{f2}) - (t_{e1} + t_{c1} - t_{f1})$
- RMS measured: 10.24 ps
- Stretcher for short pulses (~500 ps)

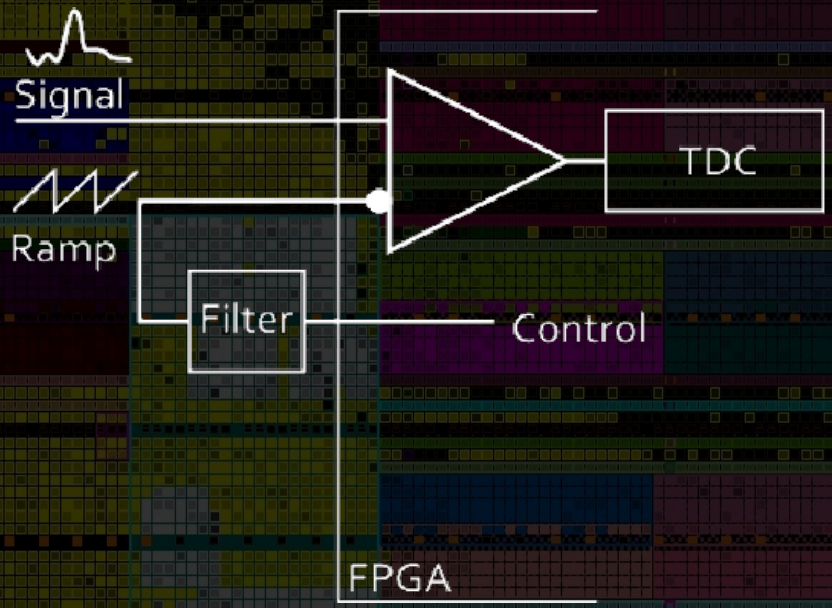


Time precision test



Amplitude Digitisation in FPGA

- A periodic ramp signal is applied to the reference pin of an LVDS buffer
- Input signal is applied to the other input
- Measure time until reference crosses input signal
- 10bit ADC, 20MSPS needs 31ps time precision
- Advantage: many channels in one FPGA (one ramp generator), no data transfer to the FPGA, low power



ch2 level [mV]	Mean [ps]	Jitter (RMS) [ps]
400	2551	50
800	3034	24
1200	3538	18
1600	4125	15

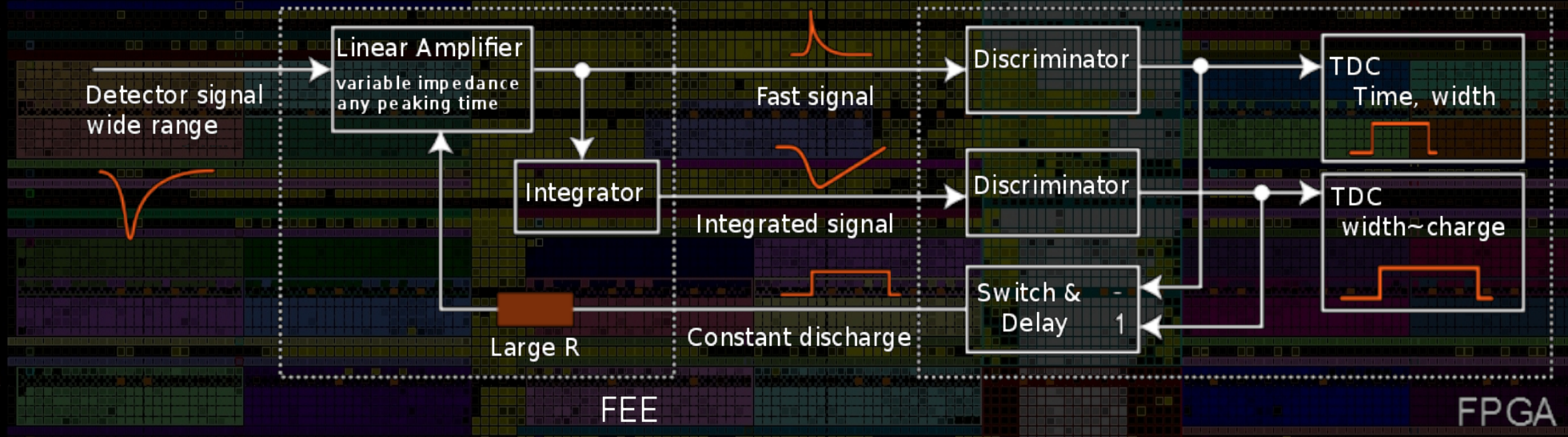
Measurements with externally generated ramp signal show that

- the ADC concept works
- the measured TDC time precision for 26ps ramps is compatible with an ADC with 10 bits precision and 20 MSPS
- An integrated solution with on board ramp generator has to be implemented and evaluated

Charge Measurement with FPGAs

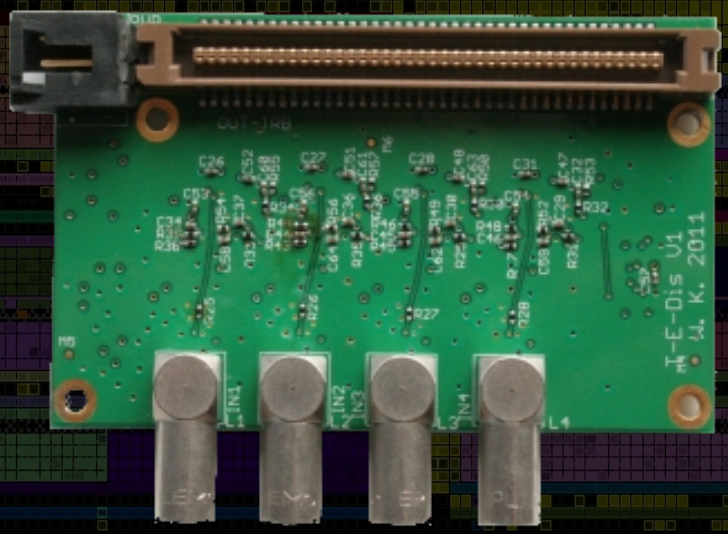
Idea: Modified Wilkinson ADC

- The input signal is integrated with a capacitor
- The capacitor is discharged using a current source → fast crossing of zero
- Measure time necessary to reach zero

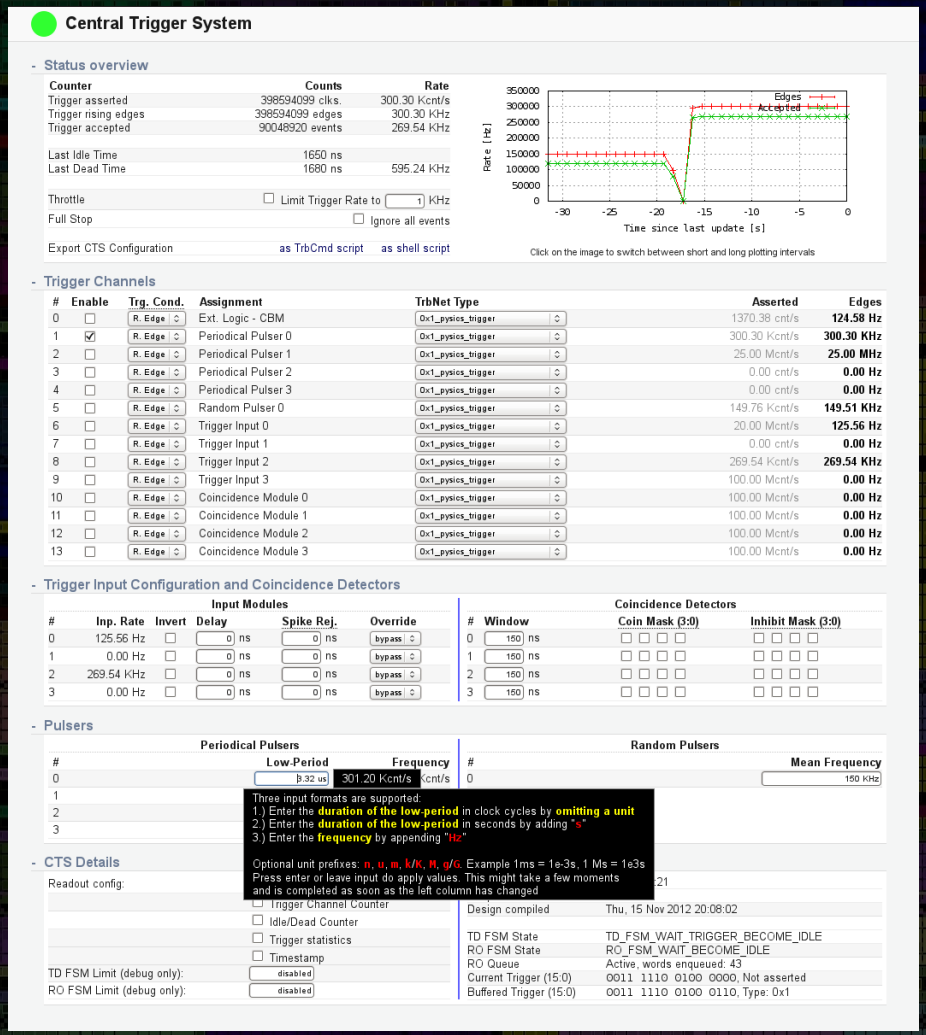


QDC Prototype

- Prototype Board (4 channels)
- First results with offline correction:
  0.2% charge precision, dynamic range:
  50
- Automatic base line restoration
- Increase of input range is possible with two integrator channels with different gains



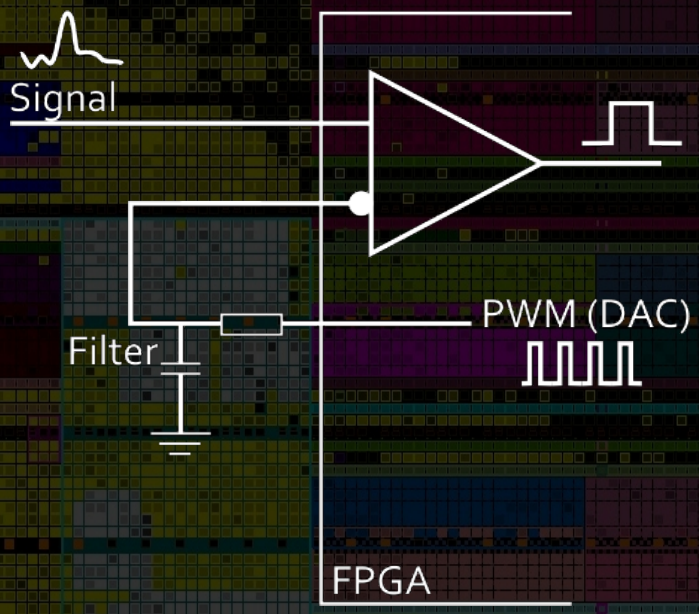
Integrated Trigger System

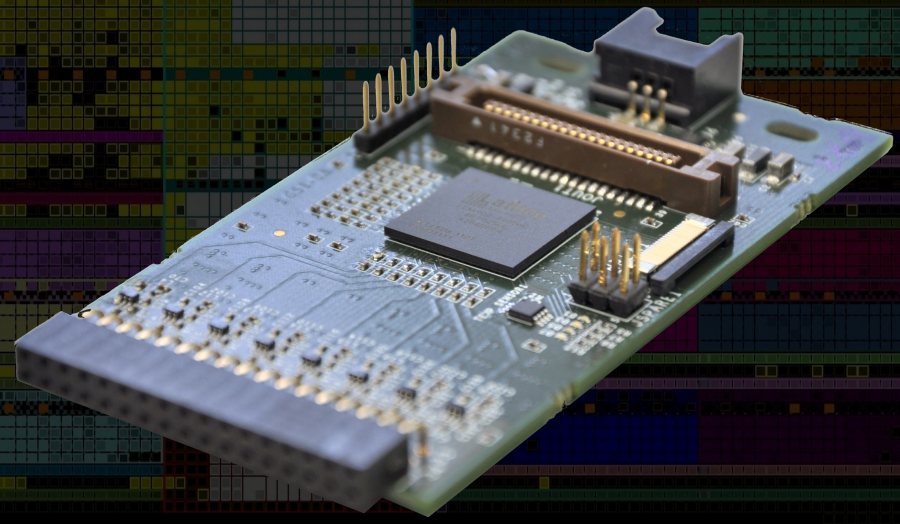


- Extendible and modular structure
- Master and slave mode operation
- Free running operation
- Up to 16 independent trigger modules
- 4 channel TDC for trigger time
- 8 general purpose trigger inputs
- Coincidence detection
- Periodic & Random pulser
- On-board and off-board trigger distribution
- Trigger generation from TDC channel inputs
- Tested successfully during the CBM and PANDA test beams with slave and master modes

Applications: PaDiWa FEE

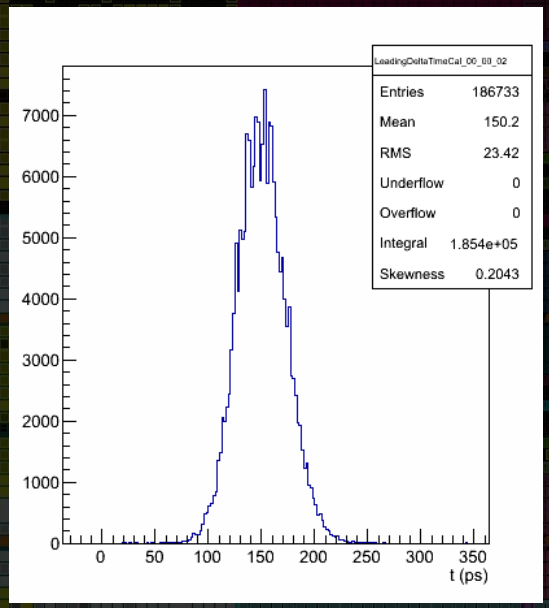
- Pre-amplified with commercial amplifiers (MMICs)
- Input LVDS buffers in FPGAs are used as discriminators – Lattice MachXO2
- The leading edge time and Time over Threshold is encoded in the digital pulse
- The thresholds are set by FPGA via PWM and low pass filter
- FEE is placed directly at the detector, only digital signals are sent out
- Time measurements are done by TDCs implemented in FPGA (TRB3)

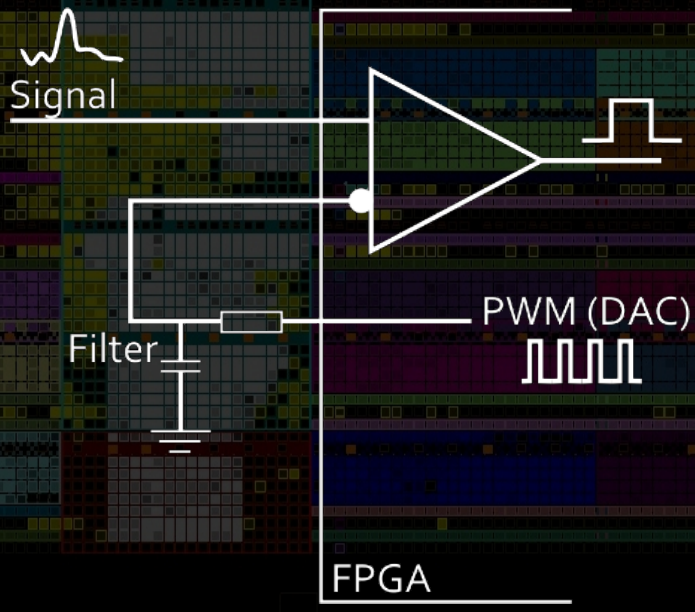




Applications: PaDiWa FEE

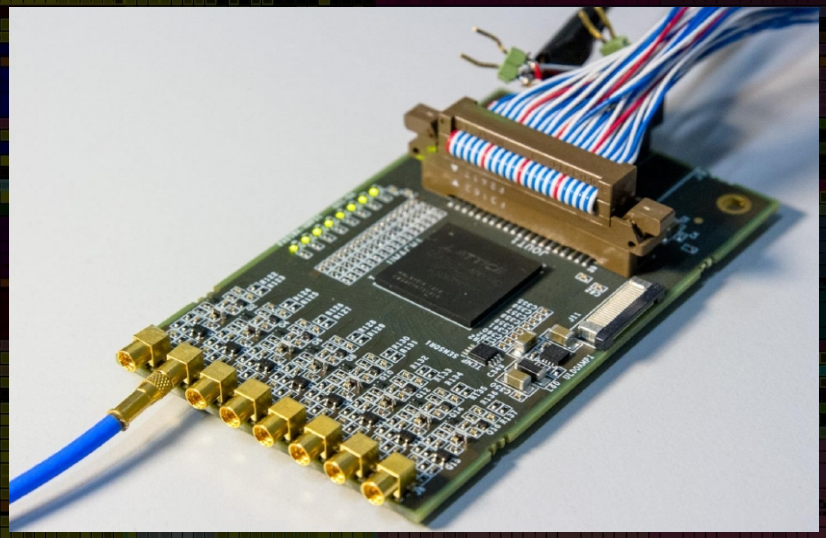
- Test setup: 500 µV, 6 ns width, analogue signal as input to PCB, amplification x40
- Threshold is set on the reference LVDS input PWM + low-pass with a resolution of <100 µV
- Pulser test: ~23 ps
- Single phototelectron laser test with MCP: ~70ps
- FEE cost (without PCB+connectors) per channel only 0.56€ (16 channel version)
- Tested at the PANDA DIRC and Barrel DIRC beam times in November 2012 and July 2013
- See Matteo Cardinali's talk on Thursday for more details

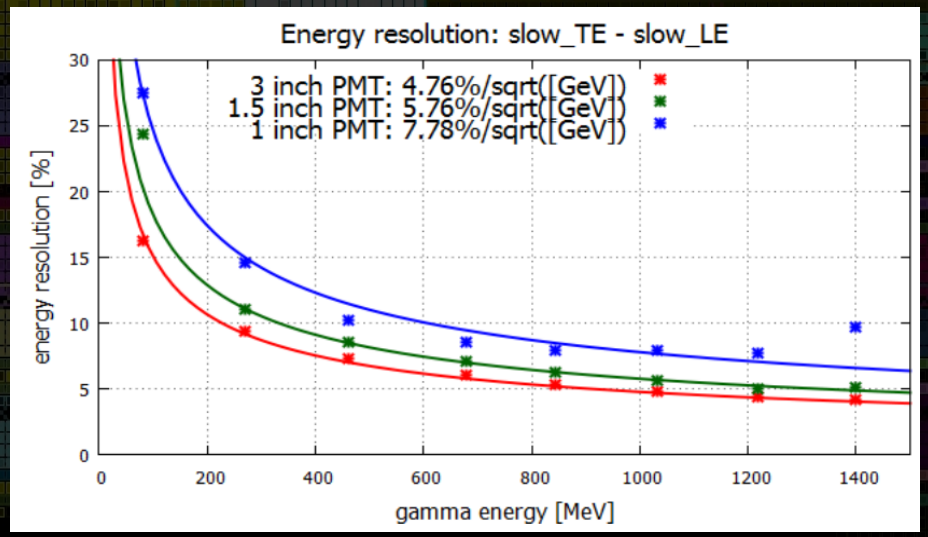




Applications: PaDiWa Amps

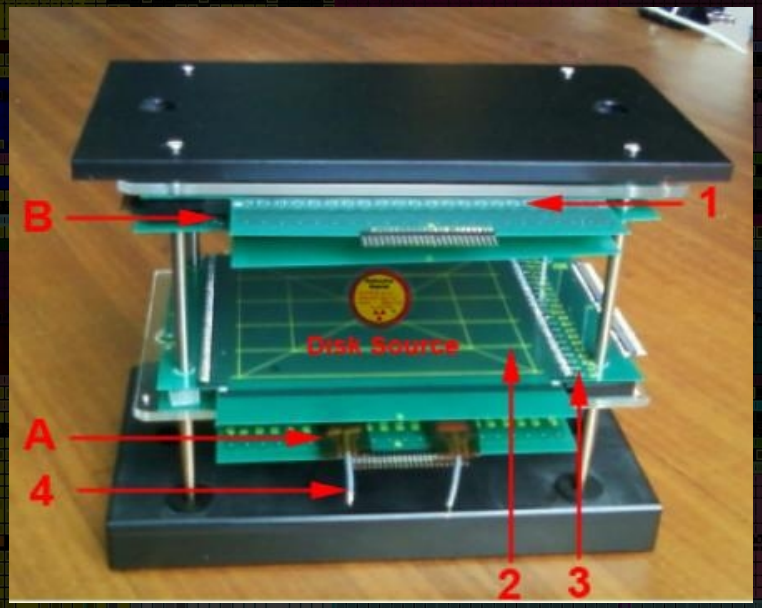
- Tested in lab with pulser and in gamma beam in Mainz (MAMI)
- Charge precision in lab: 0.5% (no walk correction)
- Charge precision: as low as 5% (no walk correction)
- Further investigations are ongoing



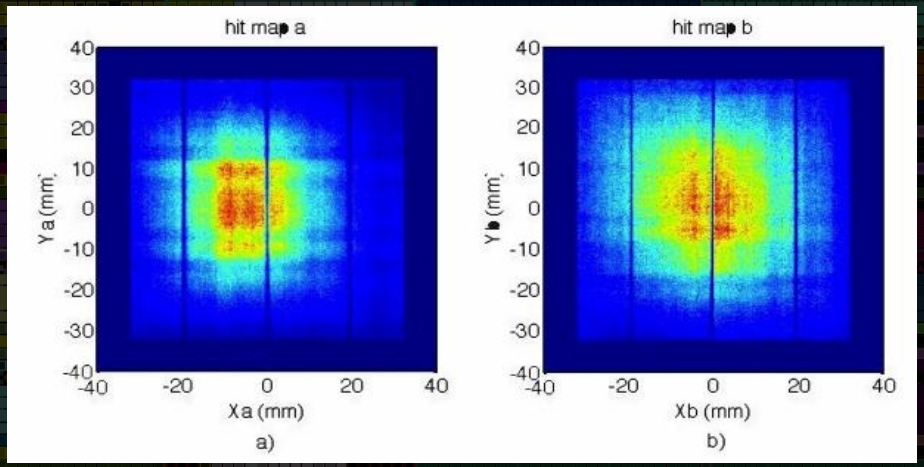


Applications: PET Scanner

- Positron Emission Tomography (PET) for molecular imaging
- Approach is RPC (Resistive Plate Chambers) based
- Simulations suggest factor 8 better performance over the best commercial tomography [1][2]
- Animal PET Prototype demonstrated 0.4 mm image resolution with TRB2 [3]
- Prototype for high resolution animal PET scanner and low sensitivity (for cost reasons) whole body human scanner is under development



A-detector a; B-detector b; I-X strips; 2-Y strips;
3-signal division network; 4-high voltage connections. [3]



Hit map in a) detector a, and in b) detector b. The shadowed vertical lines correspond to the 0.35 mm spacers used to define the gap width. [3]

[1] A. Blanco et al., Nucl. Instr. and Meth. A602 (2009) 780;

[2] M. Couceiro et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 2651;

[3] P. Martins et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 3760

Conclusion & Outlook

- Multi-purpose FPGA based TDC platform with 264 channels with a time precision of <20ps RMS
- Different FEE and AddOn boards
- All you need is power and Ethernet cable to run DAQ – thanks to the integrated trigger system and GbE
- FPGA based simple FEE: promissing lab and test beams first results
- Advantages: “simple”, off the shelf, flexible, TDC and DAQ is finished and ready to use
- Disadvantage: larger than a tailored ASIC solution
- Double edge detection in single TDC channel under construction
- TDC-based ADC design is being implemented and tested
- TDC-based QDC system for calorimeter application has been successfully tested in lab and in beam

TRB3 Community

Developers

Cahit Uğur	TDC
Jan Michel	TrbNet & DAQ
Grzegorz Korcyl	GbE
Manuel Penshuck	CTS
Michael Traxler	Organisation & Hardware
Ludwig Meier	Slow Control Software
Jörn Adamczewski-Musch	DAQ & Analysis
Sergey Linev	DAQ & Analysis
Matthias Hoek	Unpacking & Analysis

Active Users

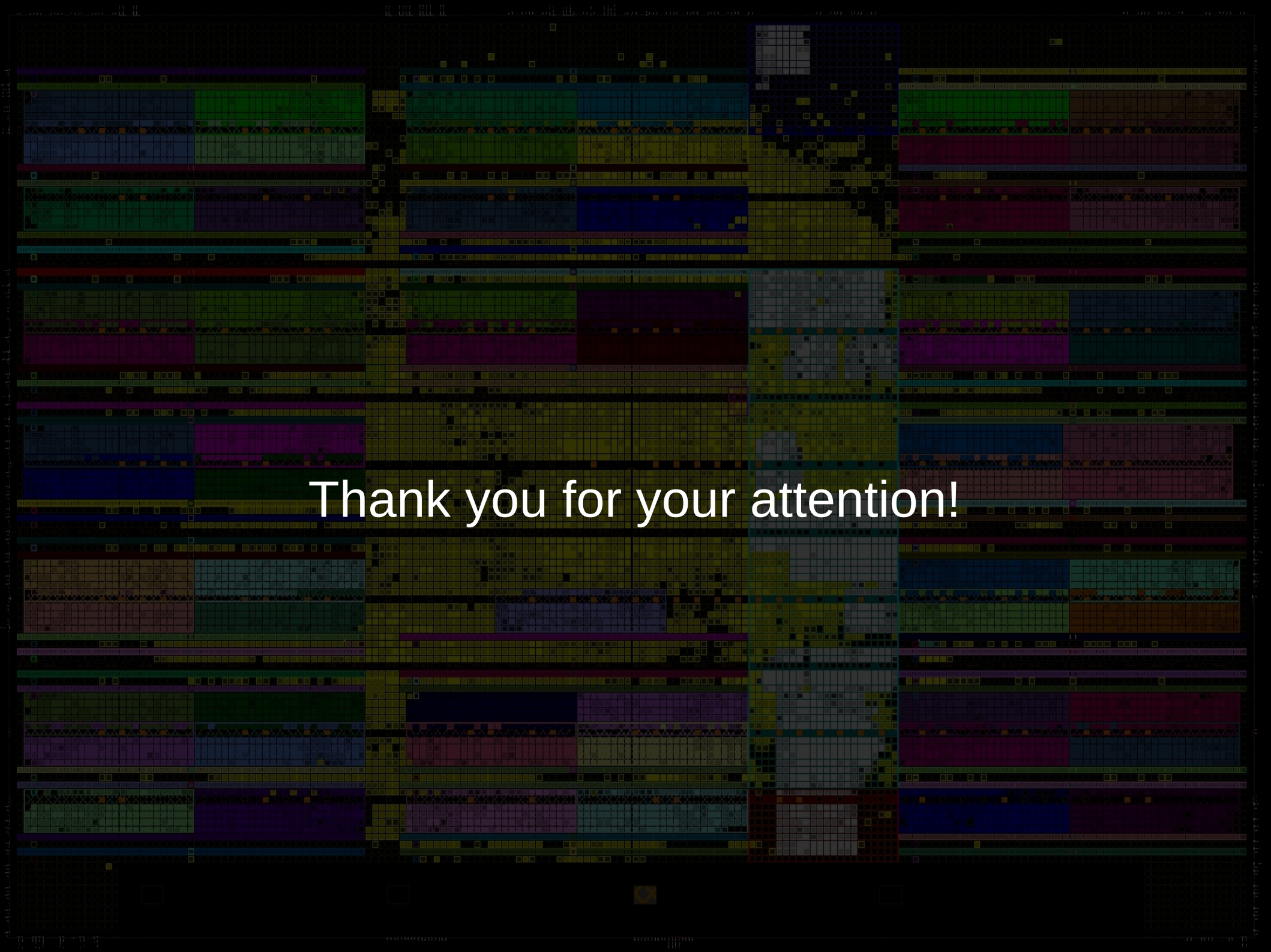
Marek Pałka
Christian Pauly
Adrian Schmidt
Andreas Neiser

PANDA DIRC Groups in Mainz & GSI

Detector Groups

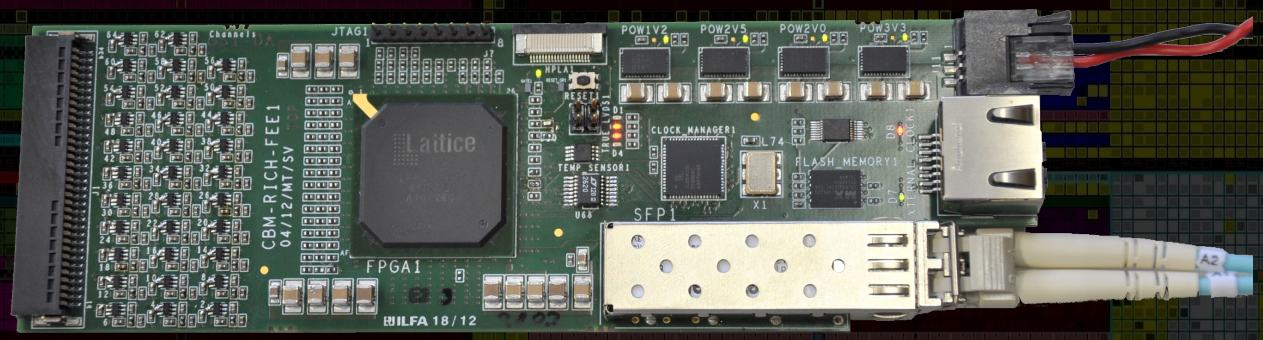
PANDA Barrel DIRC
PANDA Disk DIRC
PANDA ToF
CBM Forward Calorimeter
CBM – RICH
CBM – ToF
HADES MDC FEE
HADES Calorimeter
Mainz A2 Collaboration
Mainz Neutron Detector

Coimbra PET Scanner
and many more to come...


Thank you for your attention!

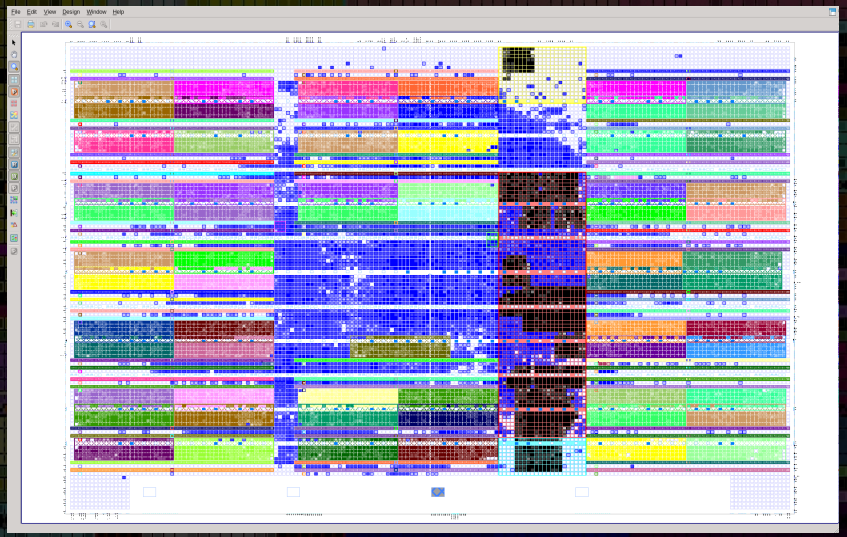
Backup Slides

FEE & 65 Channel TDC



- 64 signals from detector
- Amplification
- Thresholds
- Input signal discrimination
- Time measurement
- Data readout

- Trigger signal is digitised for reference time (65th channel)
- Data readout through 2GBit/s optical link
- 5x16 cm to be plugged on the back of an MCP-PMT
- Very high density for FEE & 65 channel TDC + DAQ + Power
- Tested during the CBM October 2012 test beam
- The Sync message is processed at the internal TRB3-CTS and distributed to 4 FEEs
- Half detector readout with CBMRICH-FEE, other half with nXYTER



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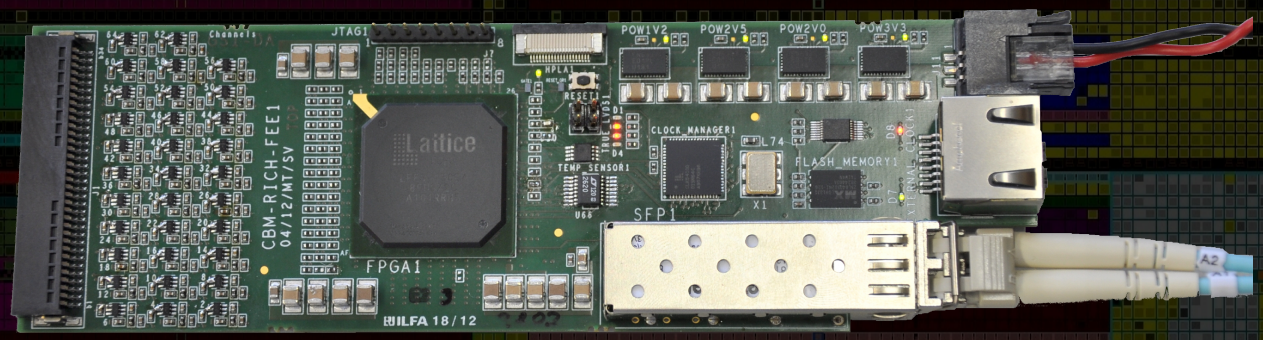

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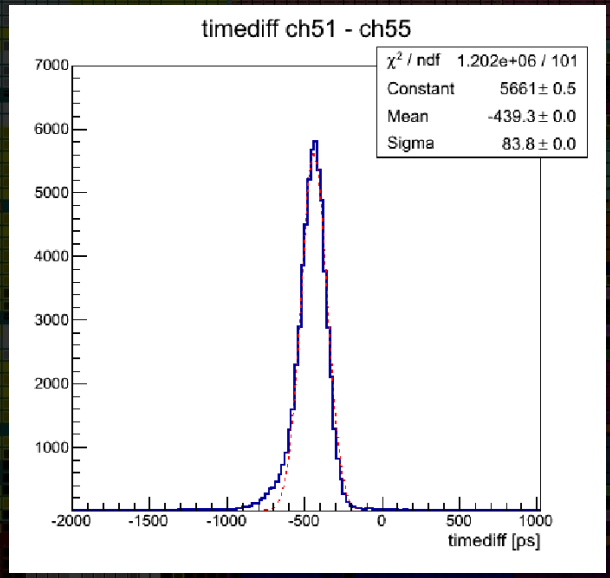
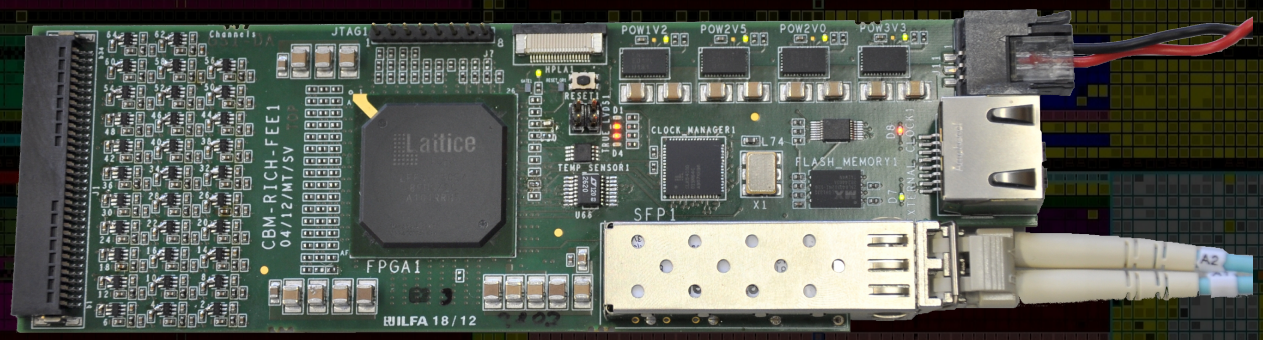


FEE & 65 Channel TDC



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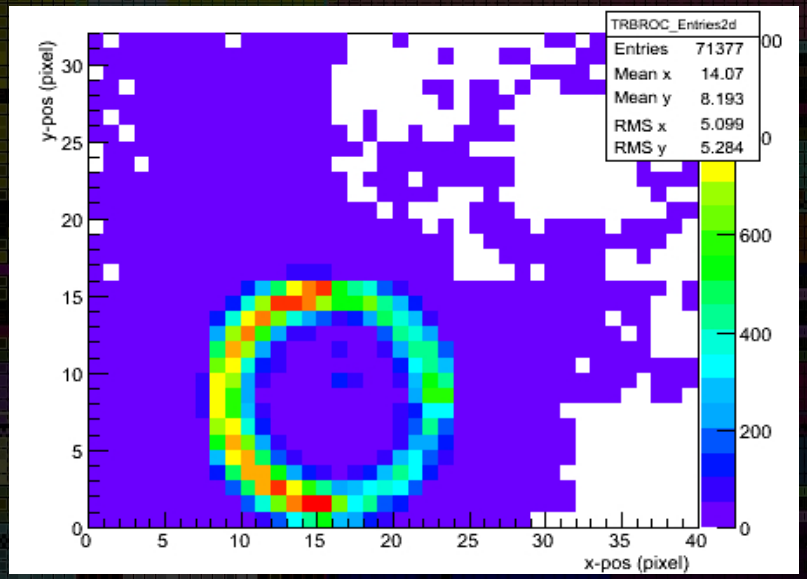
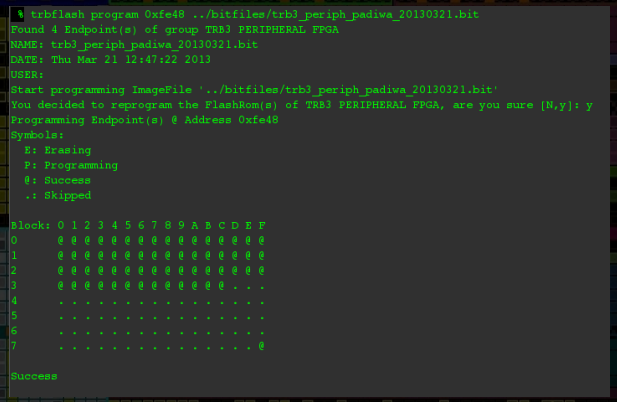
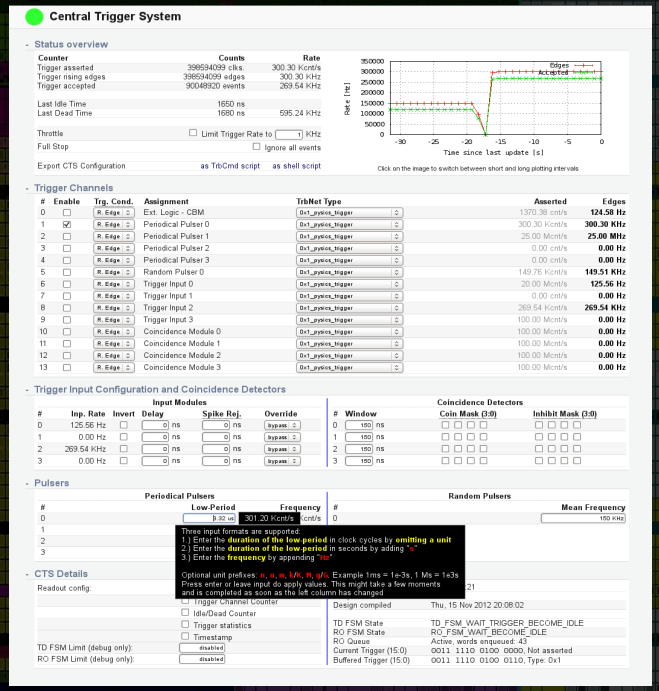


TRB3 Platform: Software

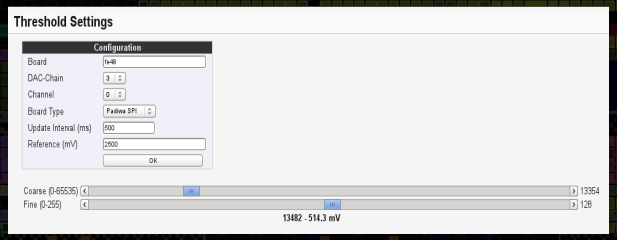
TDC
readout & channel
monitoring & control



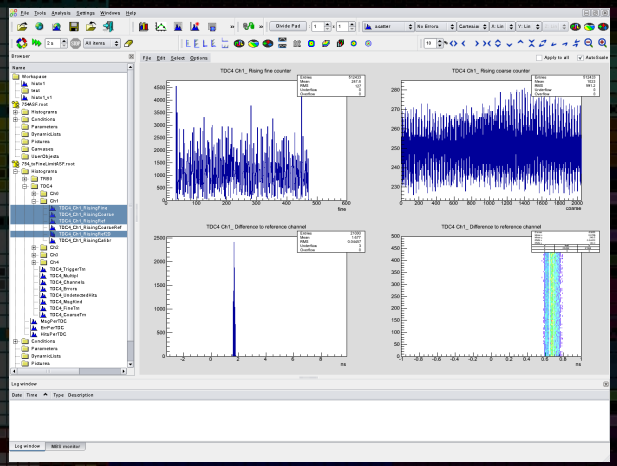
Console based
slow control software
with many features



Trigger
processing & control



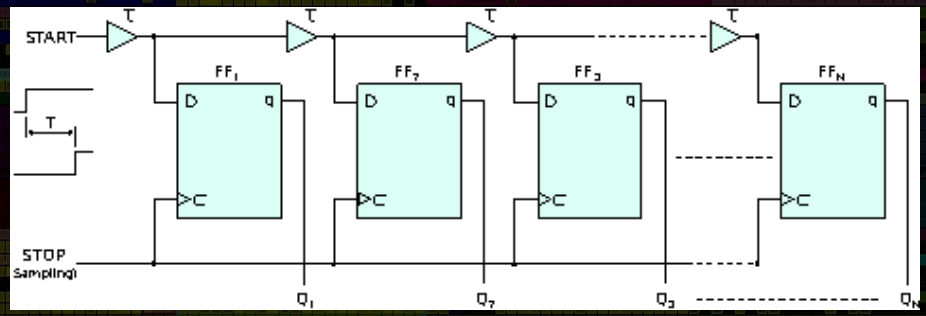
Threshold setting



Unpacking & Online Analysis

Tapped Delay Line Method

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line



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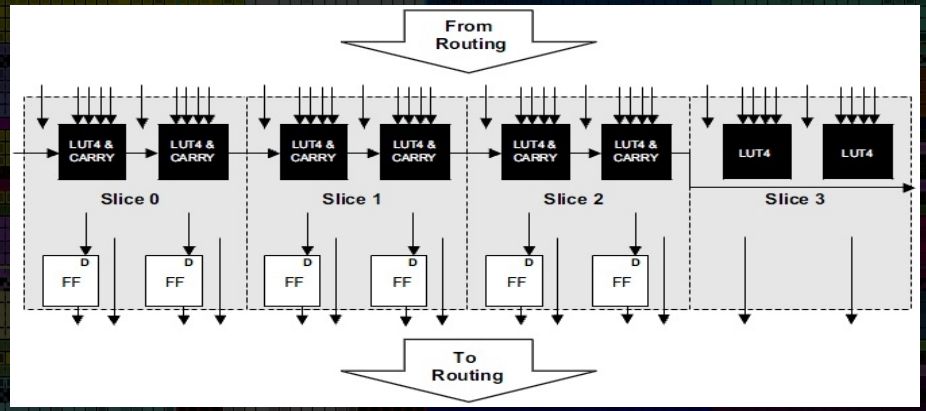
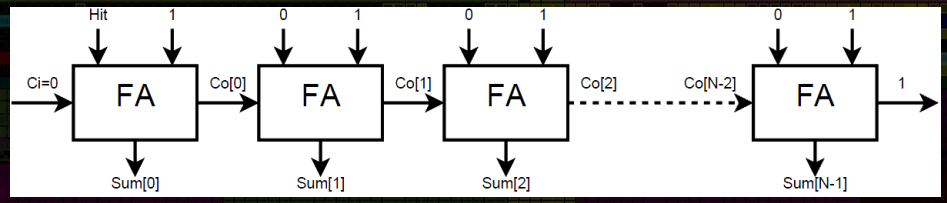
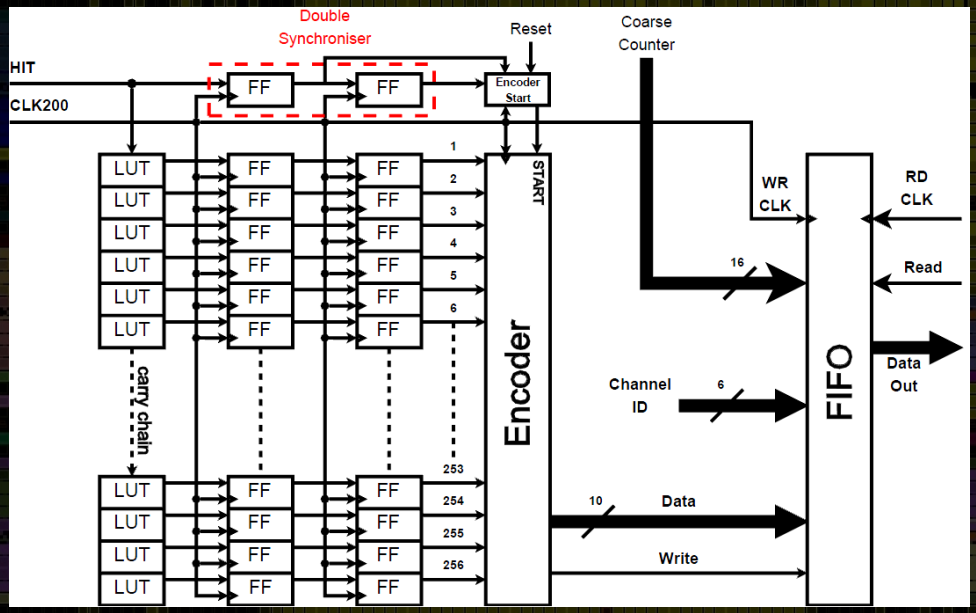


PFU Diagram

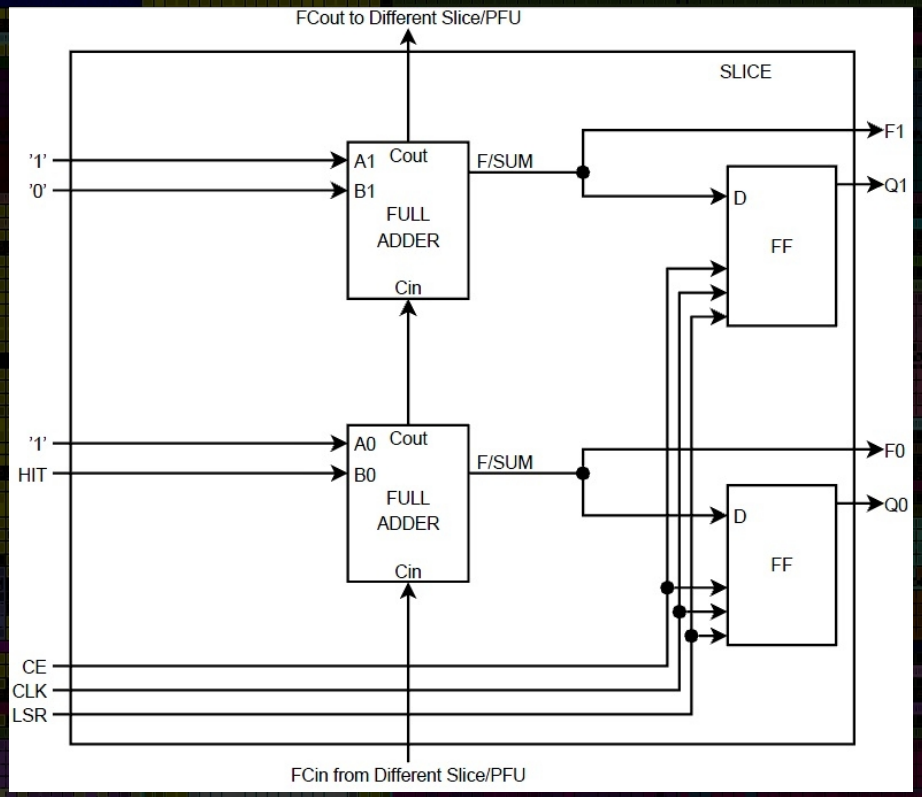
Architecture of the TDC



Delay line is realised with Full Adders [3]



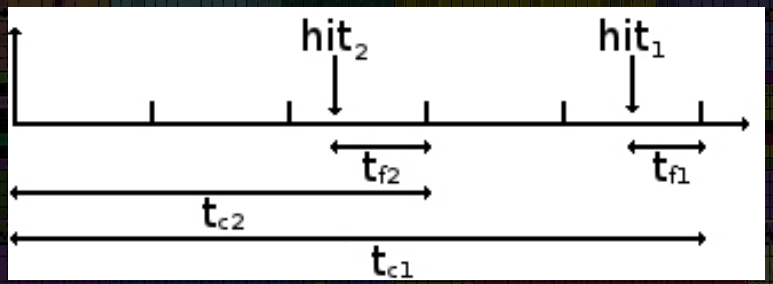
TDC Architecture



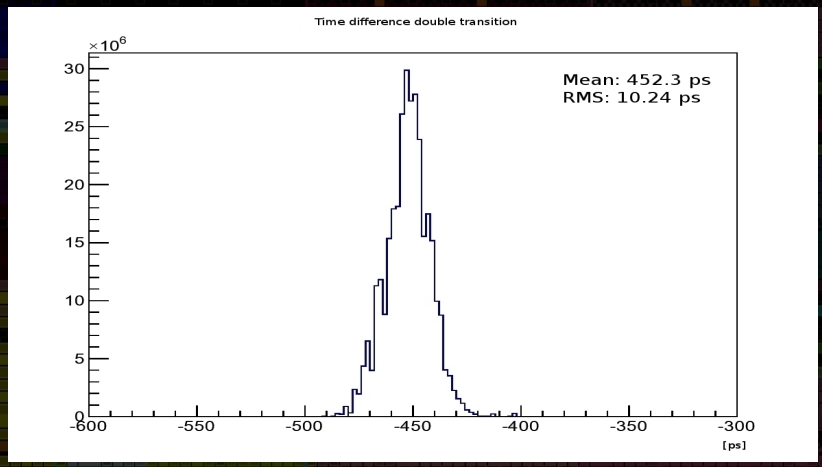
Slice diagram with LUTs programmed as Full Adders

Laboratory Test Results

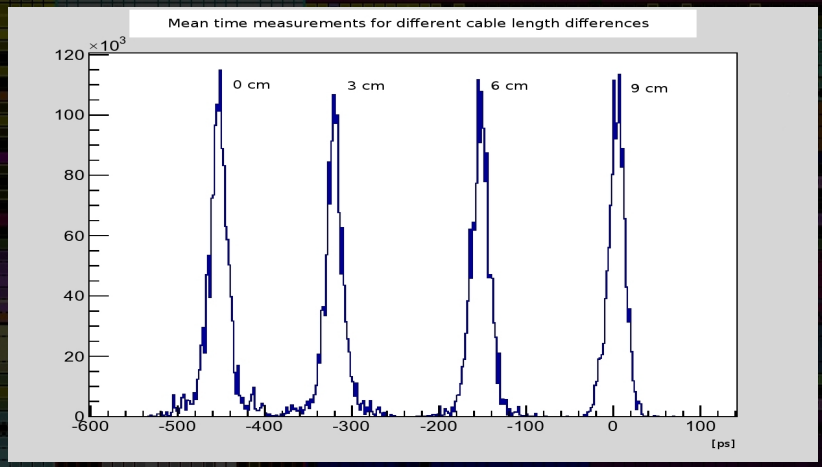
- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps against the same clock
- Precision: 10.34 ps / √2 = 7.3 ps RMS



Time difference between two measurements

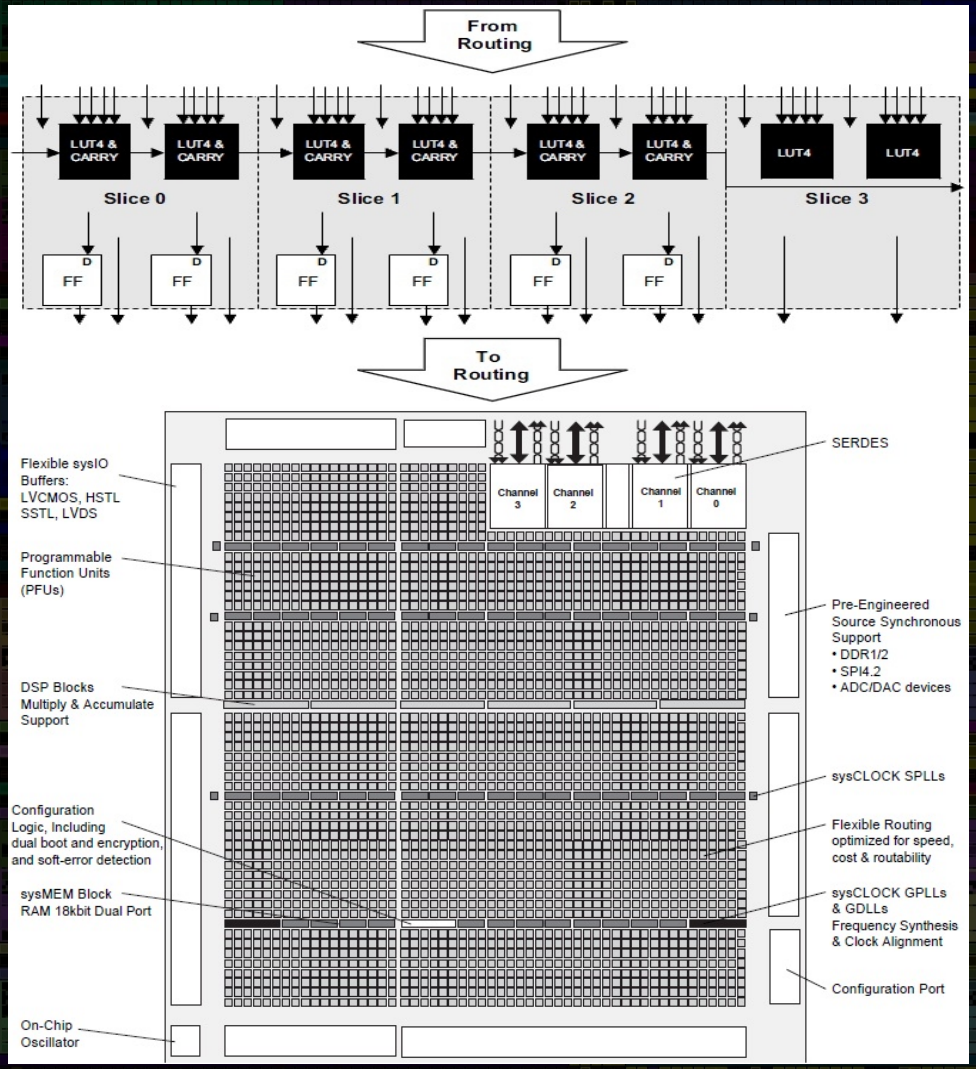


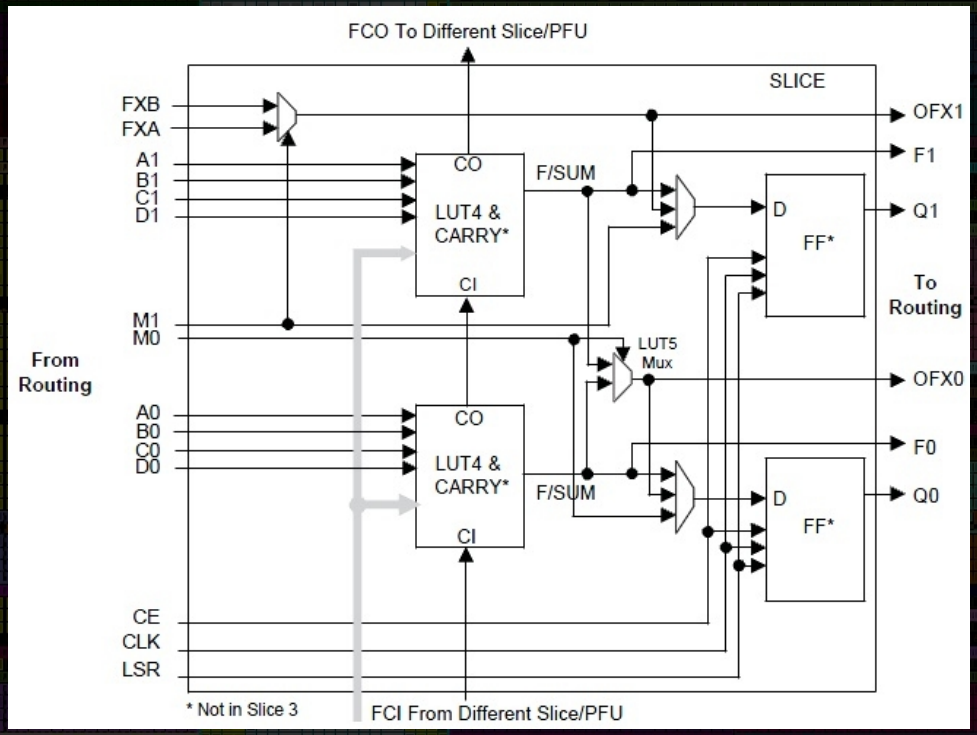
Time precision test



Mean measurement test

Architecture of TDC

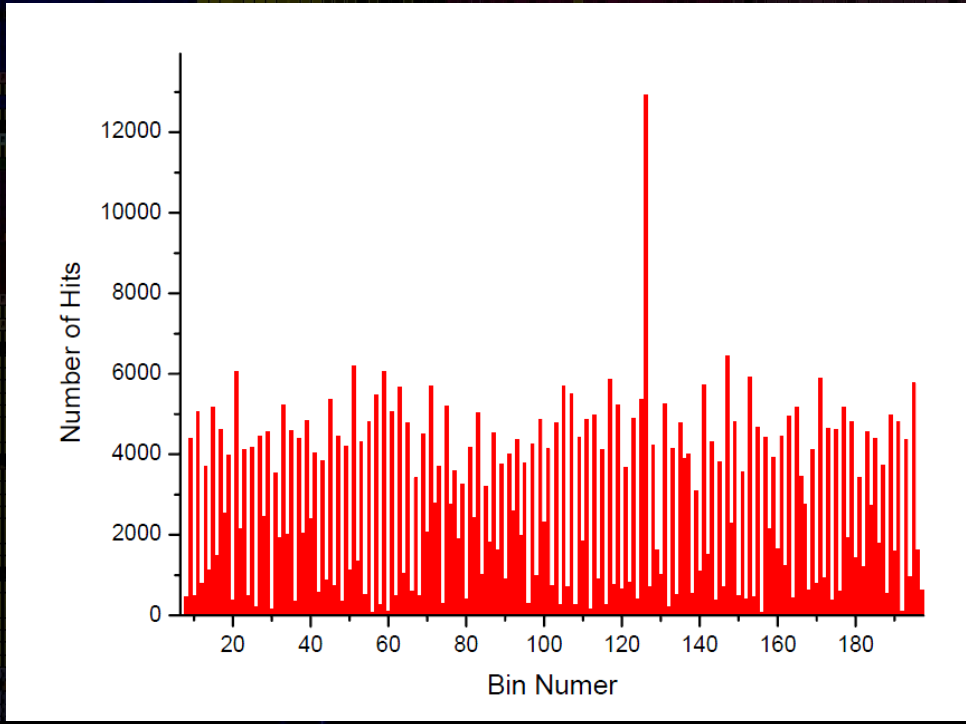




Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floor-plan

Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture



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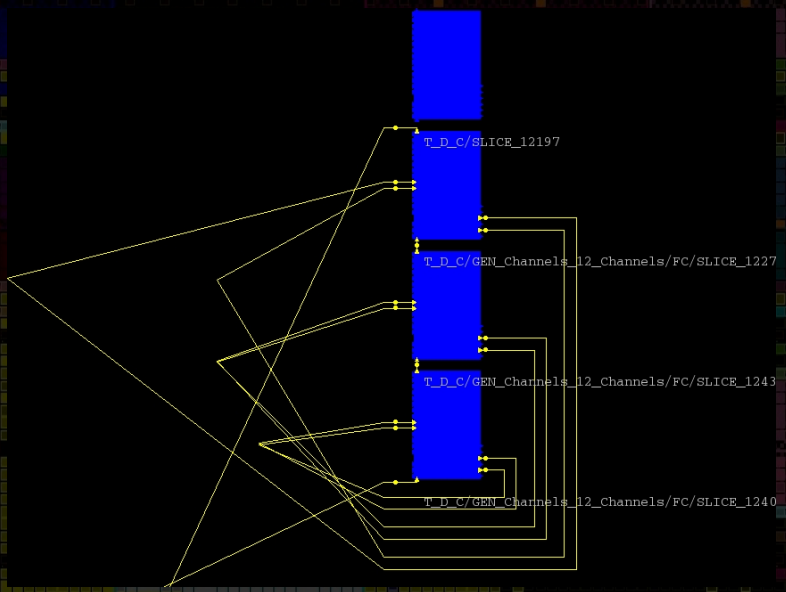
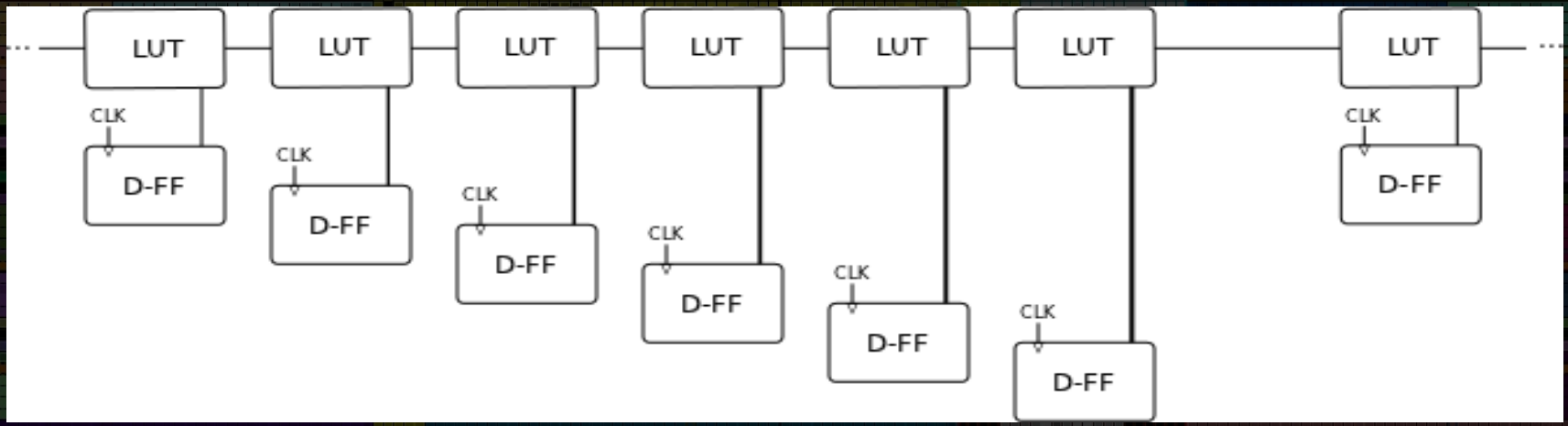
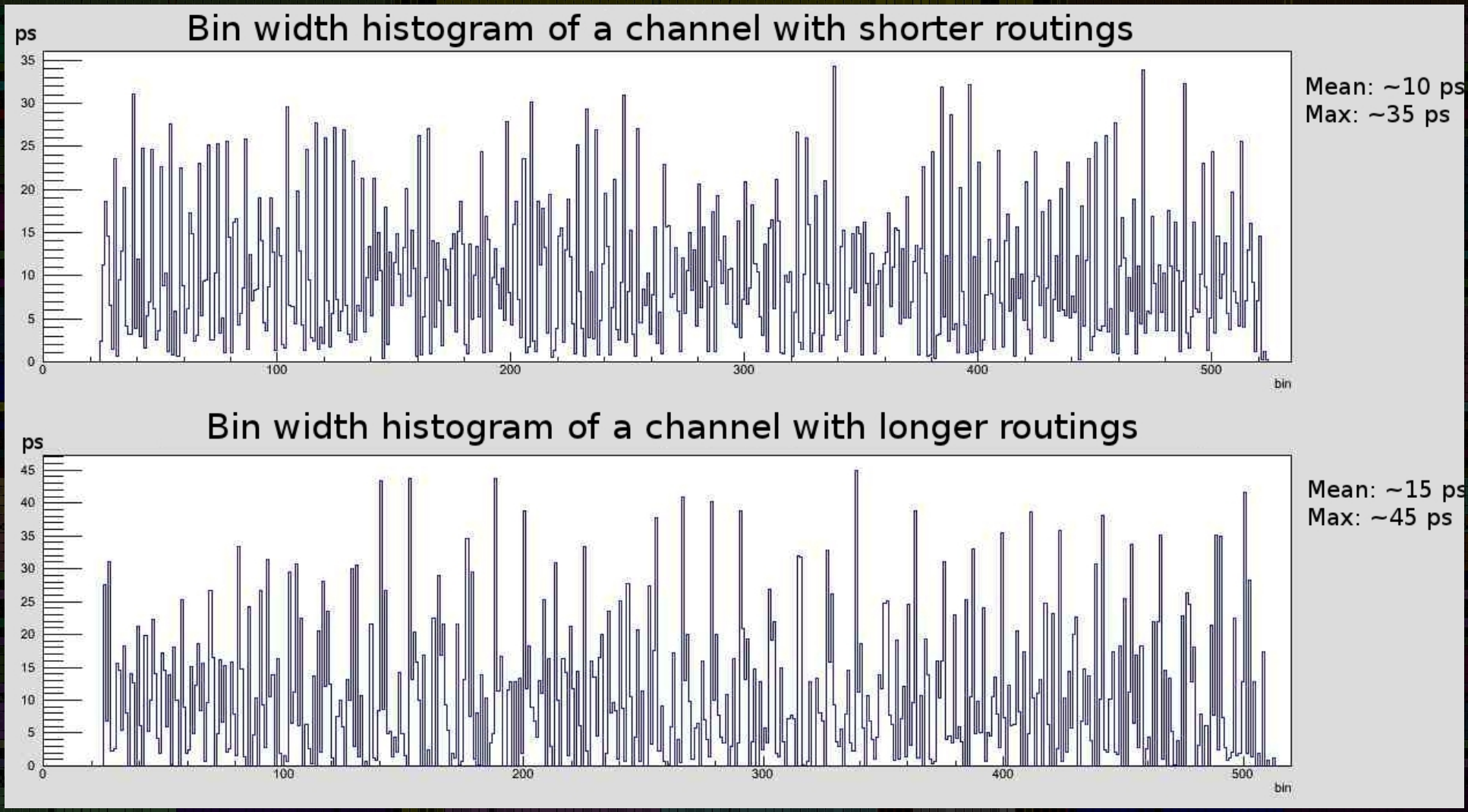




Architectural Effects of FPGA



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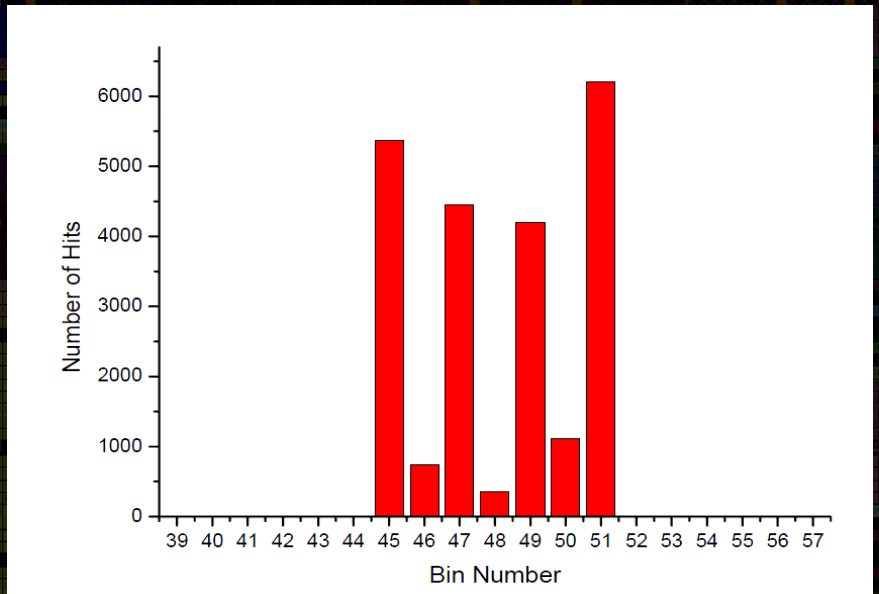
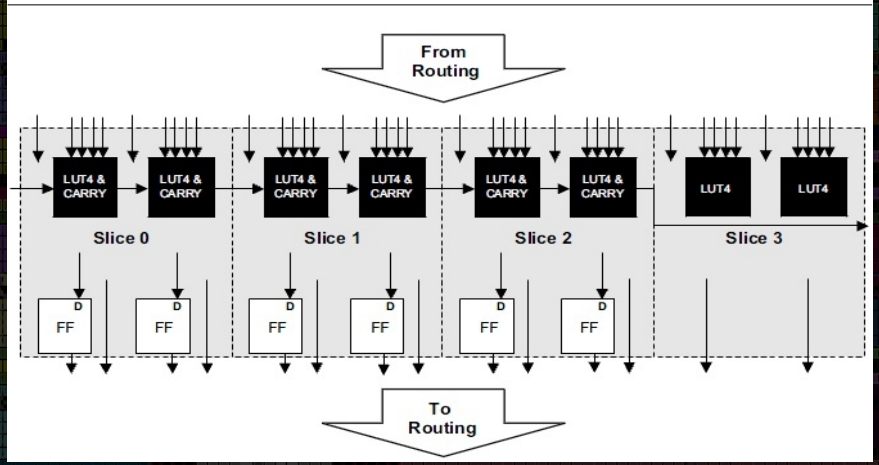
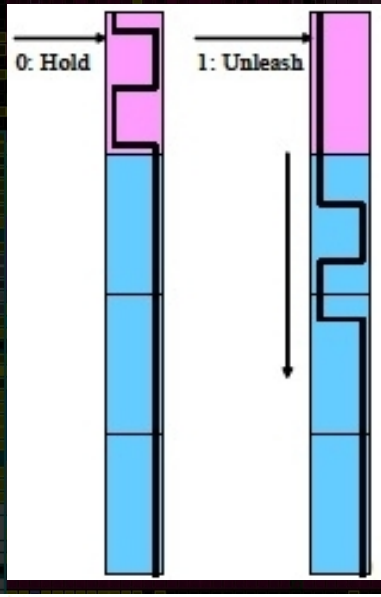
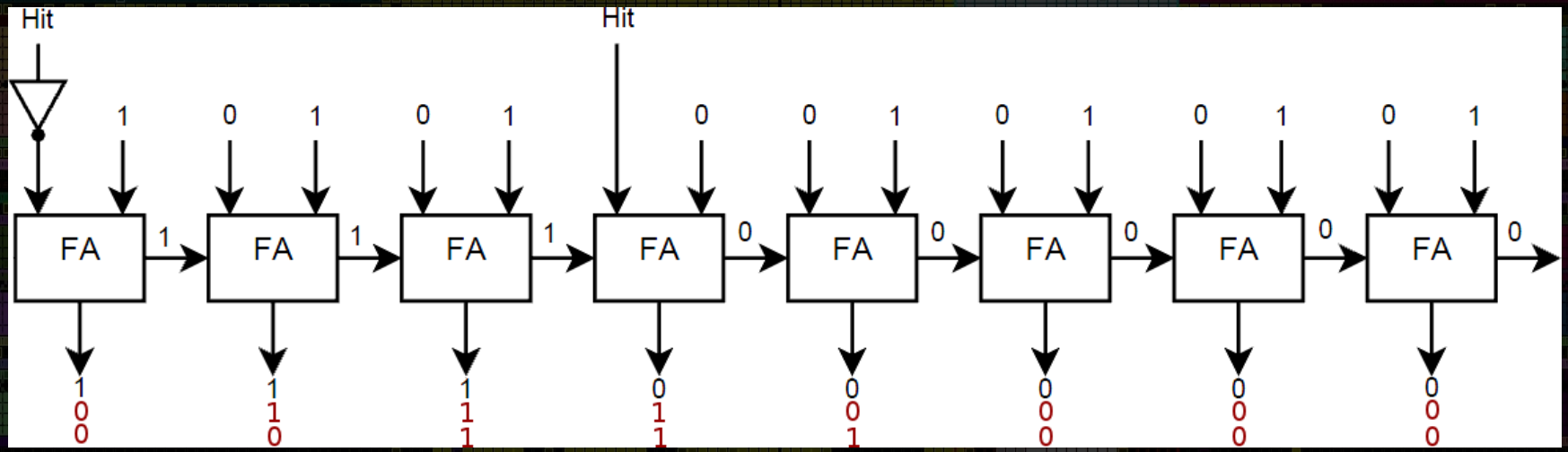




Wave Union Launcher

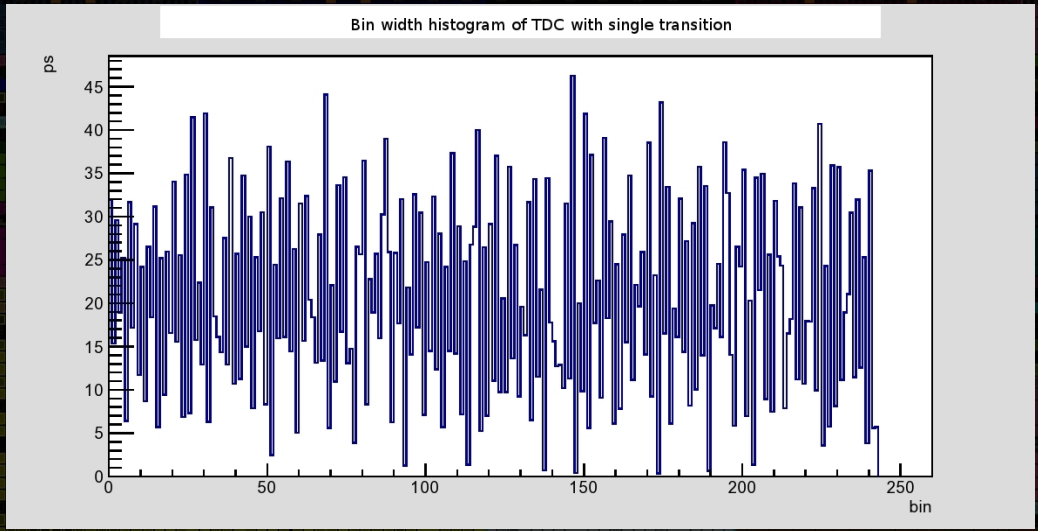
- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced



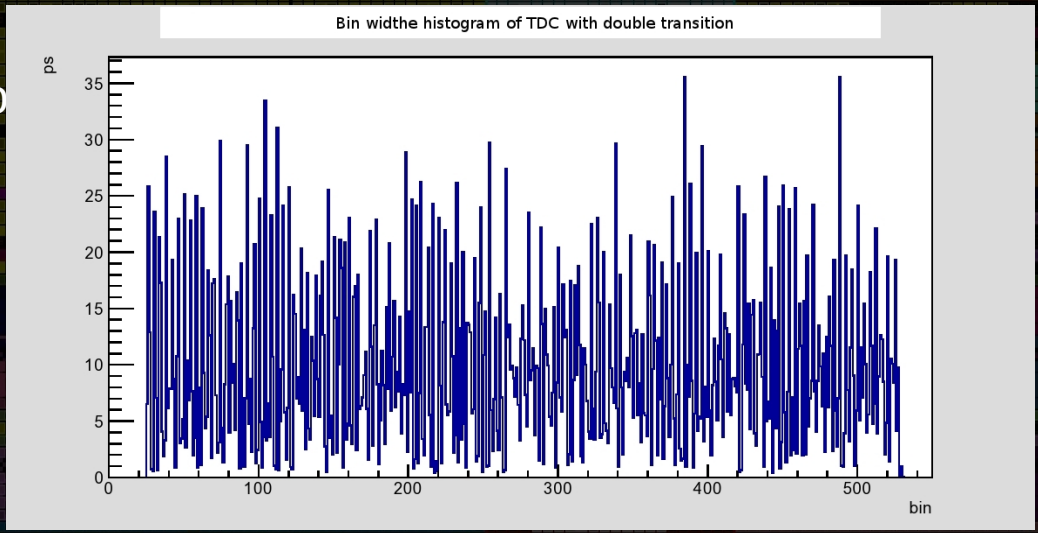


Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distributio



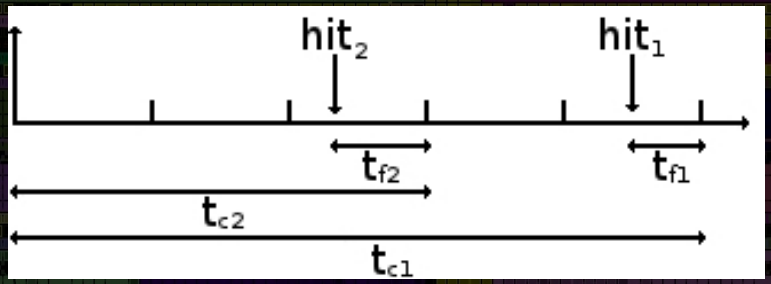
Bins: ~240
Mean: ~20 ps
Max: ~45 ps

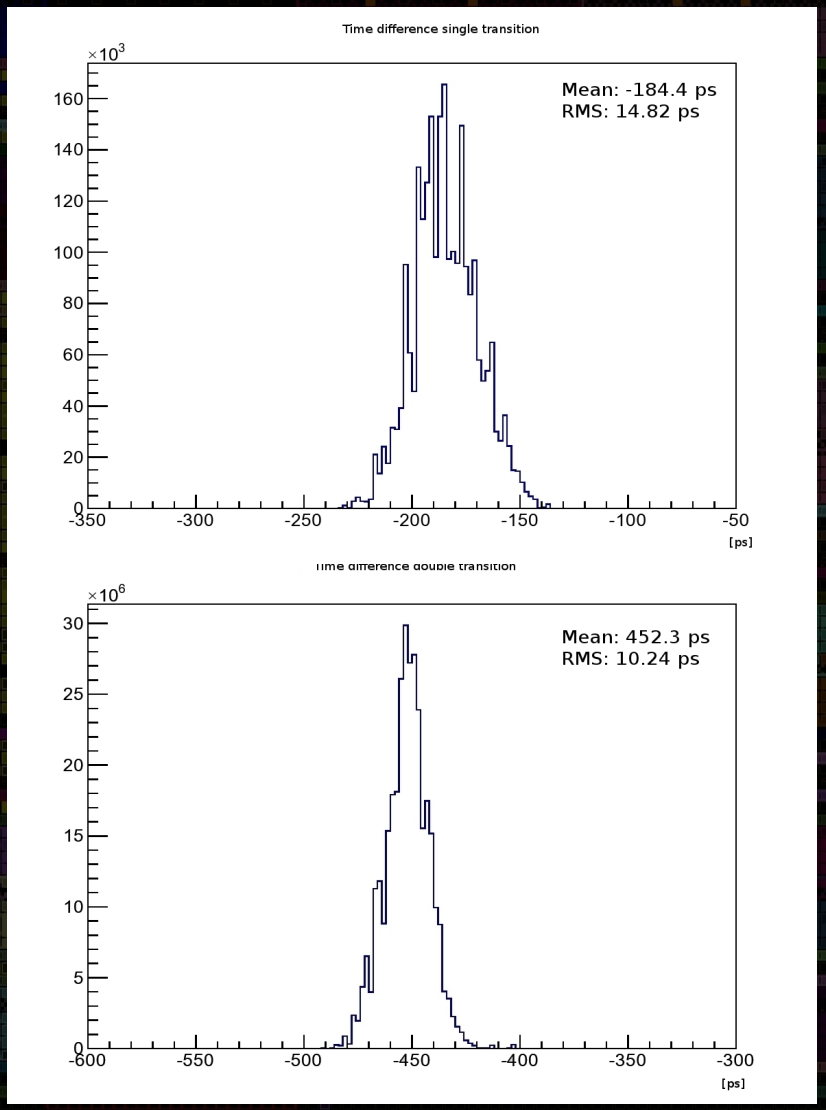


Bins: ~520
Mean: ~10 ps
Max: ~35 ps

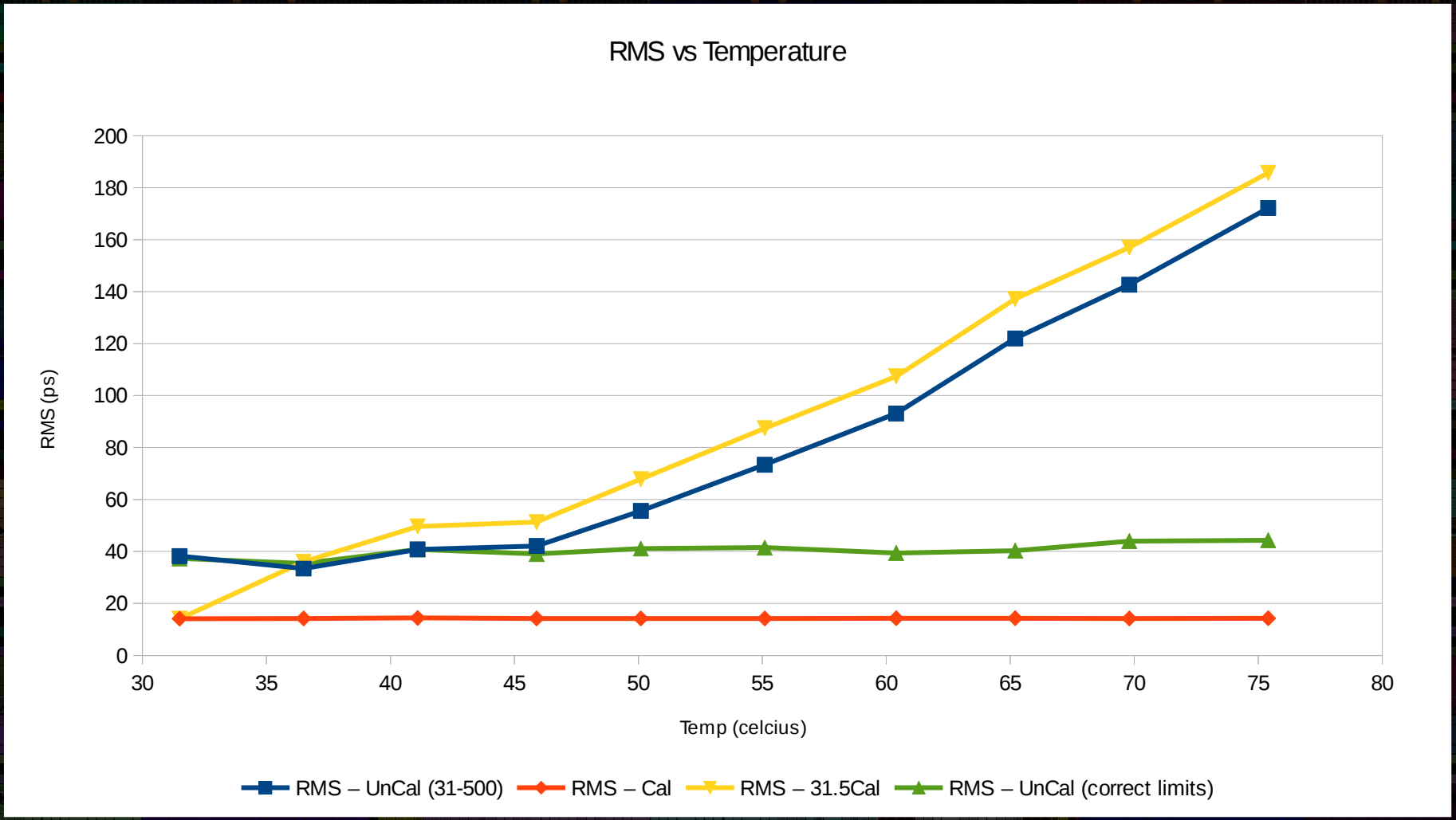
Statistical Error & Precision

- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps against same clock
- Precision: 10.34 ps / √2 = 7.3 ps
- Effect of 2 transitions: 14.82 ps / 10.34 ps = 1.43 factor

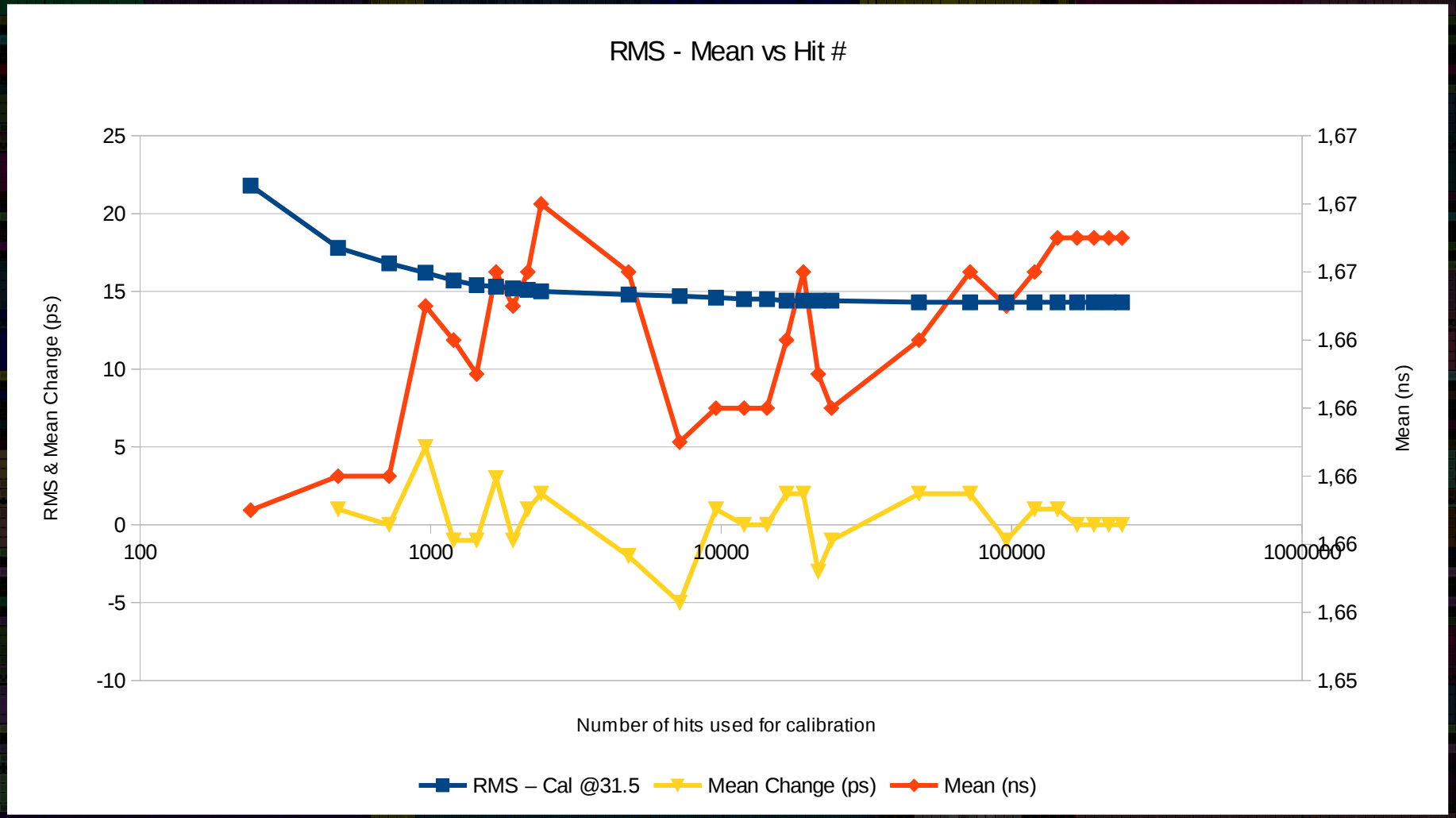




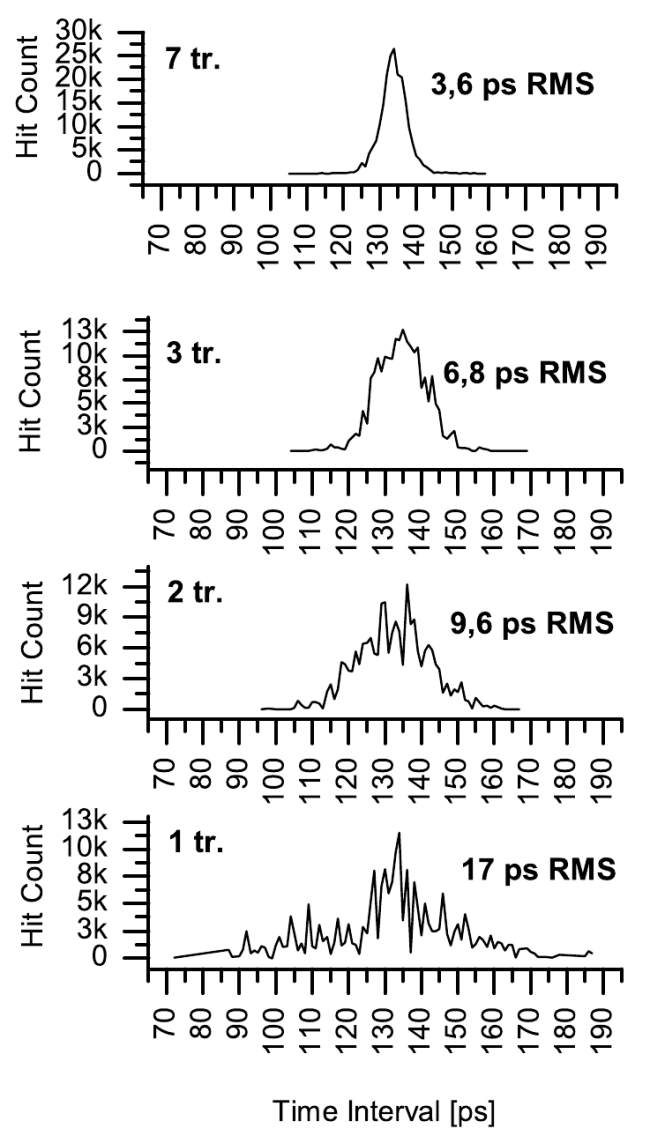
Precision vs Temperature



Precision & Mean vs Statistics



Precise TDCs in FPGAs



Published IEEE 2011, E.Bayer et al.

- TDC time precision down to 3.6 ps [RMS] (between two channels) using the wave union method [Jinyuan Wu] are possible
  - No cut on tails!
- Trade-off for number of channels, time precision and dead time can be adjusted to the needs of the application
  - 65 channels in an FPGA
  - <20 ps RMS time precision on each channel [RMS]