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Real Time Pulse Analyzer for ITER Vertical Neutron Camera

The International Thermonuclear Experiment Reactor (ITER) is a large-scale scientific experiment intended to prove the viability of fusion as an energy source, and to collect the data necessary for the design and subsequent operation of the first electricity-producing fusion power plant. ITER is an experimental nuclear reactor operating with a magnetic toroidal field of 5.3 T, plasma current of 15 MA, pulse duration up to 500 s and producing up to 700 MW fusion power. It is aimed to demonstrate the feasibility of nuclear fusion realization generating DD and DT fusion reactions with characteristic neutrons 2.5 and 14 MeV. The neutron emission profile is measured Vertical Neutron Camera (VNC). ITER VNC requires: 12-bit digitizer with sampling rate from 250 MHz to 1 GHz; count rate up to 10^7 events/s; on-line digital technique for separation and reconstruction pile-up.
Taking into account the above-mentioned specifications Digital Multichannel Analyzer for ITER VNC is based on ADC12500PXIe digitizer. It is developed in our workgroup and included into ITER Catalog of I&C products –Fast Controllers (345X28 v2.3). ADC12500PXIe digitizer is a two-channel waveform recorder with reconfigurable data processing unit, based on FPGA. Each measuring channel built on 12-bit ADC with 500 MHz sampling rate and high frequency bandwidth (0-250 MHz) and has programmable gain and zero line position. Data processing unit was configured for Digital Pulse Analyzer (DPA). DPA performs pulse height analysis using on-line algorithms implemented in the FPGA and waveform registration for debugging and monitoring. Pile-up events are detected and reconstructed using several digital processing algorithms, such as triangular or trapezoidal filter.
Developed software includes three system levels: Linux device driver, EPICS driver, Human Machine Interface (HMI). The Linux device driver conforms to the standard Linux device model in that you access and control the ADC12500PXIe device and Digital Pulse Analyzer. The driver support library provides all the functionality through a relatively small set of easy to use functions (API) that hide all driver ioctl functions and implementation details. The main purpose of EPICS driver is to interconnect HMI with Linux device driver. HMI provides a graphics-based visualization of spectral and waveform data and control of operating modes.

Summary

The International Thermonuclear Experiment Reactor (ITER) is a large-scale scientific experiment intended to prove the viability of fusion as an energy source, and to collect the data necessary for the design and subsequent operation of the first electricity-producing fusion power plant. ITER is an experimental nuclear reactor operating with a magnetic toroidal field of 5.3 T, plasma current of 15 MA, pulse duration up to 500 s and producing up to 700 MW fusion power. It is aimed to demonstrate the feasibility of nuclear fusion realization generating DD and DT fusion reactions with characteristic neutrons 2.5 and 14 MeV. ITER expected neutron emission from 10^{14} up to almost $10^{2}1$ n/s. The neutron emission profile is measured Vertical Neutron Camera (VNC). ITER VNC requires:

- all electronic equipment from ITER Catalog of I&C products;
- multichannel registration;
- common external synchronizing system for all channel registration;
- 12-bit digitizer with sampling rate from 250 MHz to 1 GHz;

- count rate up to 10^7 events/s;
- on-line digital technique for separation and reconstruction pile-up;
- reconfigurable data processing unit.

Taking into account the above-mentioned specifications Digital Multichannel Analyzer for ITER VNC is based on ADC12500PXIe digitizer. It is developed in our workgroup and included into ITER Catalog of I&C products –Fast Controllers (345X28 v2.3).
ADC12500PXIe digitizer is a two-channel waveform recorder with reconfigurable data processing unit, based on FPGA. Each measuring channel built on 12-bit ADC with 500 MHz sampling rate and high frequency bandwidth (0-250 MHz) and has programmable gain and zero line position. The digital part based on FPGA, data RAM and PCI Express x4 Lane Bridge, initialized by the onboard EPROM. PCI Express Bridge has the possibility of FPGA reconfiguration at any time (inc. during operation) and complies with PCI Express Base Specification 1.1 of data exchange operations between PC and FPGA IP application level.
Data processing unit was configured for Digital Pulse Analyzer (DPA). DPA performs pulse height analysis using on-line algorithms implemented in the FPGA and waveform registration for debugging and monitoring. Pile-up events are detected and reconstructed using several digital processing algorithms, such as triangular or trapezoidal filter.
Developed software includes three system levels: Linux device driver, EPICS driver, Human Machine Interface (HMI). The Linux device driver conforms to the standard Linux device model in that you access and control the ADC12500PXIe device and Digital Pulse Analyzer. The driver support library provides all the functionality through a relatively small set of easy to use functions (API) that hide all driver ioctl functions and implementation details. The main purpose of EPICS driver is to interconnect HMI with Linux device driver. Human machine interface (HMI) was developed using Control System Studio (CSS –Eclipse-based collection of tools to monitor and operate large-scale control systems). It is based on Java, which allows users to make the program portable between operating systems (Linux, Windows, Mac OS, etc.). HMI provides a graphics-based visualization of spectral and waveform data and control of operating modes.

Primary author: IVANOVA, Alina (I)

Co-authors: Dr KHILCHENKO, Aleksander (Budker Institute of Nuclear Physics); Mr KOTELNIKOV, Aleksander (Budker Institute of Nuclear Physics); Mr KVASHNIN, Andrey (Budker Institute of Nuclear Physics); Mr SKOPINTSEV, Dmitry (Troitsk Institute for Innovation and Fusion Research); Ms PURYGA, Ekaterina (Budker Institute of Nuclear Physics); Mr ZUBAREV, Peter (Budker Institute of Nuclear Physics); Ms IVANENKO, Svetlana (Budker Institute of Nuclear Physics); Mr AMOSOV, Vladimir (Troitsk Institute for Innovation and Fusion Research)

Presenter: IVANOVA, Alina (I)

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