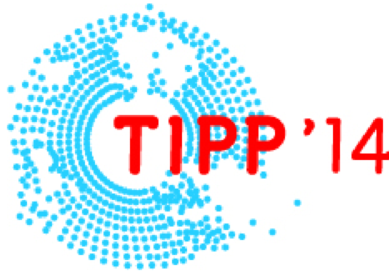

Contribution ID: **182** Type: **Poster**

A radiation hardness CMOS layout by only changing procedure of a layer

The impact from radiation to complementary metal-oxide semiconductor (CMOS) circuit which is used as read out circuit for high energy experiments or space satellite has been categorized into two problems: Total ionizing dose (TID) reflecting the long-period-time effects exists and the other is the single event effects (SEE) characterizing short time result. TID effect makes threshold voltages shifted and leakage current of NMOS transistors in CMOS device increase, especially. Thus, a number of layout methods are implemented. For example, enclosed layout transistor (ELT) has radiation hardness against TID effects while it has large implementation area, complicated effective W/L ratio, and asymmetric source and drain capacitance. It makes circuit design difficult. Other technique except ELT needs additional layer to exploit or careful design to eliminate short problem by silicide process. However, we presented simple and powerful radiation hardness layout method which needs only layer procedure change. It has been implemented using 0.18 μm CMOS process. Traditional NMOS, proposed NMOS, and ELT will be tested by using Co-60 gamma ray source up to 30 Mrad and compared about leakage current, noise at input gate, and threshold voltage shift.

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Track Classification: Experiments: 2b) Astrophysics and Space Instrumentation