Performance of Three Dimensional Integrated Circuits Bonded to Sensors

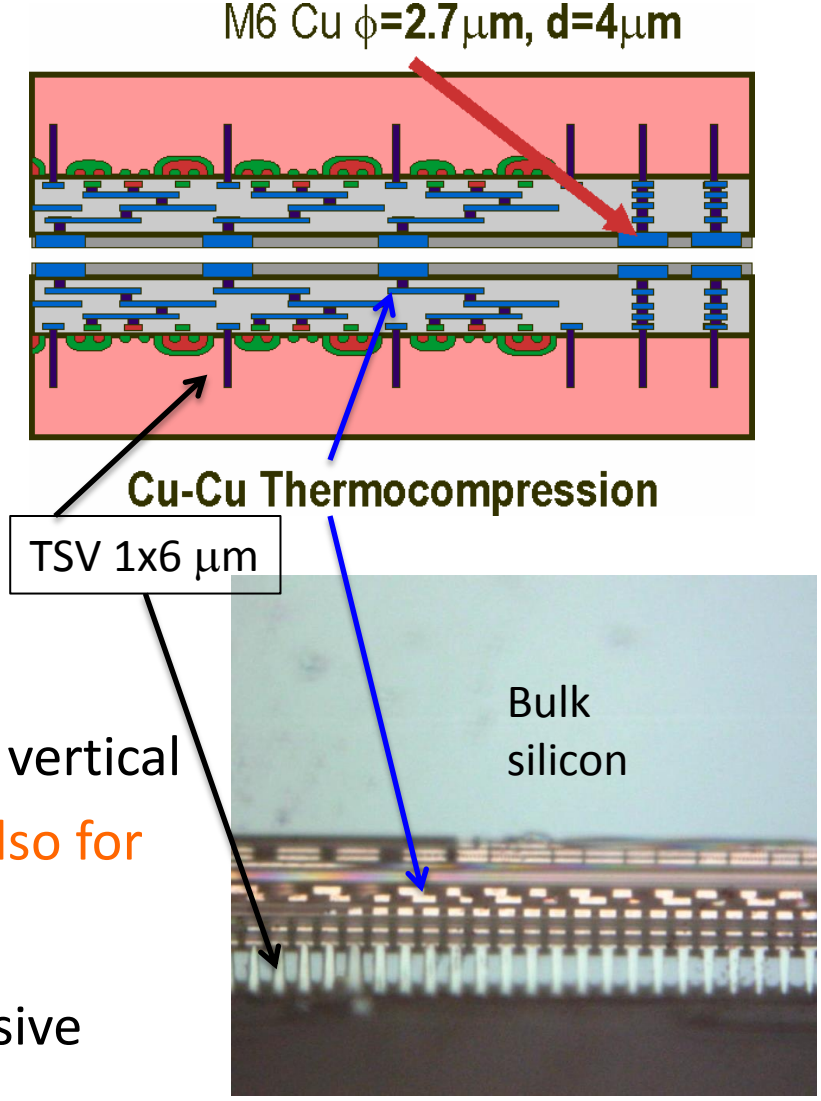
Ronald Lipton, Fermilab

This talk will summarize results of our work to explore integration of sensors and electronics based on “3D” (multi-tier) technology.

- 3D Technology
- Processes and Designs
- Two-tier electronics results
- Results of integration of electronics with sensors
- Development of tiled arrays
- Conclusions

G. Deptuch, R. Yarema, P. Grybos, R. Szczygiel, M. Trimpl ,J. Hoff, J. Thom, P. Wittich, Z. Ye , A. Shenai, P. Siddons, G. Carini, M. Tripathi, U. Heintz, M. Narain, R. Lipton, T. Zimmerman, S. Holm, S. Poprocki

3D Integrated Circuits



A three-dimensional integrated circuit (3D-IC) structure is composed of two or more layers of active electronic components using horizontal intra-tier and vertical inter-tier connectivity. Component Technologies

- Through Silicon Vias (TSV): small diameter vertical connectivity - not only to build chips but also for attaching detectors to readouts
- Bonding: Oxide-, polymer-, metal-, or adhesive
  - Wafer-Wafer, Chip-Wafer or Chip-Chip
- Wafer thinning
- Back-side processing: metallization and patterning

3D For Particle Physics

Why is 3D technology interesting for HEP? – We care about bonding sensors to complex analog/digital electronics

- It enables intimate interconnection between sensors and readout circuits
- It enables unique functionality with innovative circuit/sensor topologies
  - Separate digital/analog/ and data communication tiers
  - Multi-layer micro/macro pixel designs which can provide high resolution with minimal circuitry
- Wafer thinning enables low mass, high resolution sensors
- Bonding technologies enable very fine pitch, high resolution pixelated devices
- Commercialization of 3D and wafer-wafer bonding can reduce costs for large areas

R&D Choices

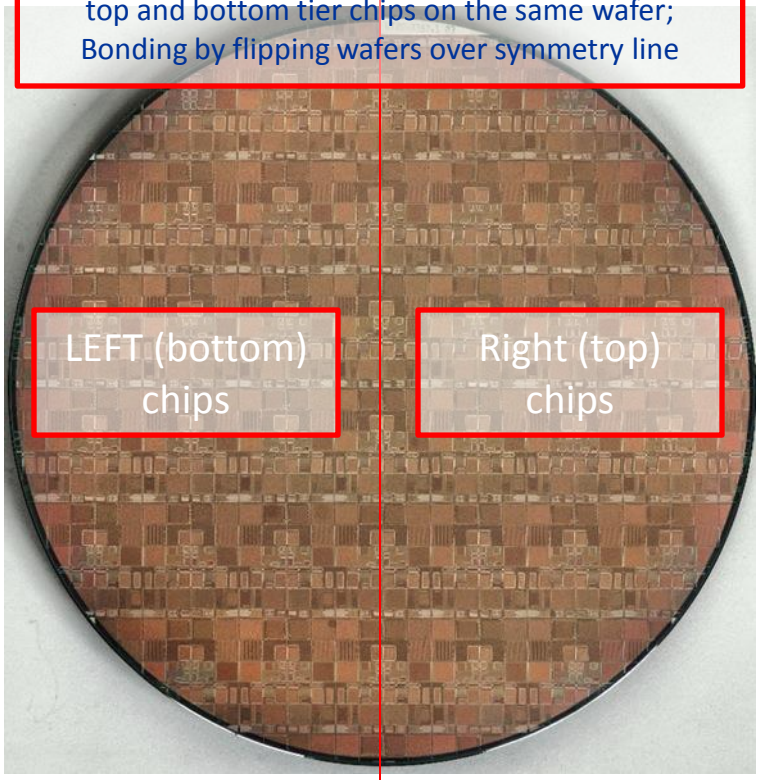
- Technologies on the menu (US):
  - Oxide bonding/0.18 m SOI (MIT-LL)
  - Direct oxide bonding (Ziptronix, Novati/Tezzaron) – IMEC
  - Cu stud (RTI, IBM)
  - Via middle (Tezzaron), via last (MIT-LL)
- Initiatives in the US:
  - DARPA funded studies - Technologies, software,cooling, multiproject runs from MIT-LL, Tezzaron
  - MIT-LL, Tezzaron/Novati, IBM, Ziptronix, RTI, Allvia …

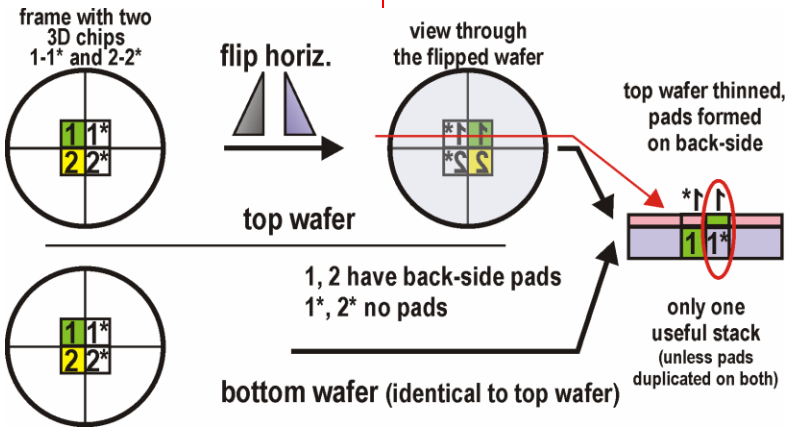
Our initial work was with MIT-LL (VIP-1). We then moved to a "commercial" technology.

‘Fermilab’ 3D-IC run

- 3D-IC Consortium established in late 2008, now 17 members; 6 countries: USA, Italy, France, Germany, Poland, Canada) + Tezzaron – *various goals among members.*
- Fermilab organized first 3D-IC MPW run for HEP
- Designs in: 05/2009; Chartered (GF) 130nm
  - Fermilab had a role of silicon broker
  - Many challenges in working with cutting edge technology: design mistakes, incompatibility of software tools (Tezzaron not Cadence), lack of 3D oriented verification, handling of databases >10GB, shifting GF requirements (DRC), changing personnel at GF, slow progress through fab etc.
- MPW frame accepted for fab in 03/2010
- 3 FNAL chips VICTR(CMS), VIP(ILC) and VIPIC(x-ray)

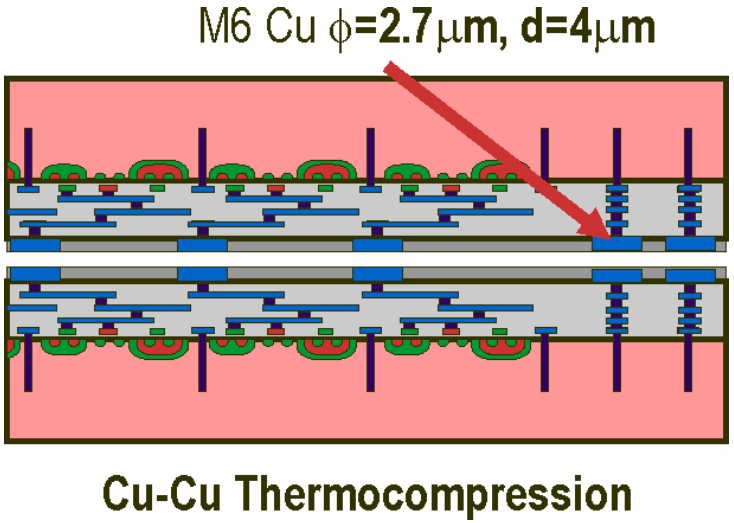
130nm GF/Tezzaron wafer - FNAL MPW before 3D bonding; single mask set used to fabricate top and bottom tier chips on the same wafer; Bonding by flipping wafers over symmetry line



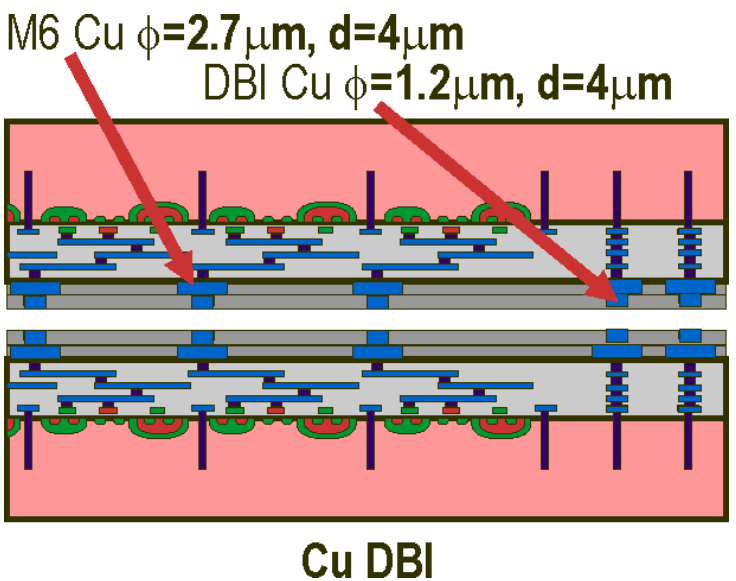


‘Fermilab’ 3D-IC run

Tezzaron / Novati

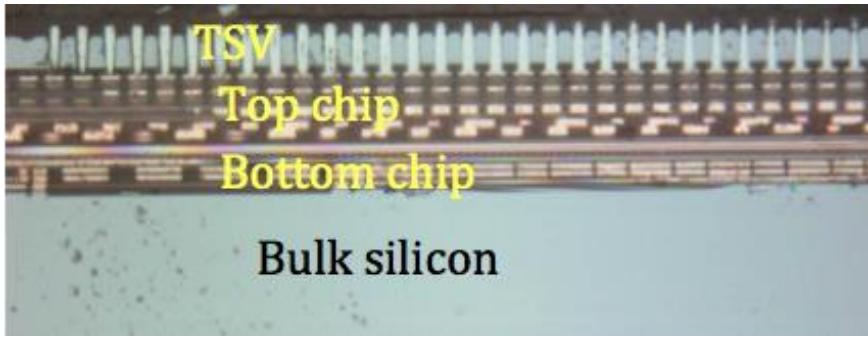


Ziptronix / licensed to Novati



- Difference between Cu-Cu thermocompression and Cu DBI wafer bonding methods:
  - Cu-Cu not reworkable, bonding established by fusing metal pads, forgiving on surface planarity
  - Cu DBI reworkable shortly after bonding, bonding established by chemically fusing oxide surfaces, must be ultra planar

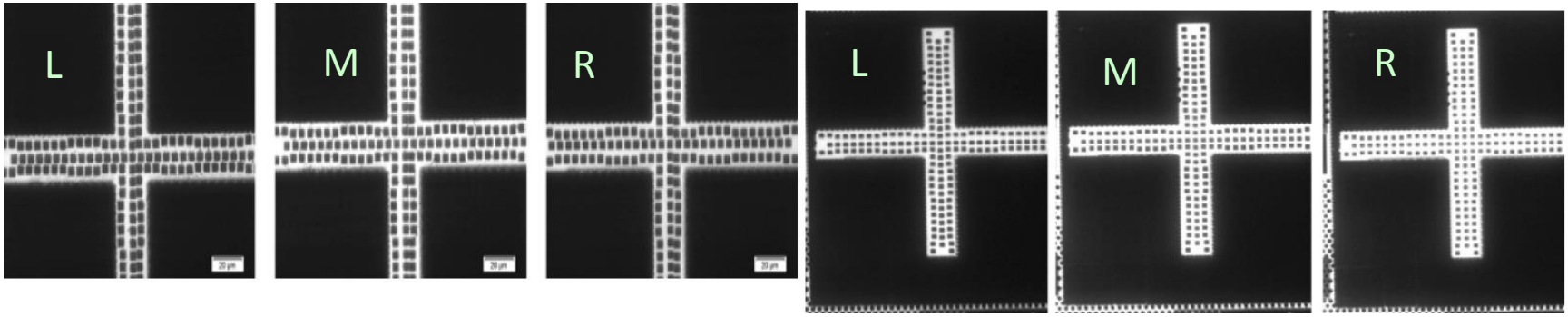
3D Process Development



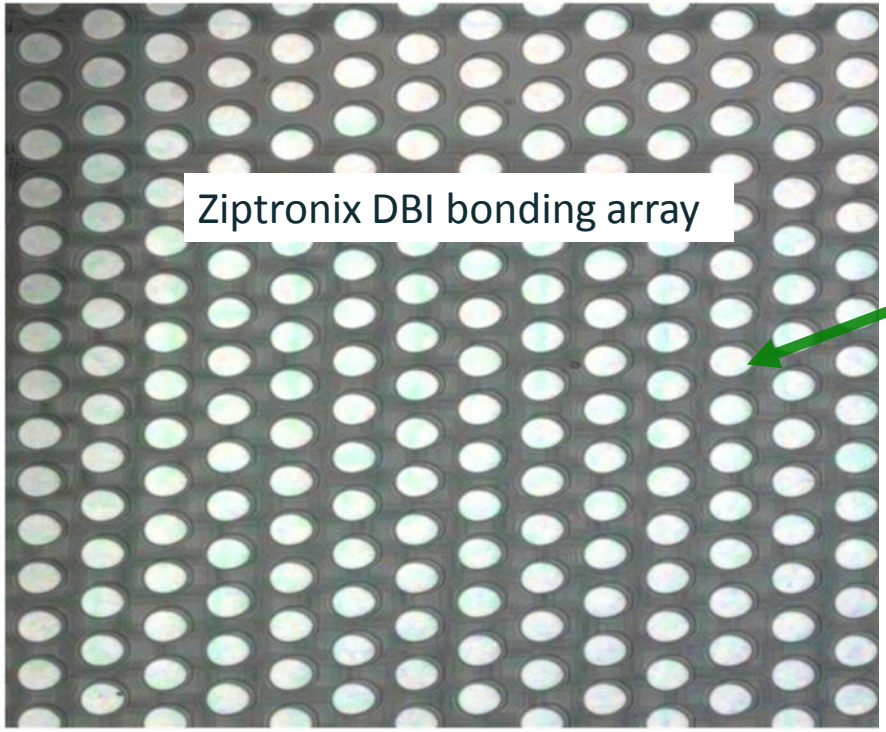
Misaligned Bond Interface in Cu-Cu bonded wafer

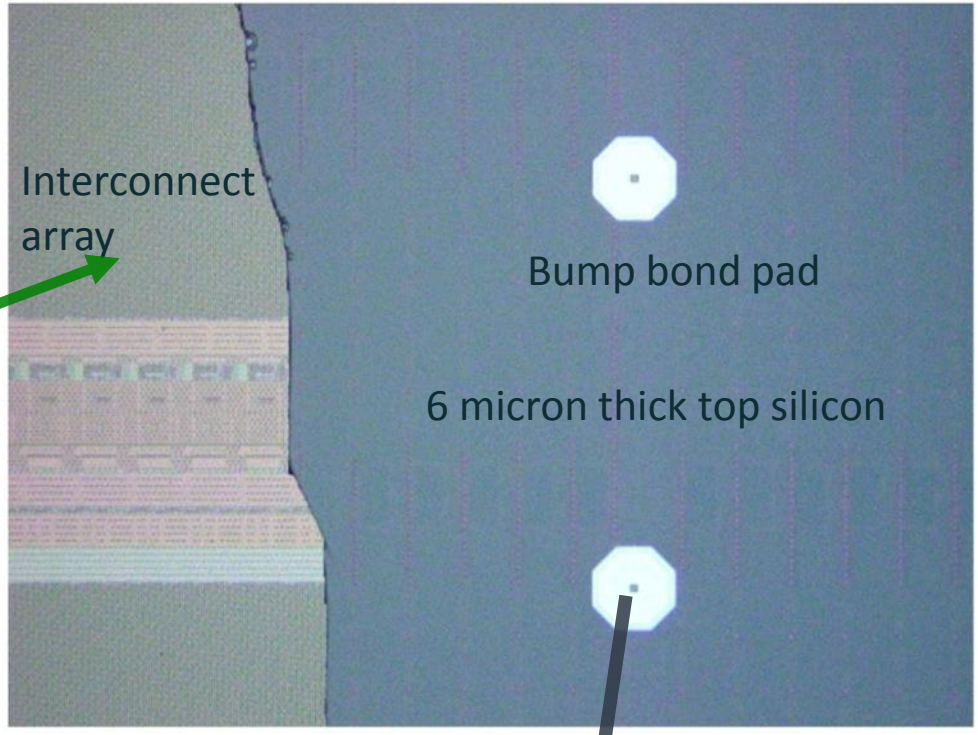
The original cu-cu bonding technique developed by Tezzaron had several issues

- Aging of top copper
- Wafer misalignment
- (Too) Aggressive design rules - 2.7 μm octagons on a 4 μm pitch
  - alignment between wafers must be better than 1 um
- The DBI-oxide bonding process solved these problems.



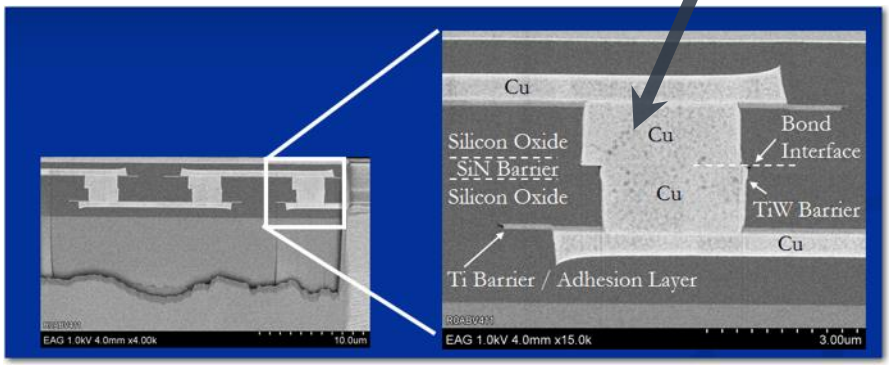
Cu-Cu **Alignment Keys** DBI

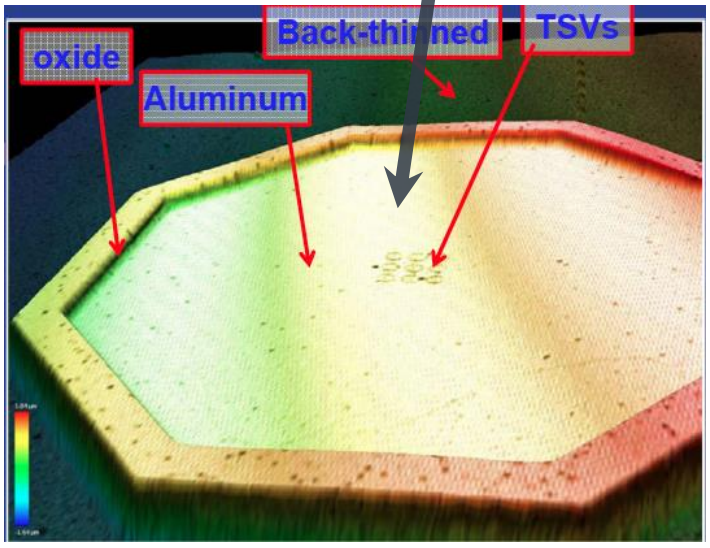




4 micron pitch

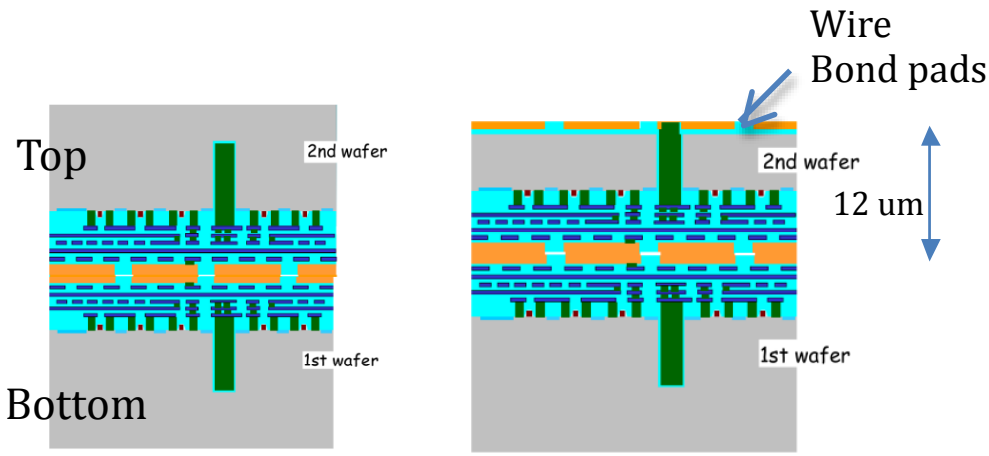
DBI Copper pillars

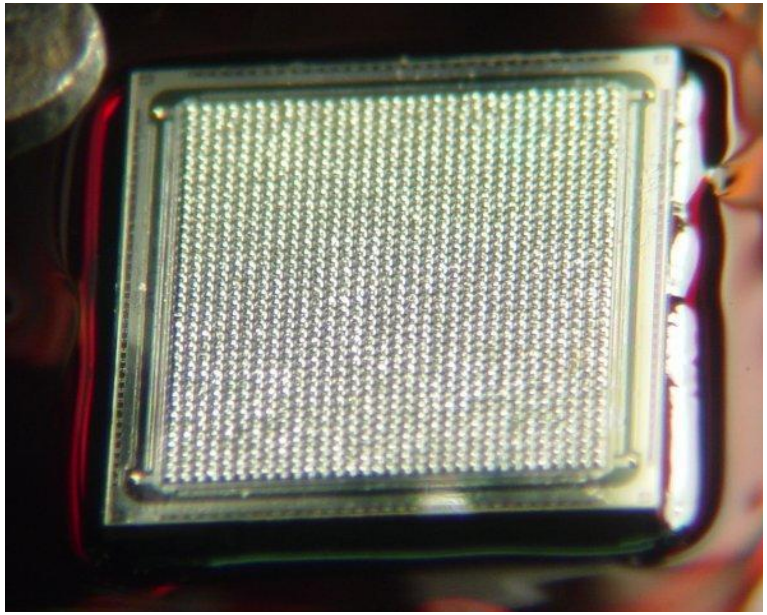




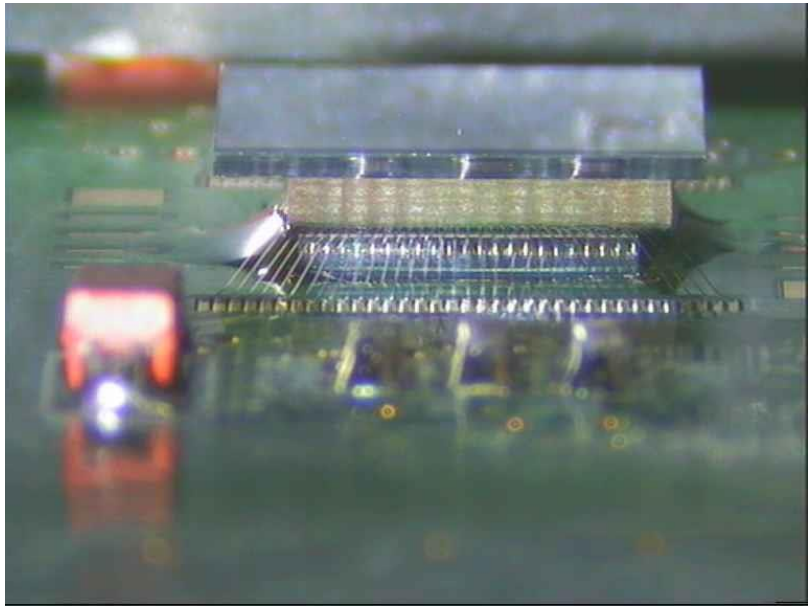
Two-Tier Devices

- Final two-tier (no sensors) wafers were delivered in 2013
- VICTR and VIPIC wafers were tested, both bare and with bump bonded sensors.





VIPIC with bumps

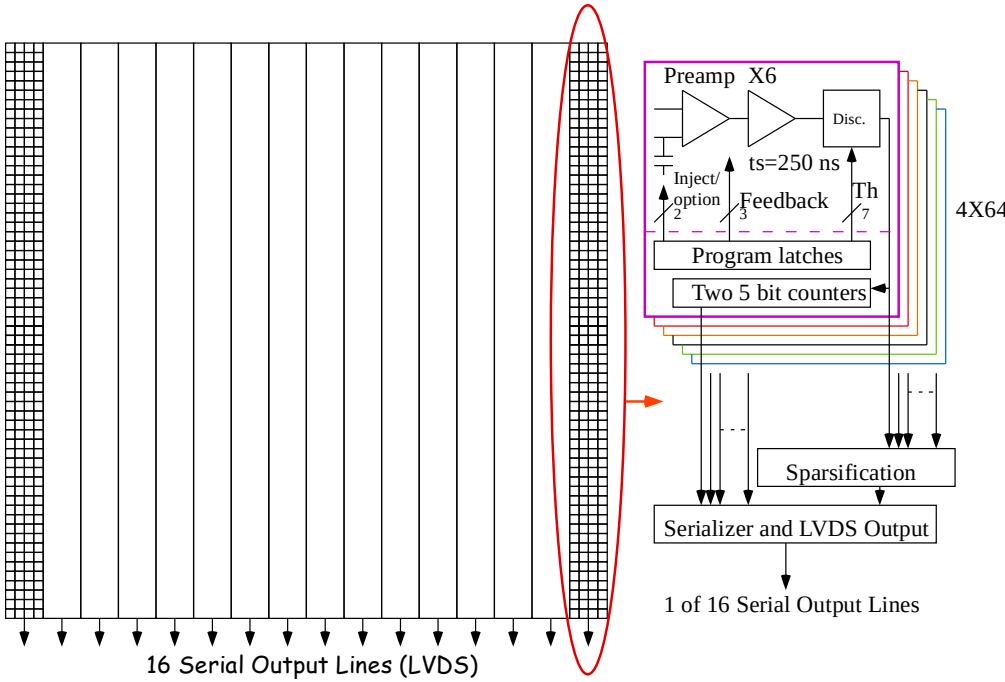


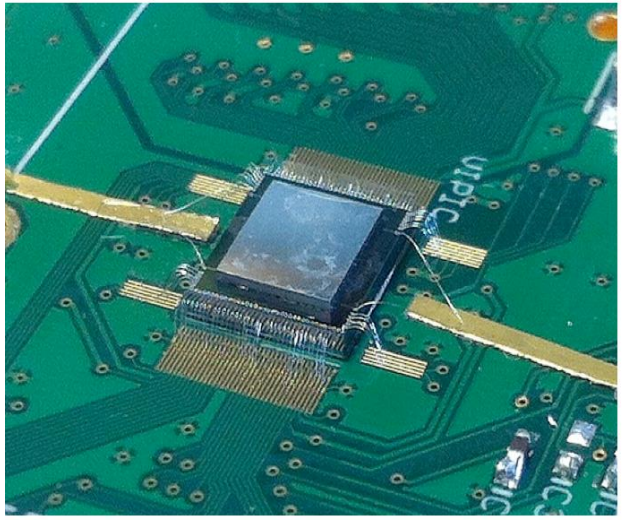
VICTR with top sensor and interposer

Two-tier results -VIPIC

VIPIC is a chip design for X-ray photon correlation spectroscopy with deadtimeless readout

- Separate analog/digital tiers
- 25 inter-tier connections/pixel (64x64 80 μ pixels)





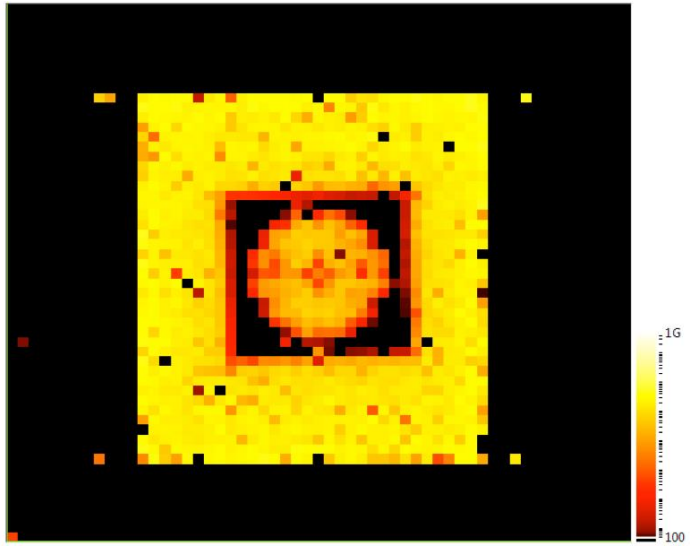
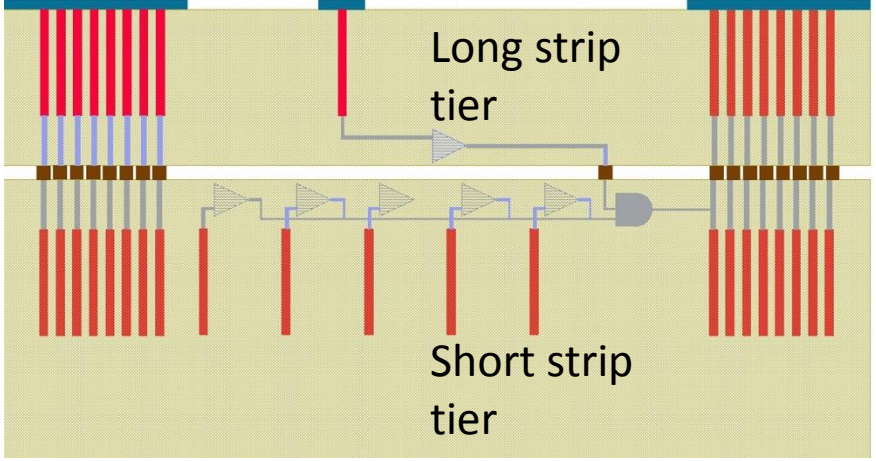


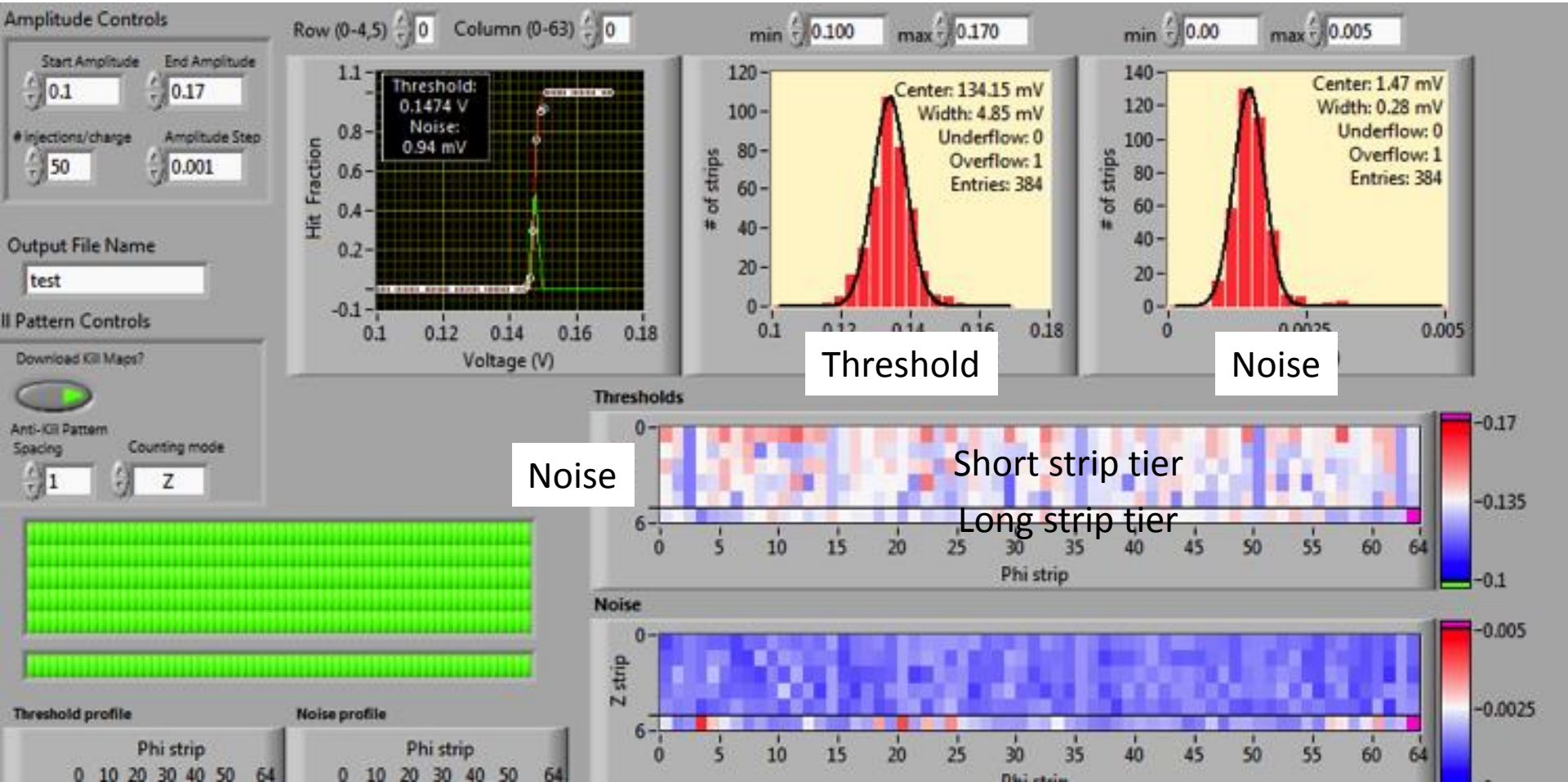
Image with bump bonded sensor

Two-tier results - VICTR

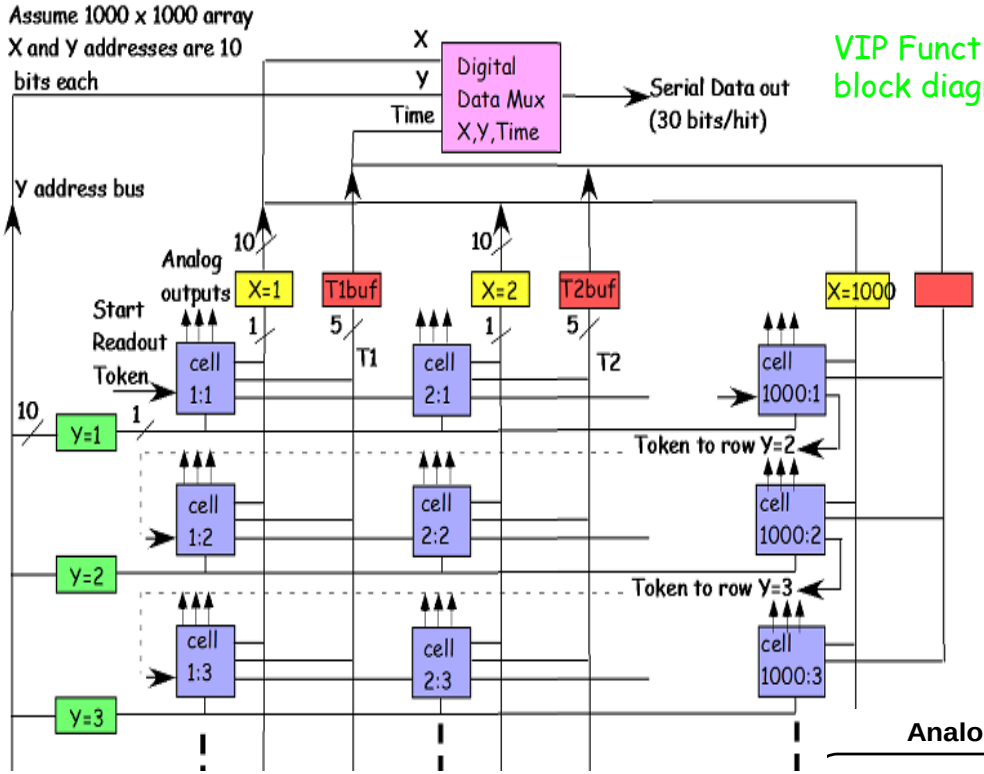
VICTR chip is designed for CMS track trigger applications – correlating hits in long and short strip tiers

- **64 5 mm top tier “long strip”**
- **64 x 5 array 1 mm bottom tier “short strip”**
- **Modified FEI4 (Atlas) front end**





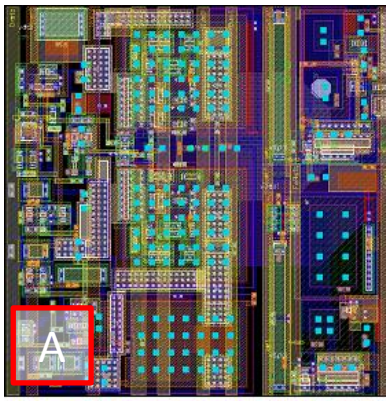
Two-tier Results– VIP2b

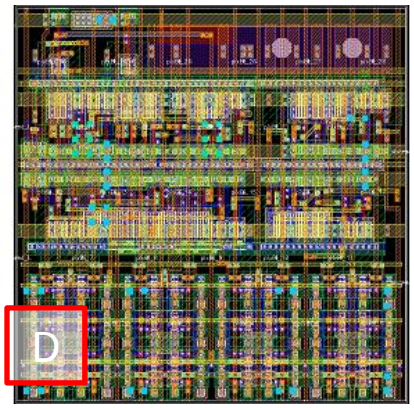


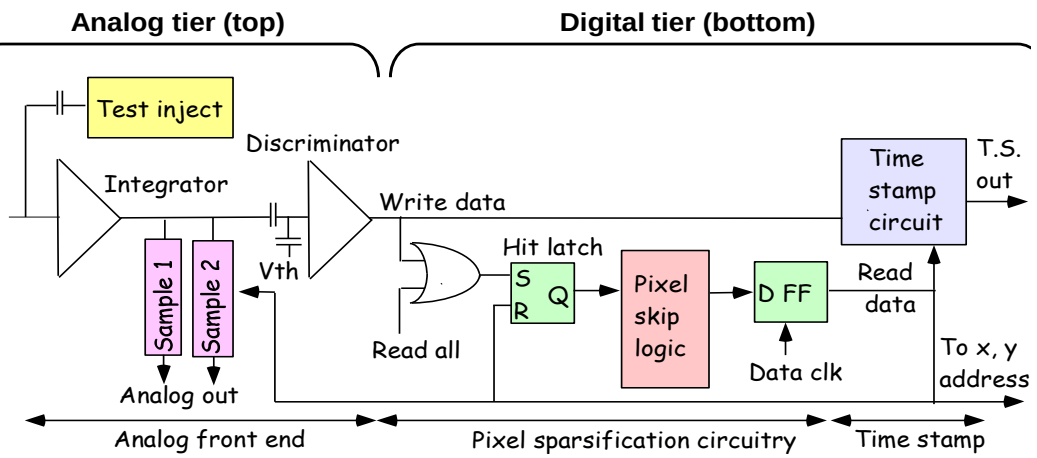
VIP Functional block diagram

– **How it works:**

- 192 × 192 array of 24x24 μm² pixels
- 8 bit digital time stamp (Δt=3.9 μs)
- Readout between ILC bunch trains of sparsified data
- Sparsification - token passing scheme
- Single stage signal integrating front-end with 2 S/H circuits for analog signal output with CDS
- Analog information available for improved resolution
- Serial output bus
- Polarity switch for collection of e^- or h^+





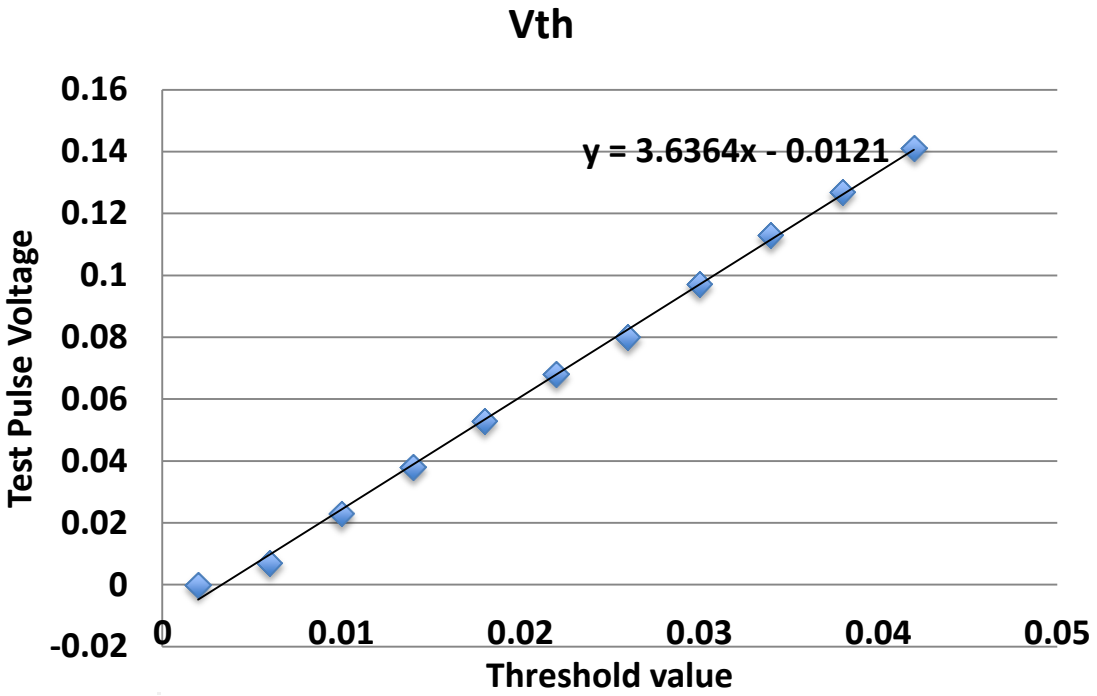


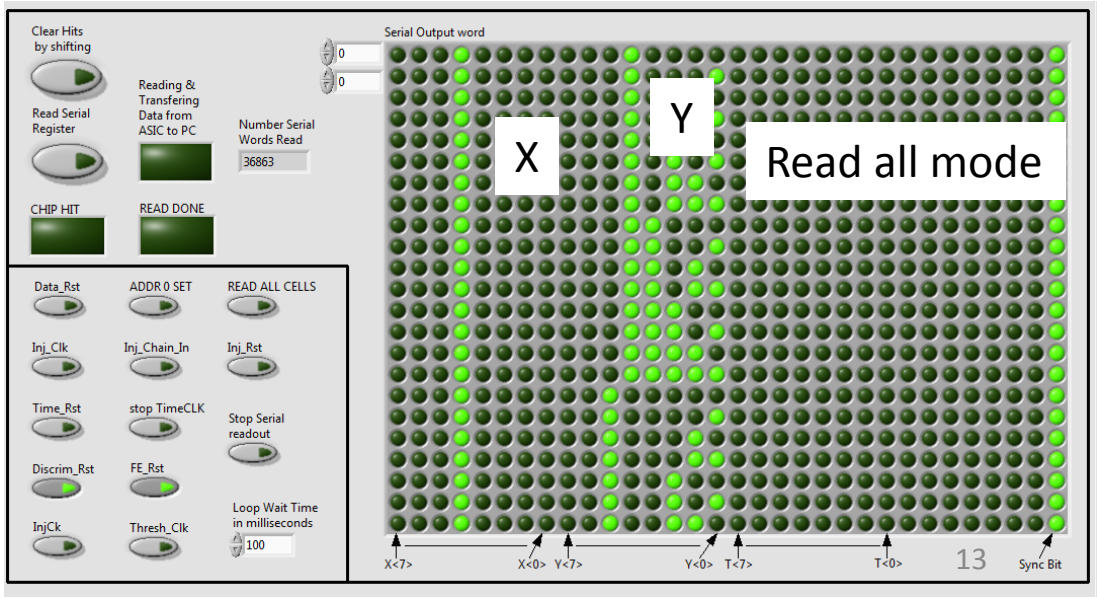
VIP Testing

- Successfully read out all 192x192 = 36,864 pixels
- Token passes though at 189 ps/pixel

Possible issues with pixel masking, odd row test pulse

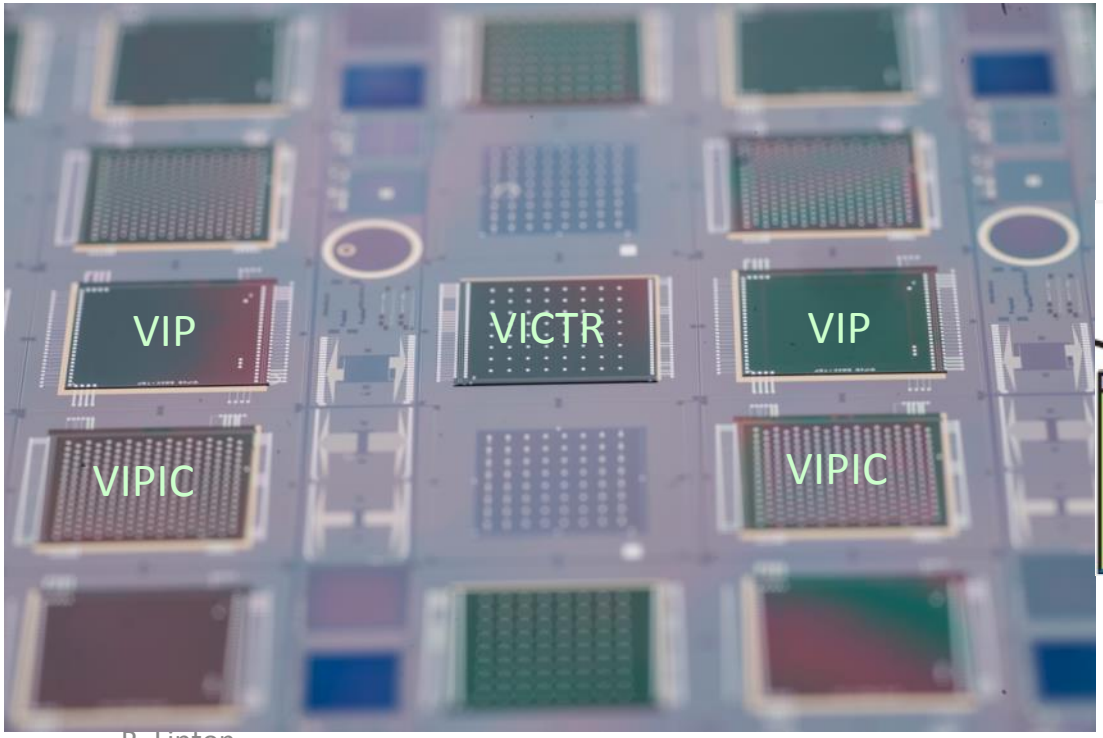
Detailed testing just beginning

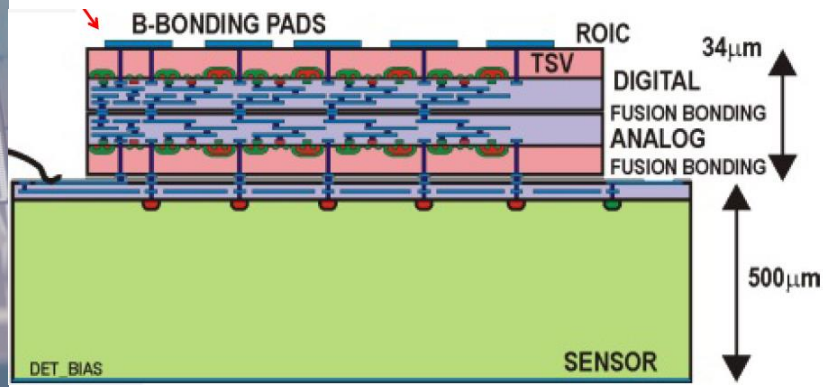




Sensor Integration – Three tier devices

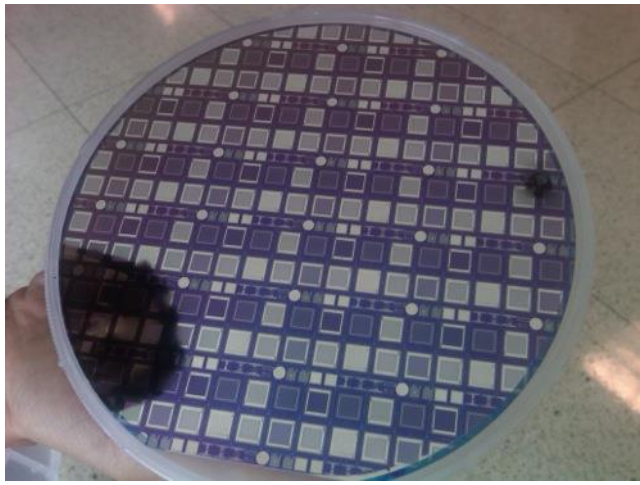
- We then chip-to-wafer oxide bonded 3D chips to BNL sensors to form integrated sensor/electronics assemblies – parts received in March
  - This completes our initial 3D work with Tezzaron and Ziptronix
  - VIP(ILC), VICTR(CMS), and VIPIC(X-Ray) assemblies



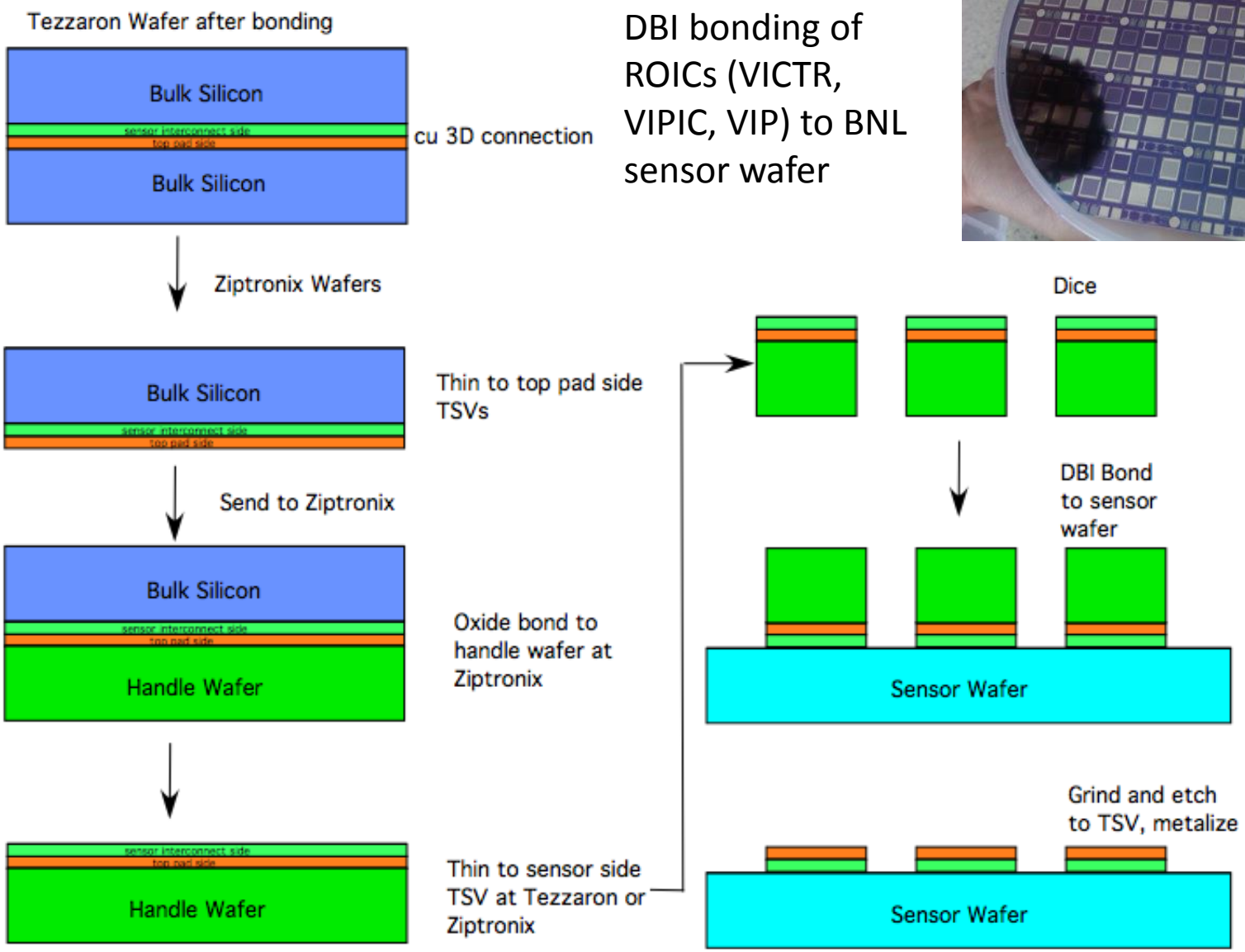


R. Lipton

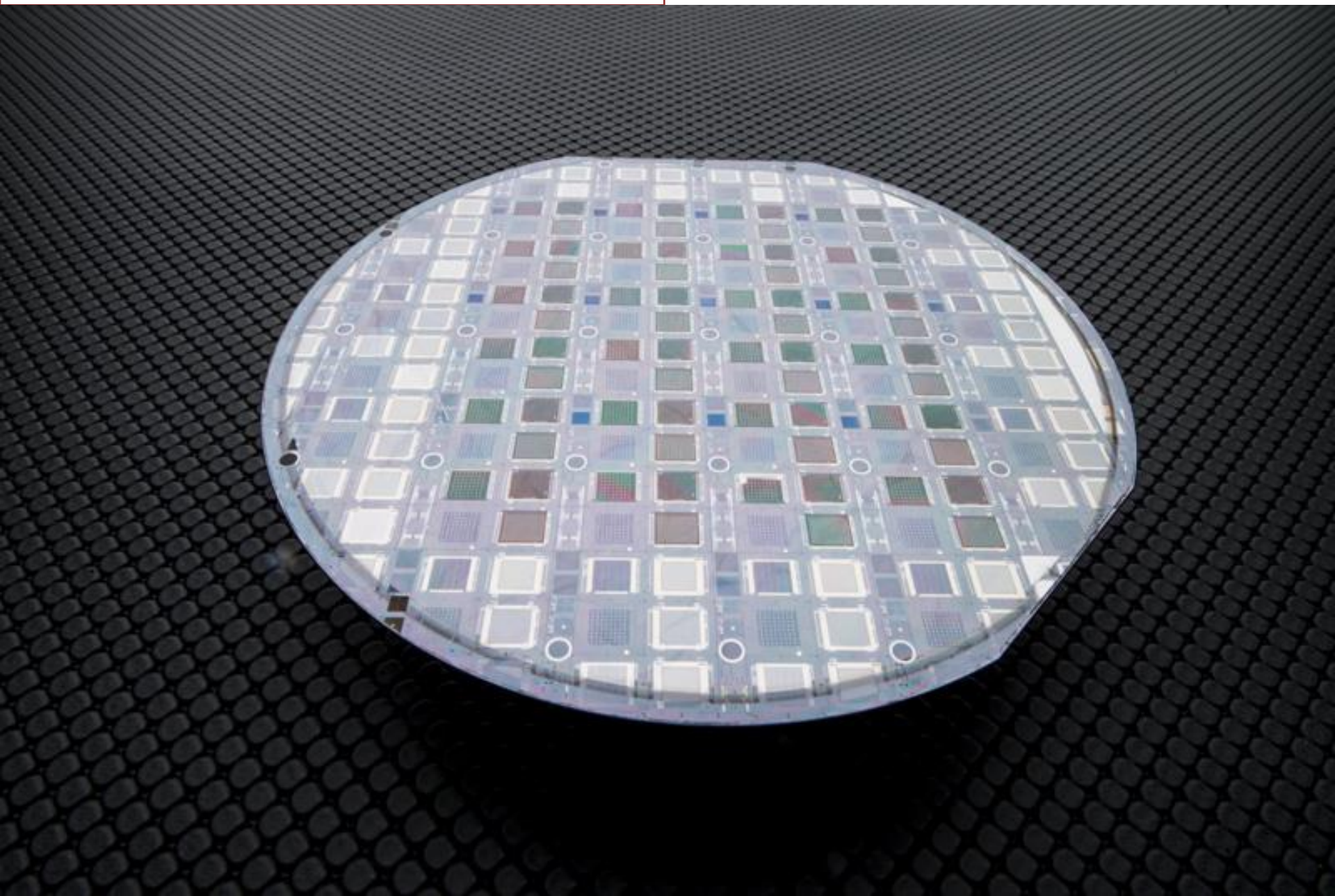
Chip-to-Wafer bond



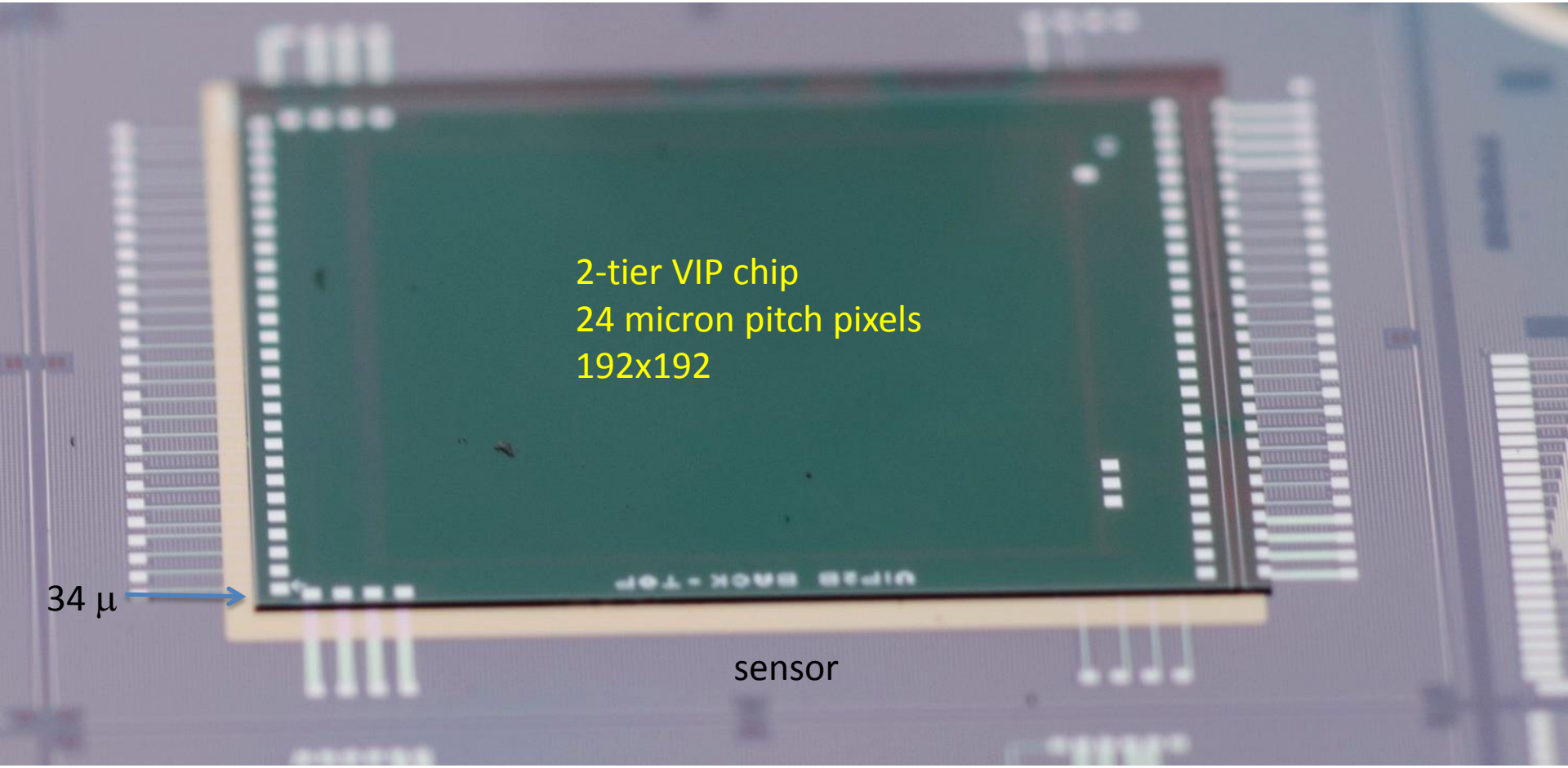
DBI bonding of ROICs (VICTR, VIPIC, VIP) to BNL sensor wafer



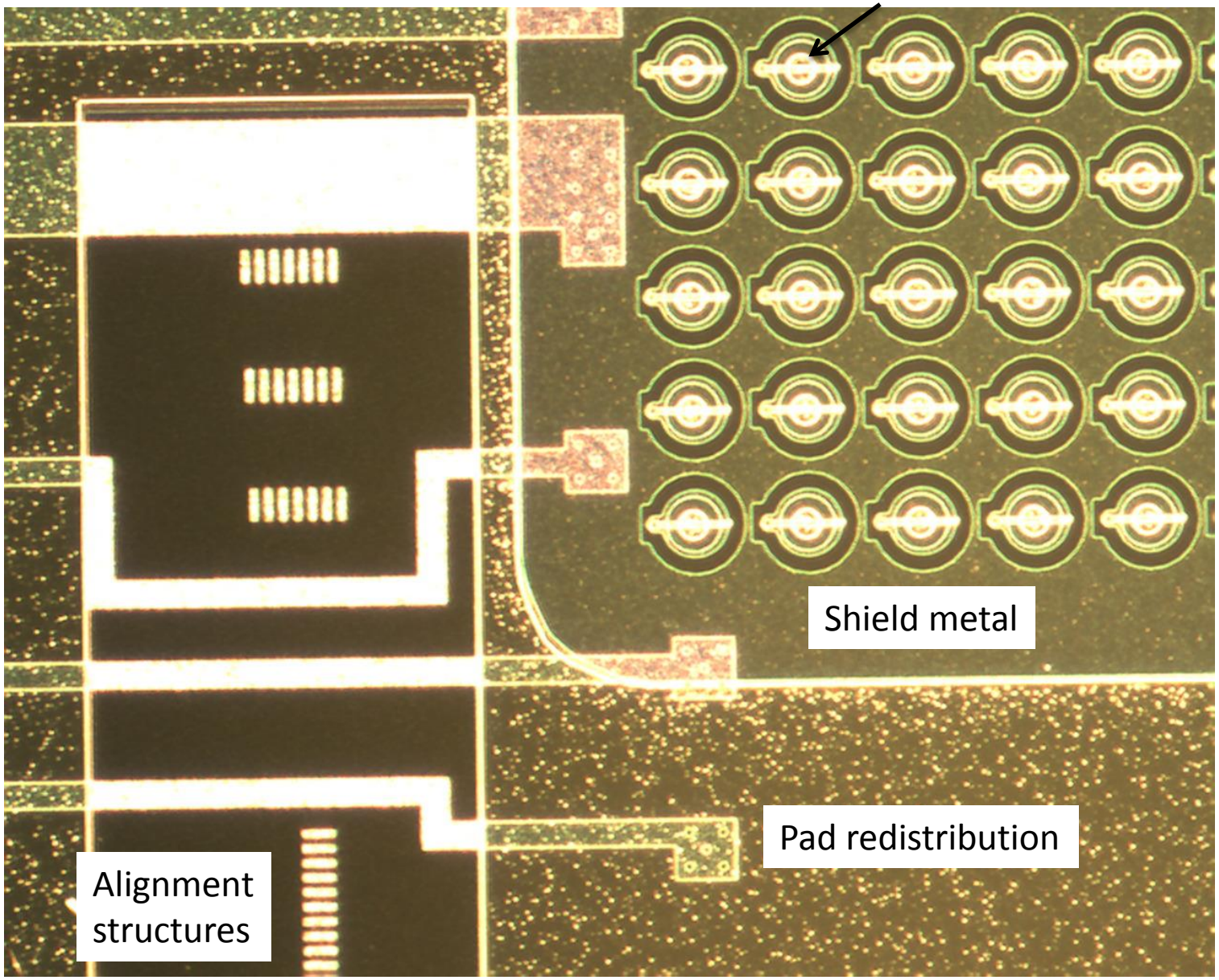
Wafer with bonded Chips



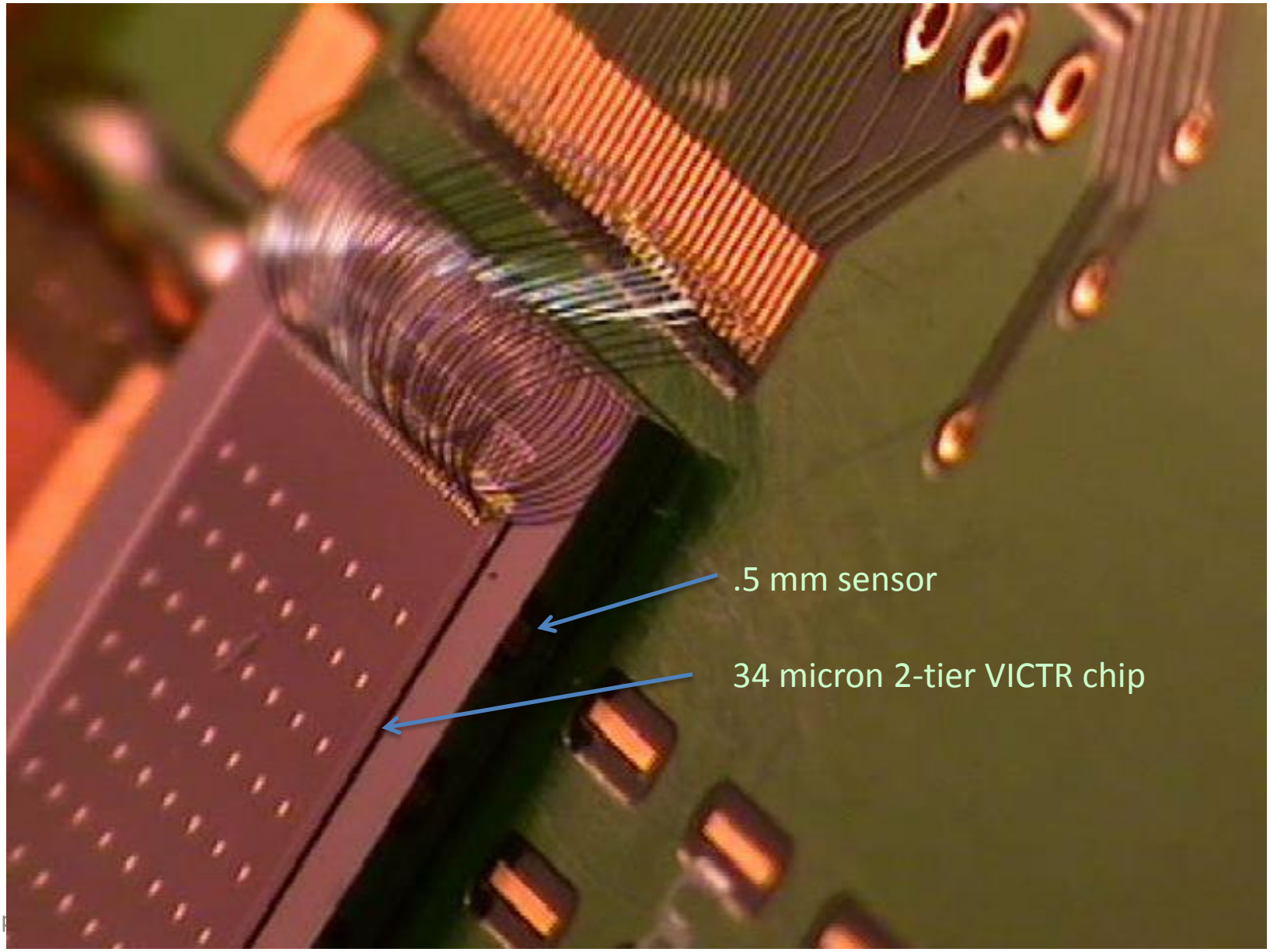
VIP



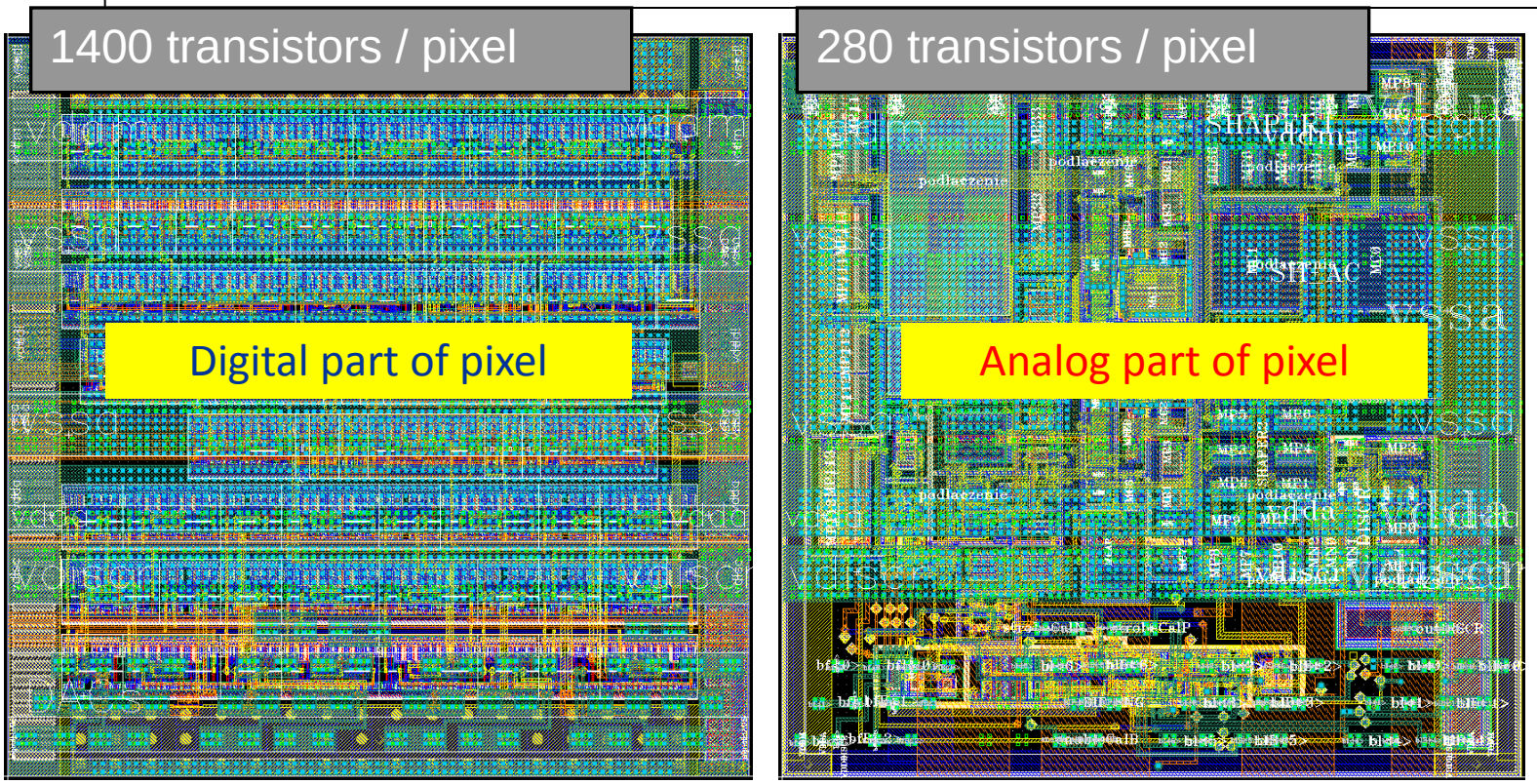
DBI Interconnect



Mounted detectors



3D-IC: Fermilab designs – VIPIC



- 64 × 64 array of 80 mm^2; shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e$^-$ ENC
- Two dead-time-less modes of operation (64 × 64 matrix / in 16 sub-matrices of 4 × 64 pixels):
  - timed readout of hits acquired at low occupancy (address and hit count) σ_t=10μs
  - imaging – counting of events
- Sparsified readout with priority encoder circuit (hit pixel address readout only)

VIPIC Sensor results

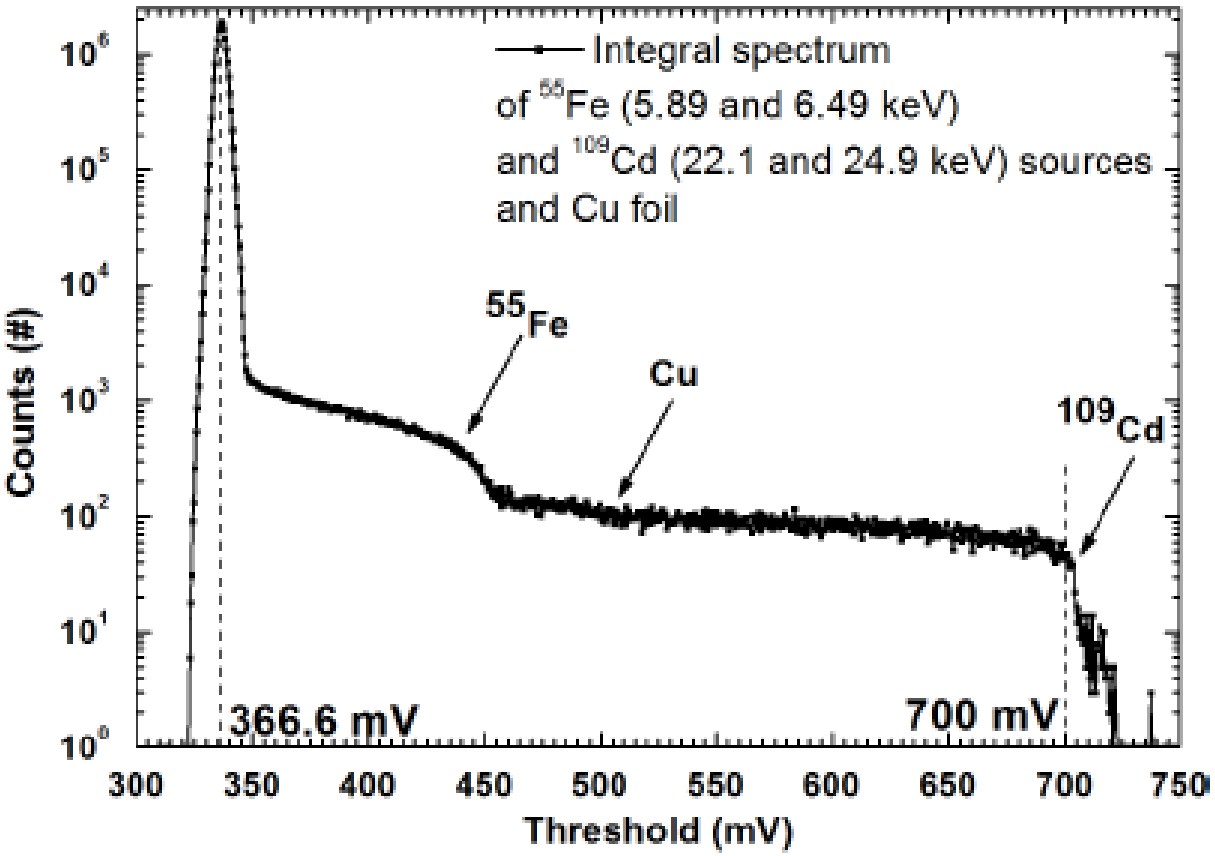
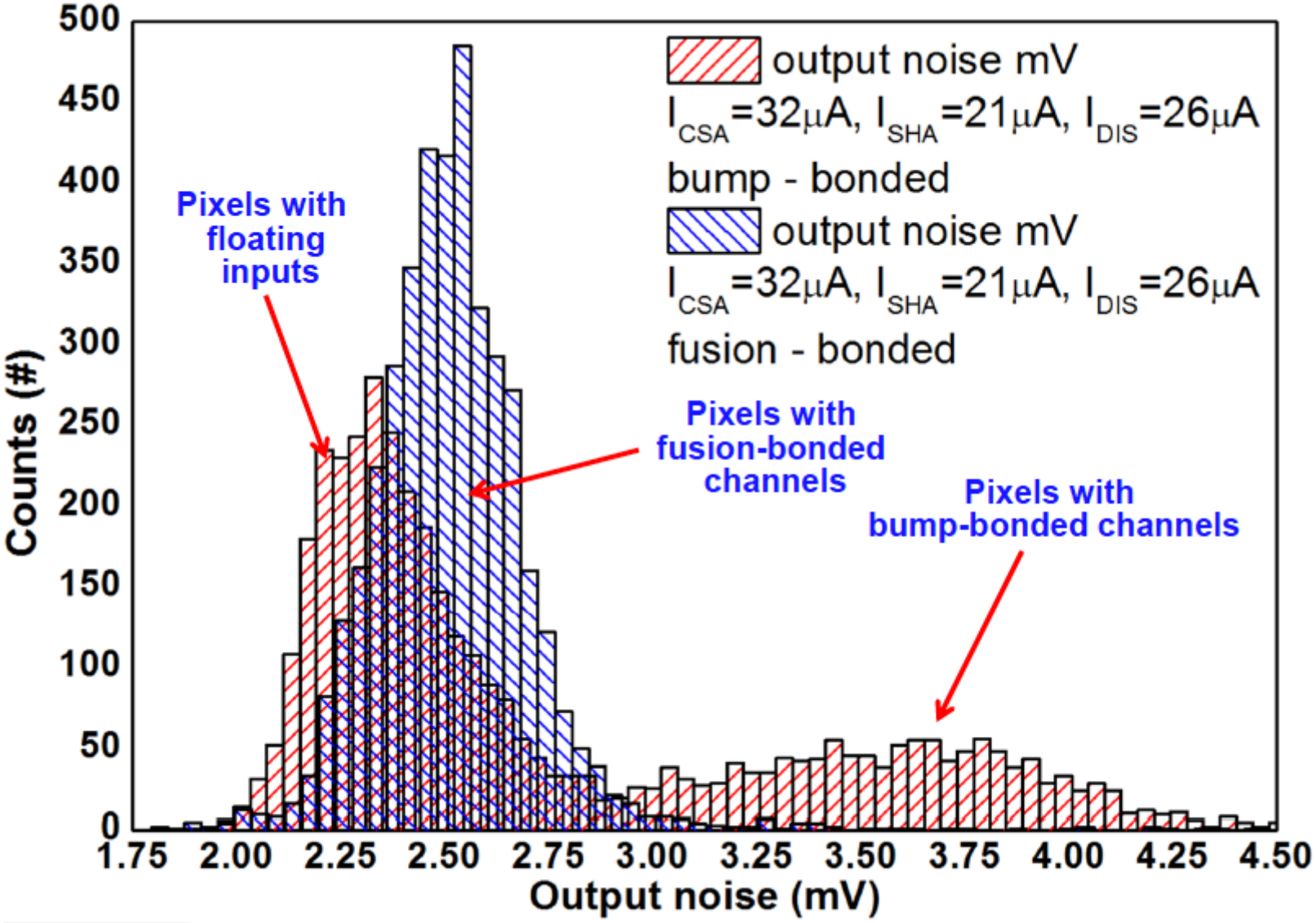


Fig. 5: An integral spectrum registered with simultaneous exposure to ^{55}Fe (back side) and ^{109}Cd (front side) sources.

Because we have both bump-bonded and oxide bonded VIPICs we can compare the performance directly

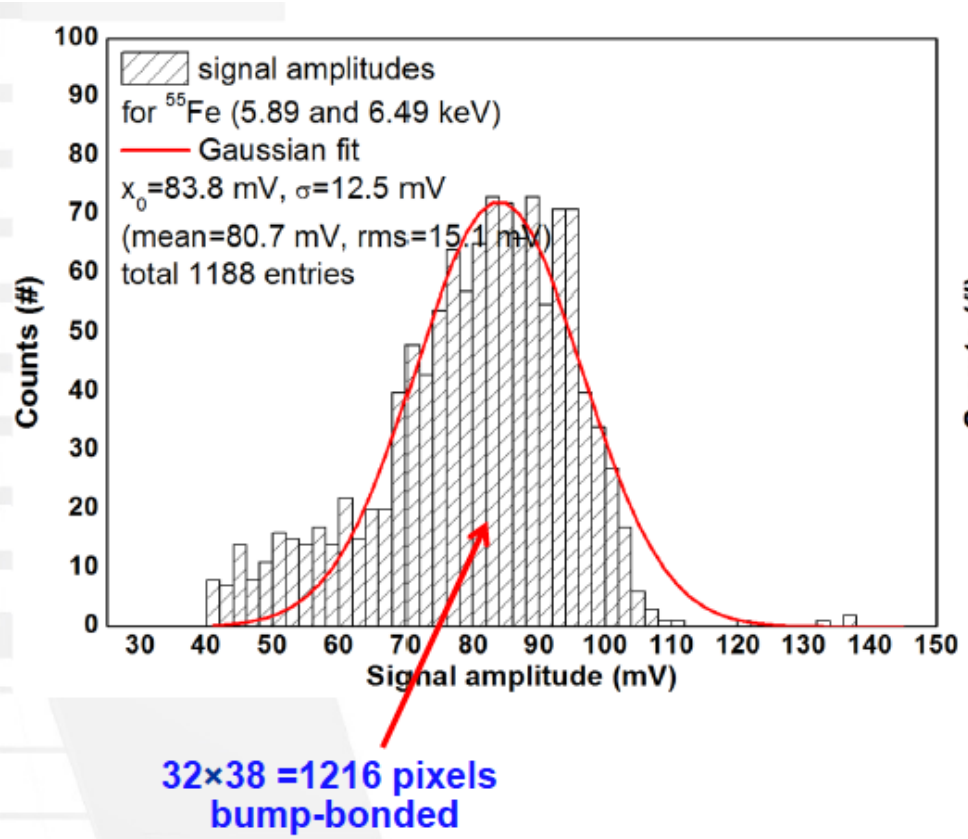
VIPIC Noise

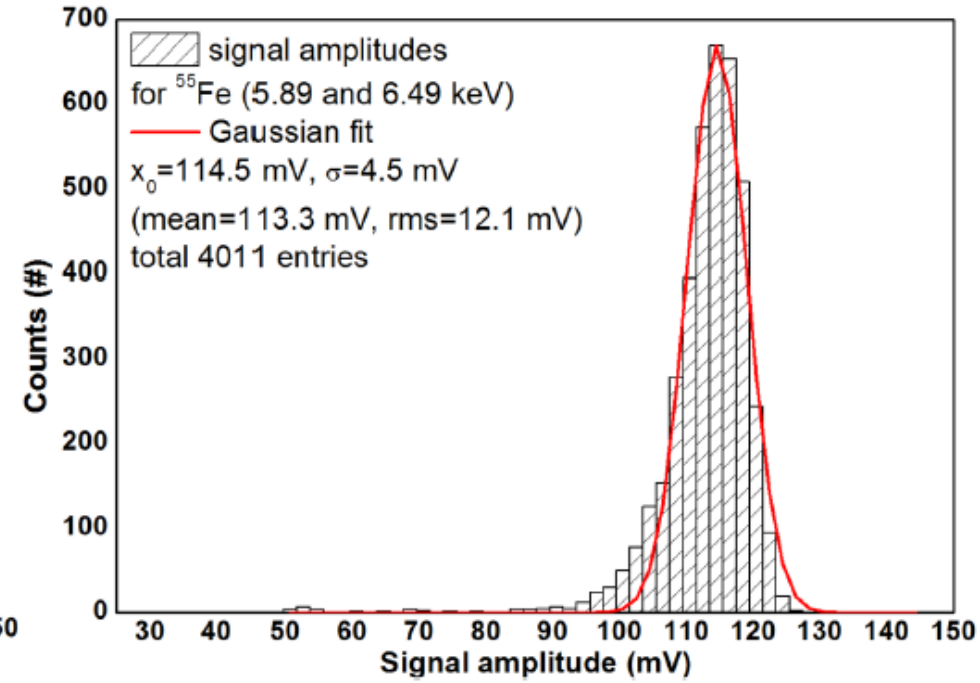


Output noise on oxide bonded devices are close to pixels with no sensors bonded – low interconnect capacitance associated with oxide bond

VIPIC Gain

Lower capacitance is also reflected by larger gain





VIPIC Sensor results

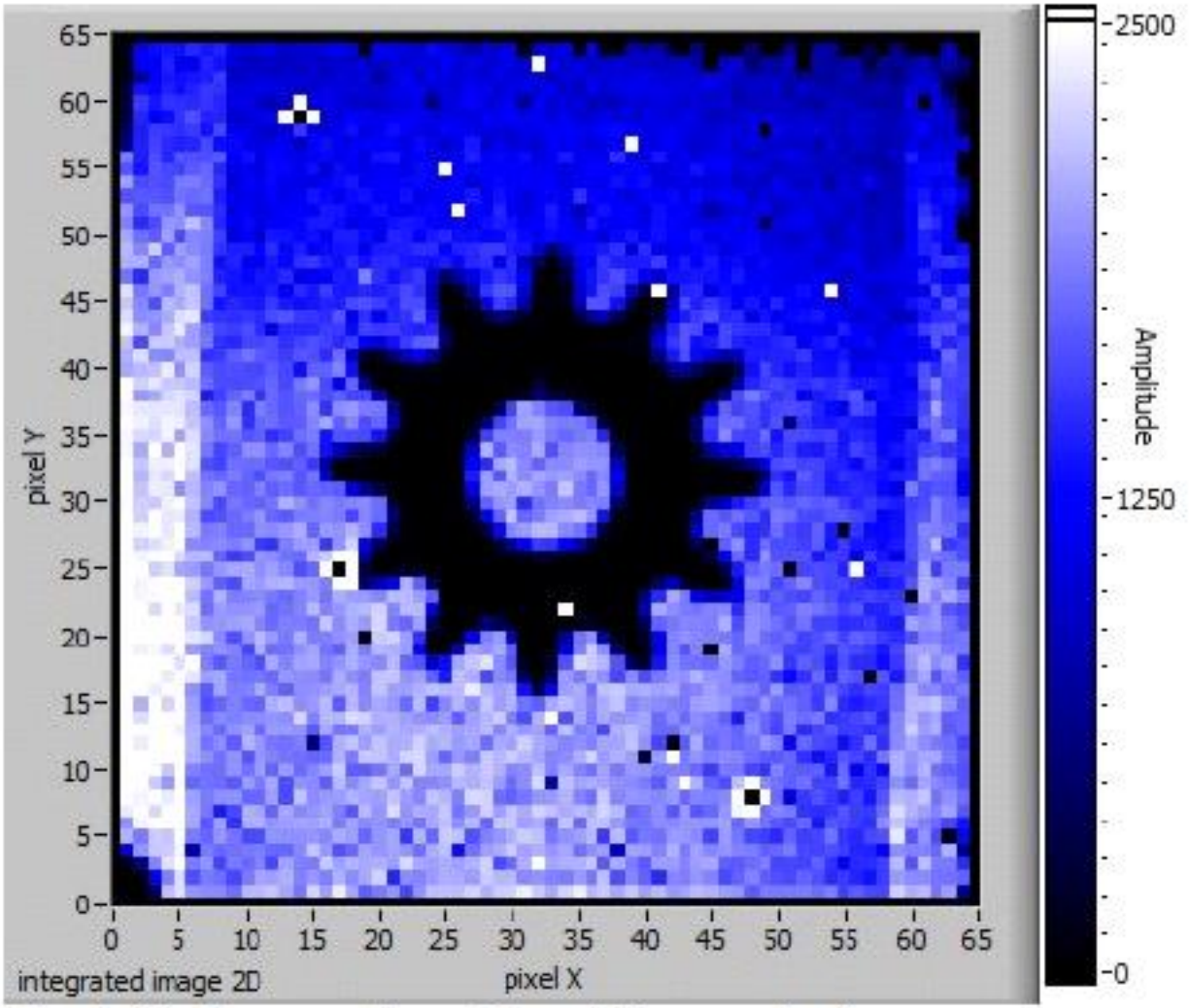


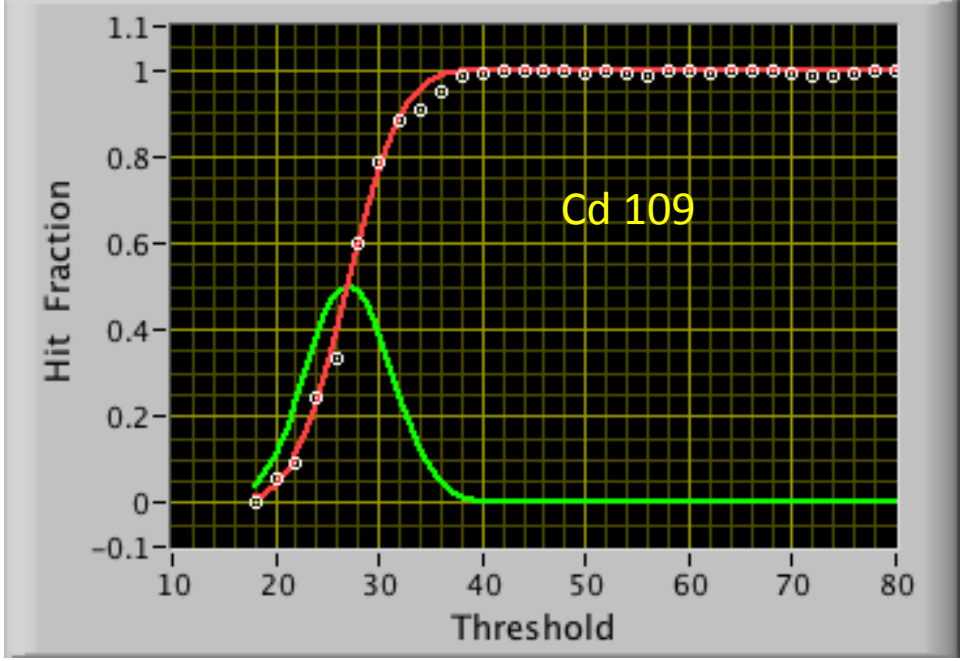
Fig. 4: Radiogram of a wrist-watch gear wheel.

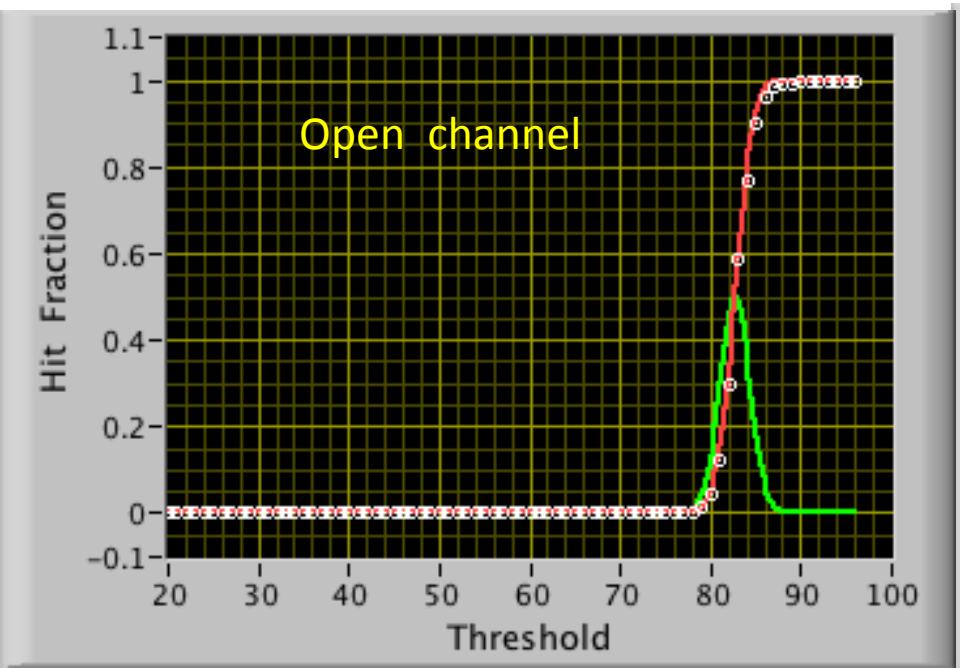
Other Results

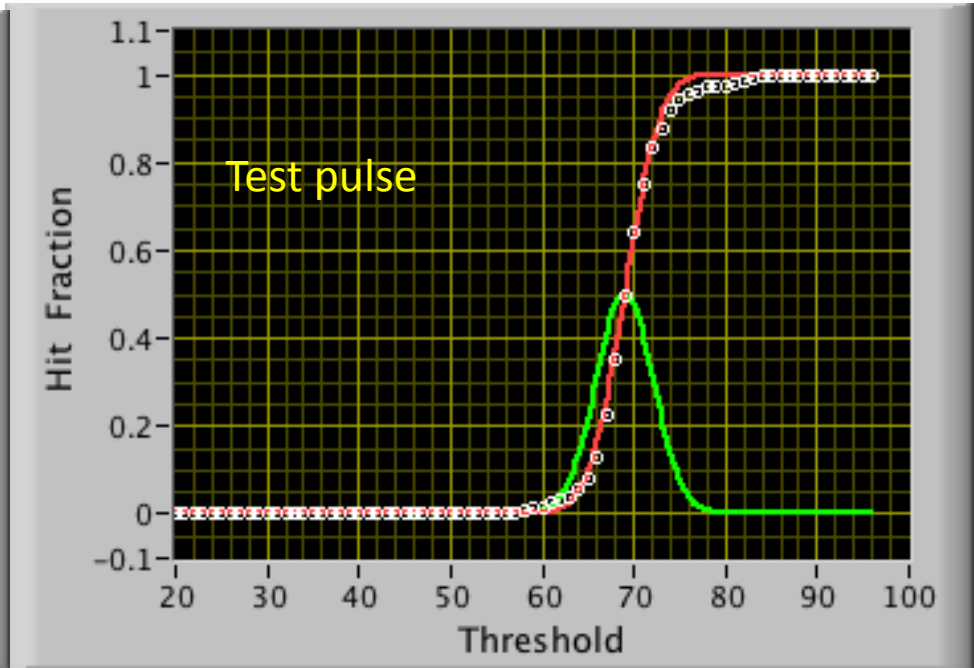
Just started testing VICTR

- Initial threshold scan with Cd^{109} source
- Test Pulse noise ~700 e^- (FEI4 front end designed for lower C_{in})

VIP not yet tested







Large Area Arrays

We have demonstrated new technologies for chip and sensor interconnect. For wide applicability we need to address yield, cost and commercial access. *The goal is inexpensive, large area, fine pitch pixelated systems.*

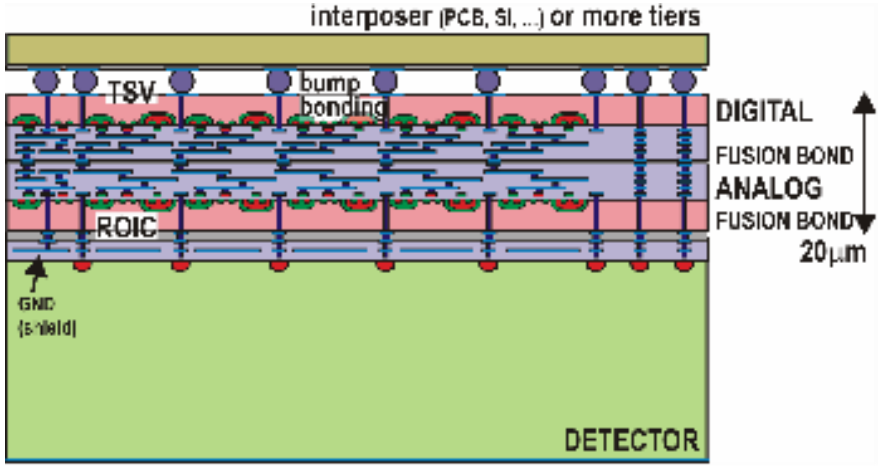
- Such systems will be important (crucial) for many applications in HEP, x-ray imaging and Nuclear Physics
- Two approaches:
  1. Use the fact that wafer-scale sensors can be fabricated with good yield and bond an array of smaller readout chips to a large sensor
     - Interconnect geometry is a central issue
  2. Fabricate tiles from wafer-wafer bonded devices which can be butted on all four sides to fabricate arrays of arbitrary size.

Combining the two 3Ds

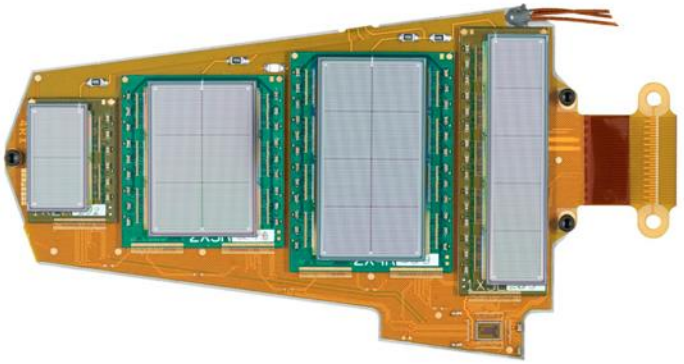
Low cost, large area, thin, pixelated sensor planes with no dead regions.

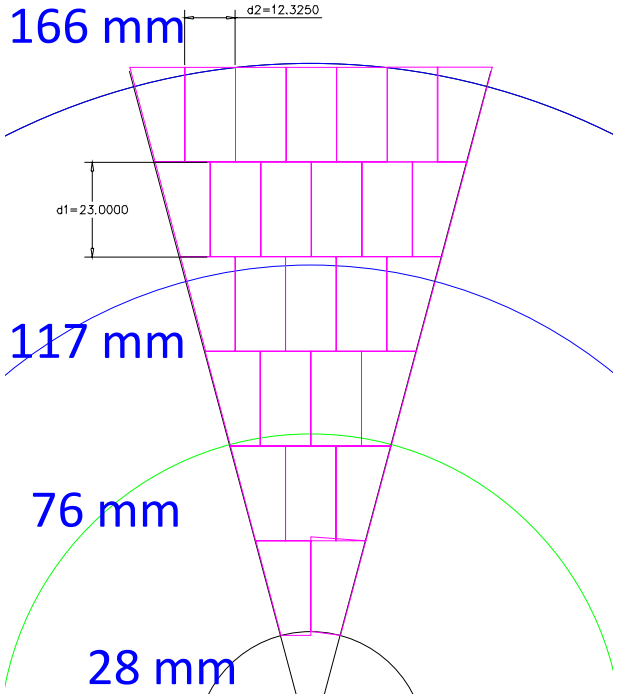
Decouple bond and array yields

- 3D provides backside interconnect to eliminate peripheral bond connections
- Sensors can be processed to have “active edges” using deep reactive ion etch so assemblies can be tiled.



CMS FPIX Plaquette



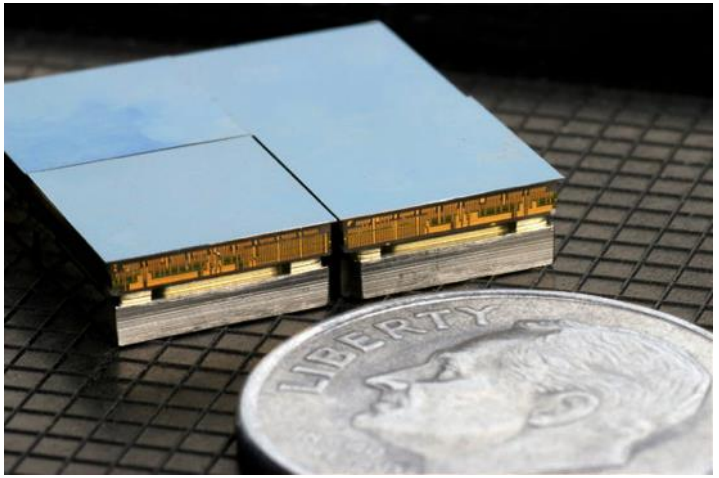


SiD (ILC) Outer pixel disk

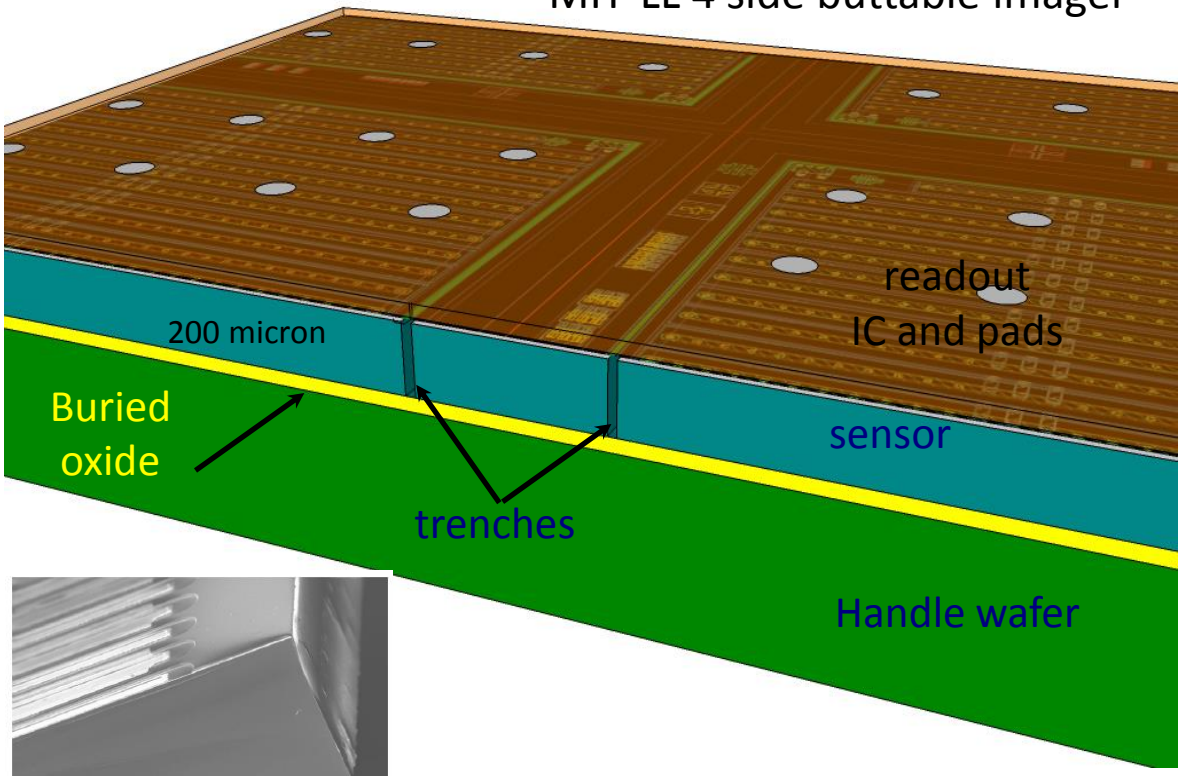
How can we do it with 3D?

Combine active edge technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.

- These tiles can be used to build large area pixelated arrays with good yield and reasonable cost
- Tiles can populate complex shapes with optimal tiling and low dead area
- Only bump bonds are large pitch backside interconnects
- High density and geometrical flexibility

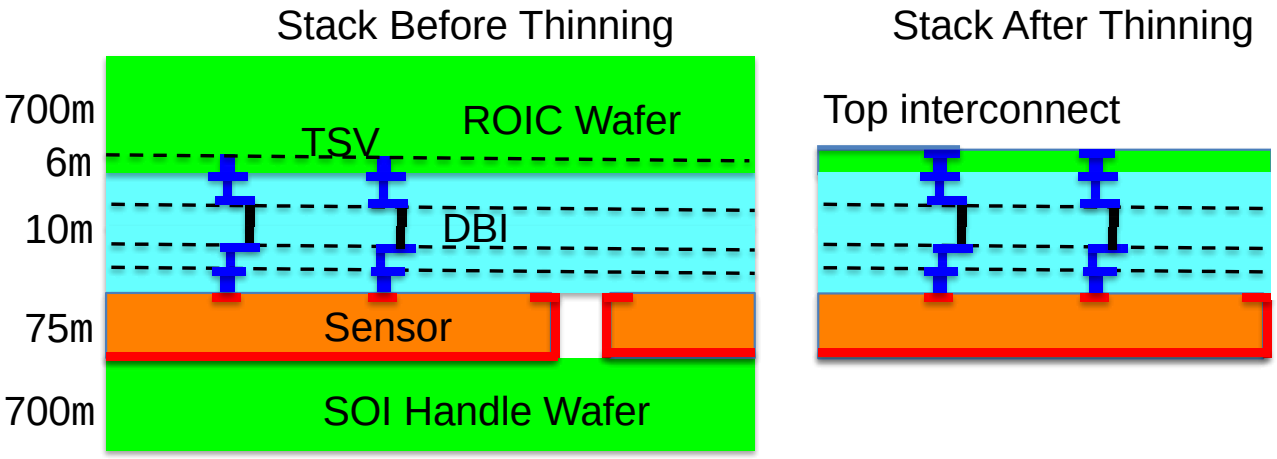


MIT-LL 4 side buttable imager

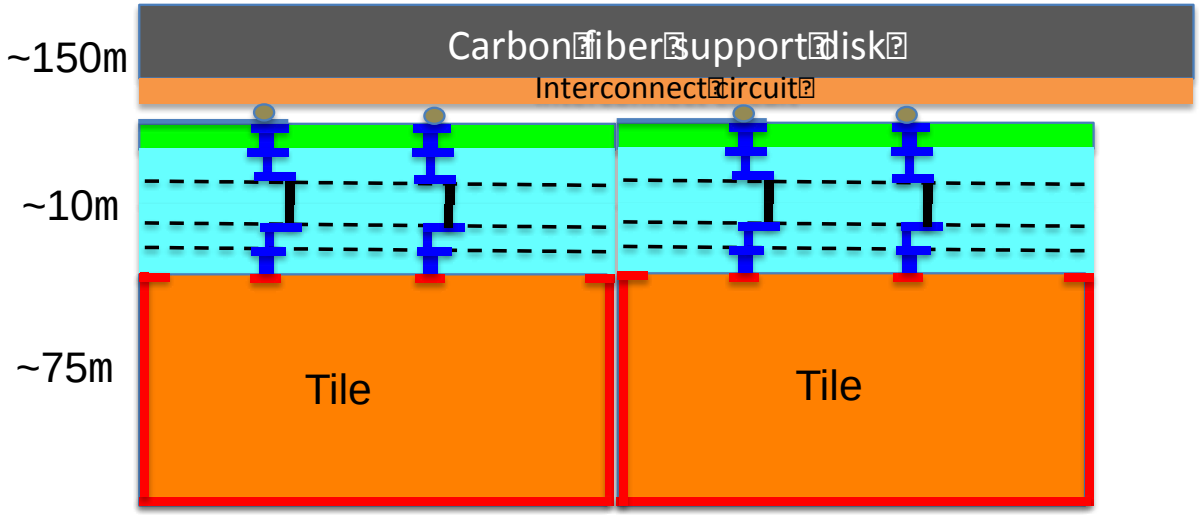


VTT Active Edge sensor

Tiling sensors



Needs a robust, planar wafer-wafer bond to allow thinning and topside processing

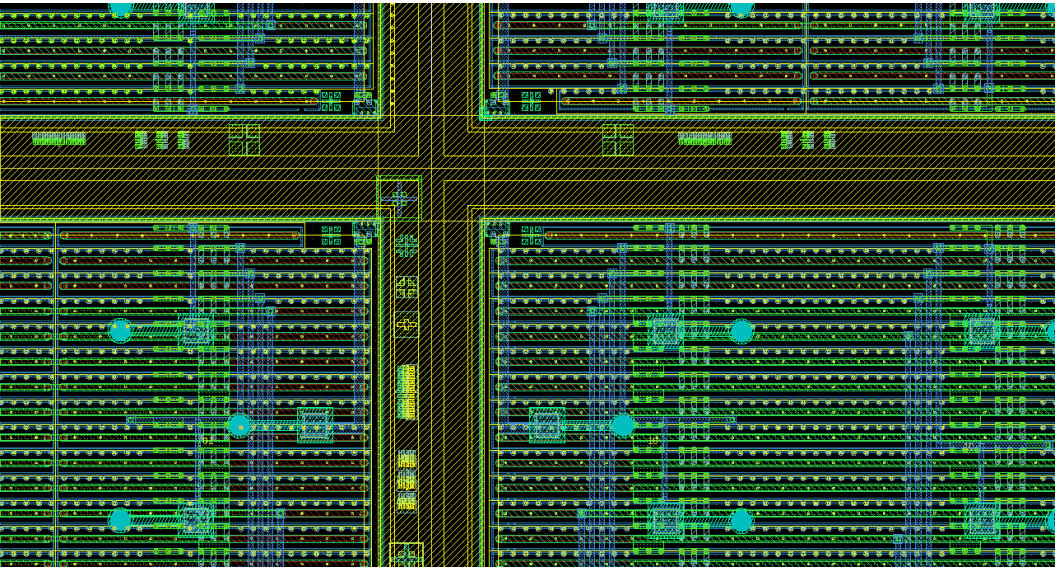


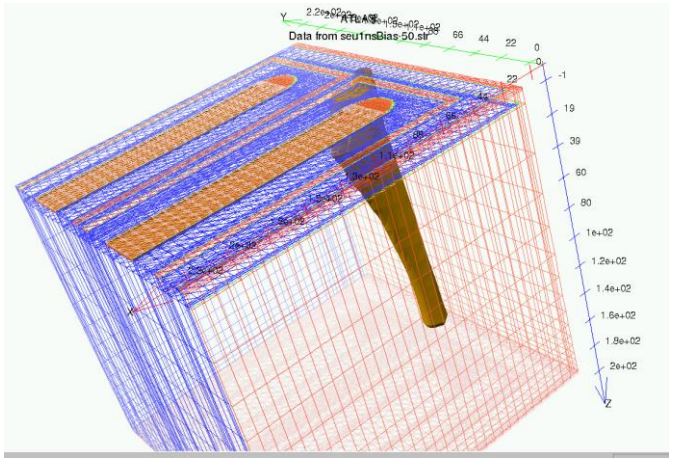
Demonstration Project

A project to demonstrate this technology is underway using:

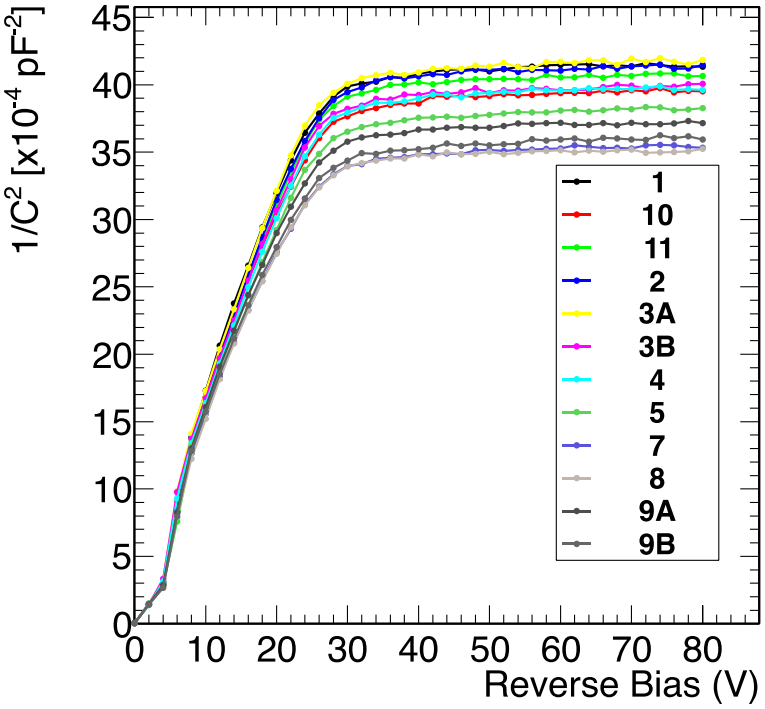
- active edge sensors from VTT, based on early CMS long/short strip PS module designs
- Dummy ROIC wafers from Cornell

The two will be wafer-wafer DBI bonded by Ziptronix .





Simulation of charge density due to 3.5GeV muon hitting near the edge- study charge collection and edge effects.



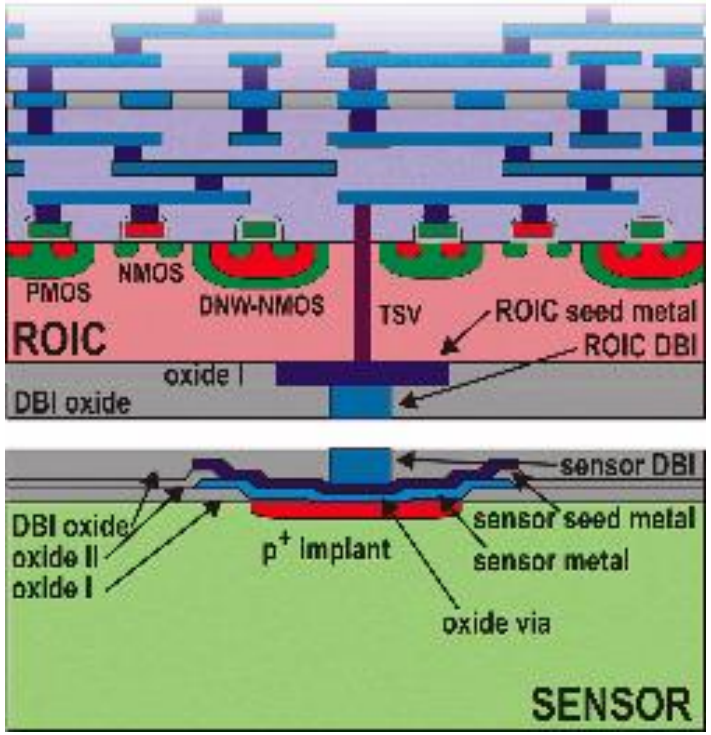
Summary

- We are now able to use 3D technology to combine optimal sensors and readout without many of the compromises inherent in other technologies – this is available now
- We have demonstrated a commercial process for:
  - 3D bonding wafer-wafer bonding and post processing of two layers of commercial 0.13 micron electronics with 4 μ pitch
  - Chip-to-wafer oxide bonding to sensors with 25-80 μ pitch
  - Reduced noise relative to bump bonding
- We are studying the extension of these technologies to large area devices by combining active edge devices with 3D electronics

3D – Sensor/ROIC Oxide Bonding

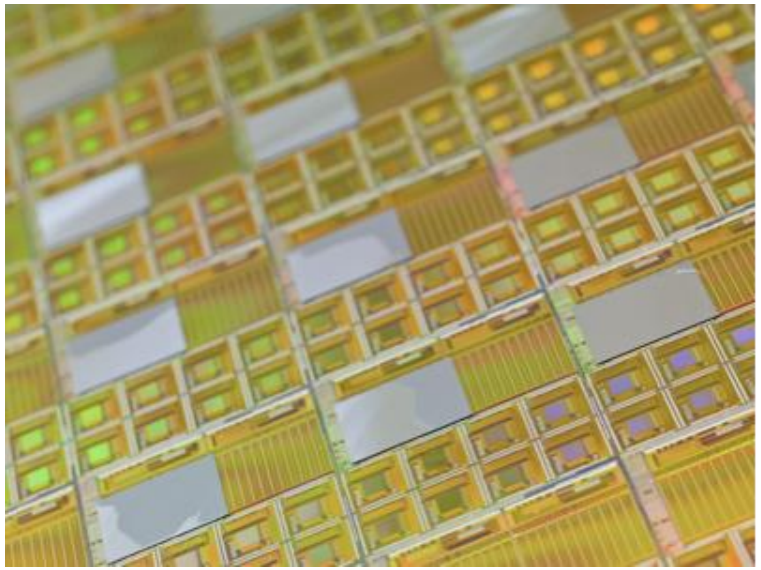
A promising fine pitch bonding technology the direct bond interconnect (DBI) oxide bond process from Ziptronix

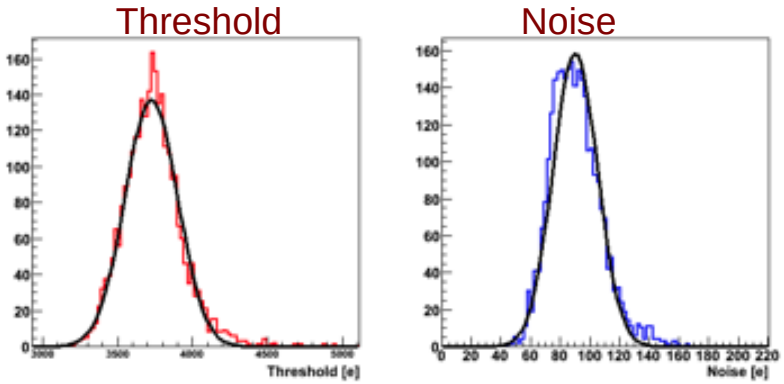
- No bump bonds – planar resulting wafer
- Very fine pitch - 4 microns used for 3D Tezzaron wafers
- Mechanical strength enables aggressive post-bond thinning
- Uses standard IC processes - CMP and metalization
  - Can withstand high temp.
- Wafer-wafer bond can be reworkable
- In principal can be low cost

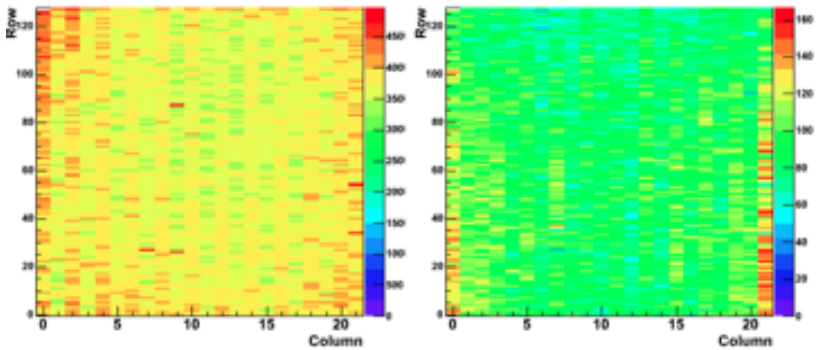


Oxide Bonding

- Initial work was based on existing ROIC wafers from BTeV and sensor wafers from MIT-LL.
  - Sensor chip to FPIX wafer bond
  - Sensors ground to 100 microns - 8 V depletion
  - 100% connectivity on sensors without obvious bond voids
  - No degradation in s/n
  - Radiation hard to >10 MRad
- This the process that was eventually used for 3D wafers



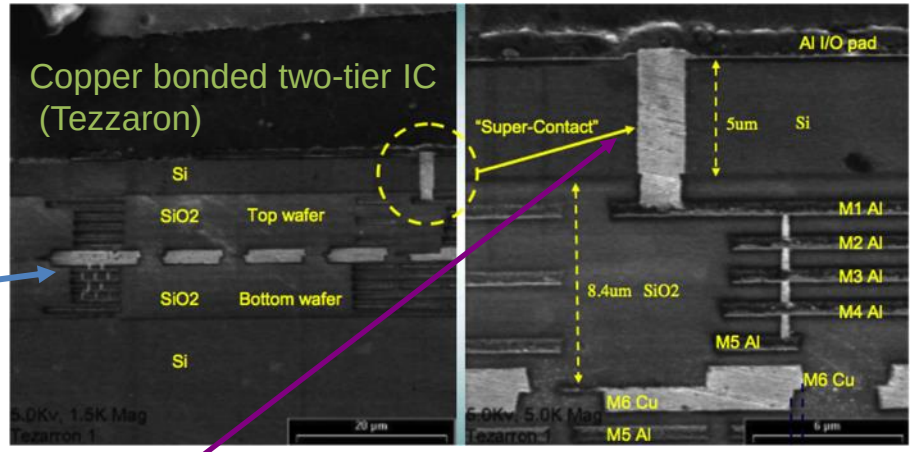


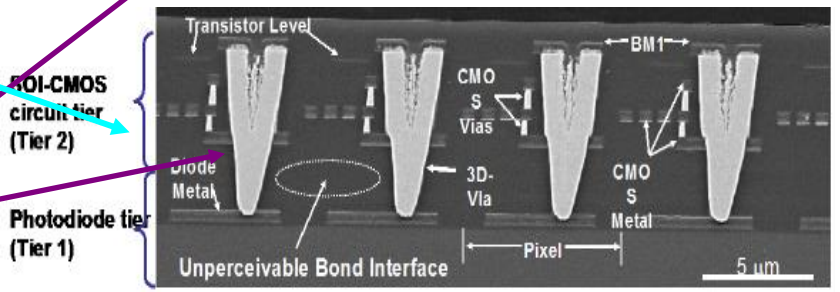


3D Interconnect

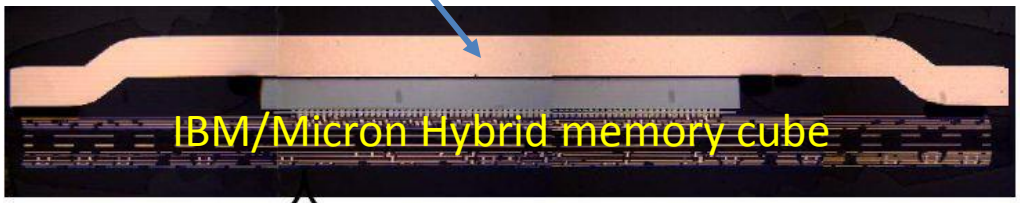
Technology based on:

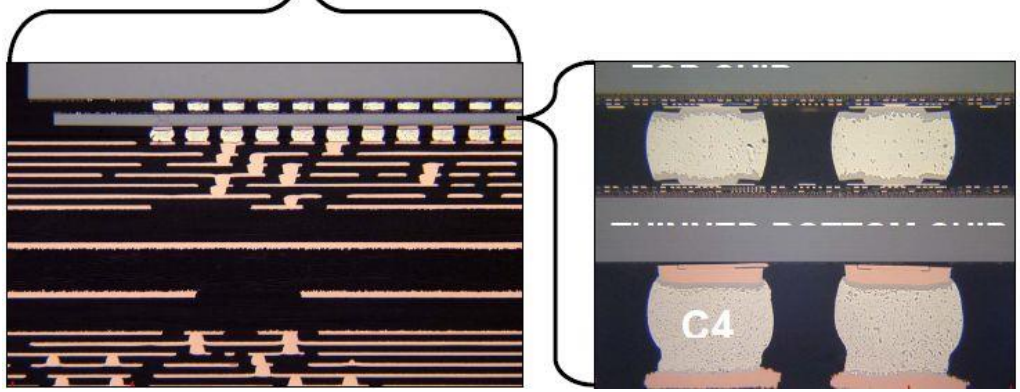
- Bonding between layers
  - Copper/copper
  - Oxide to oxide fusion
  - Copper/tin bonding
  - Polymer/adhesive bonding
  - Cu stud
- Through wafer via formation and metalization

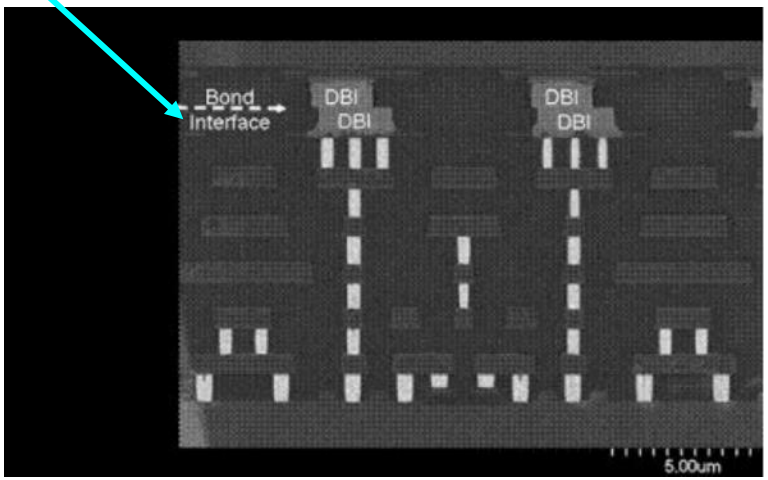




8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)

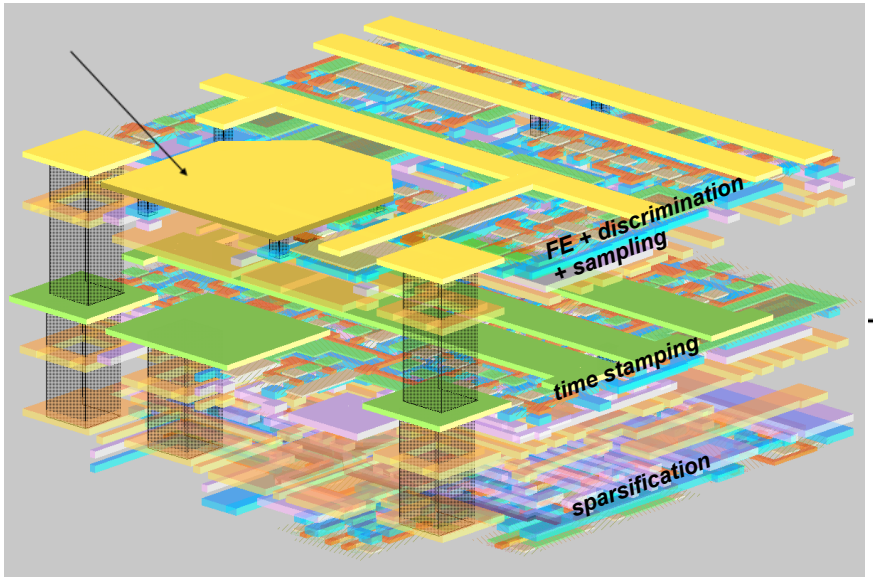




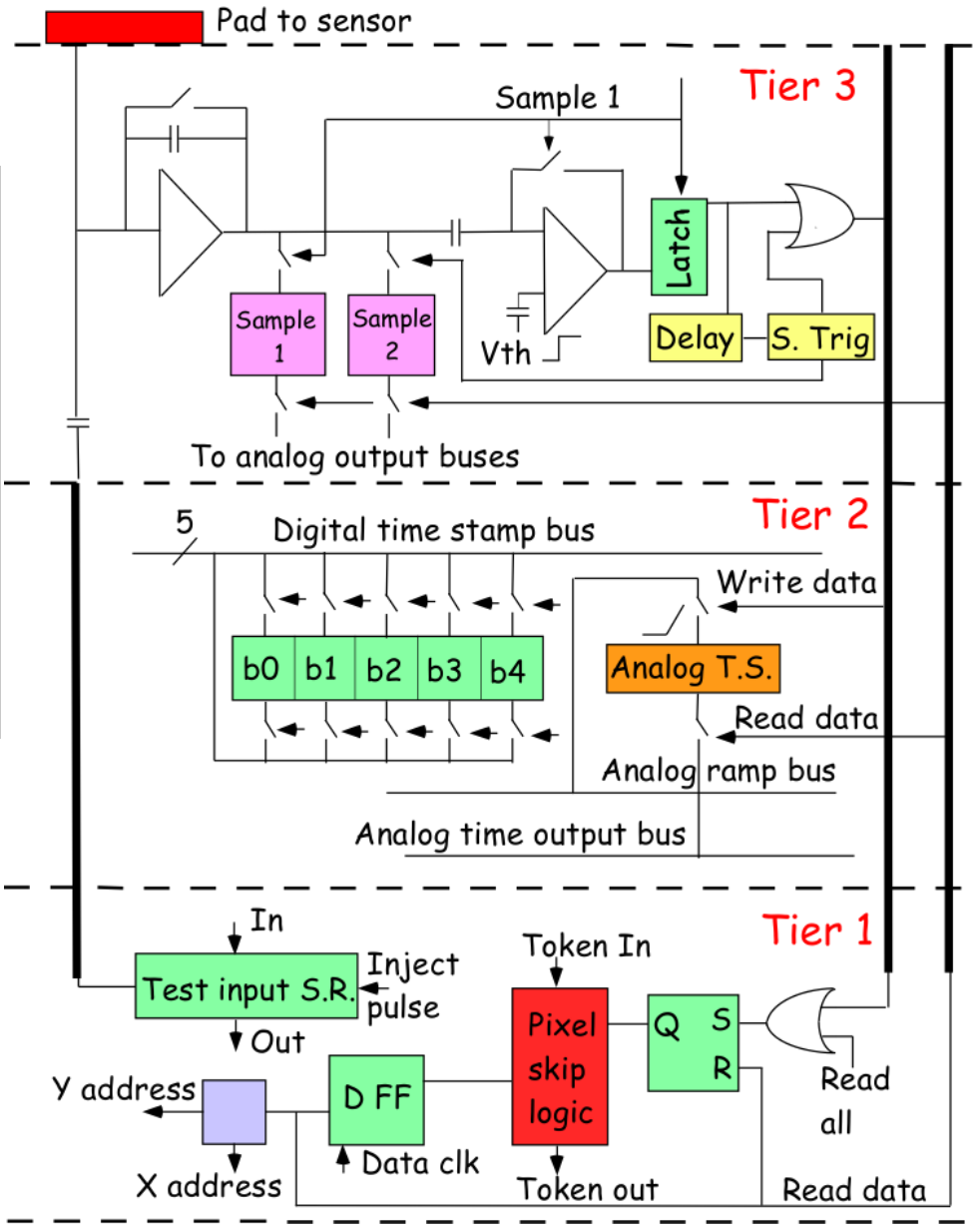


8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

3D Geometry

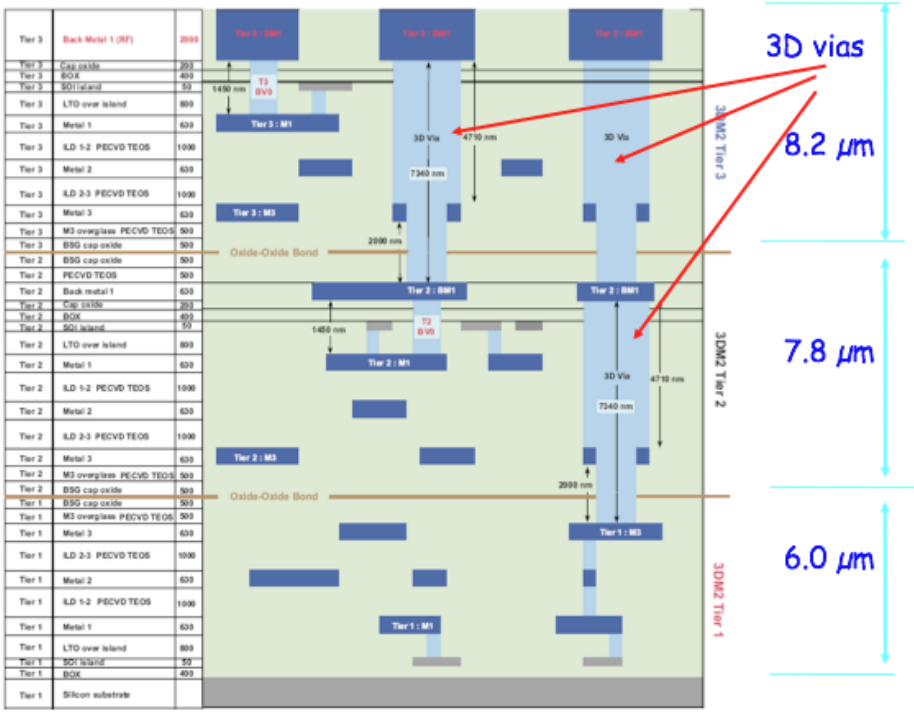


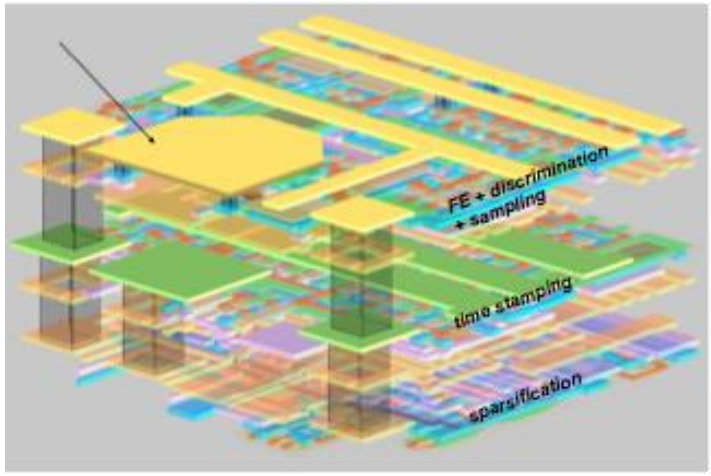
Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff



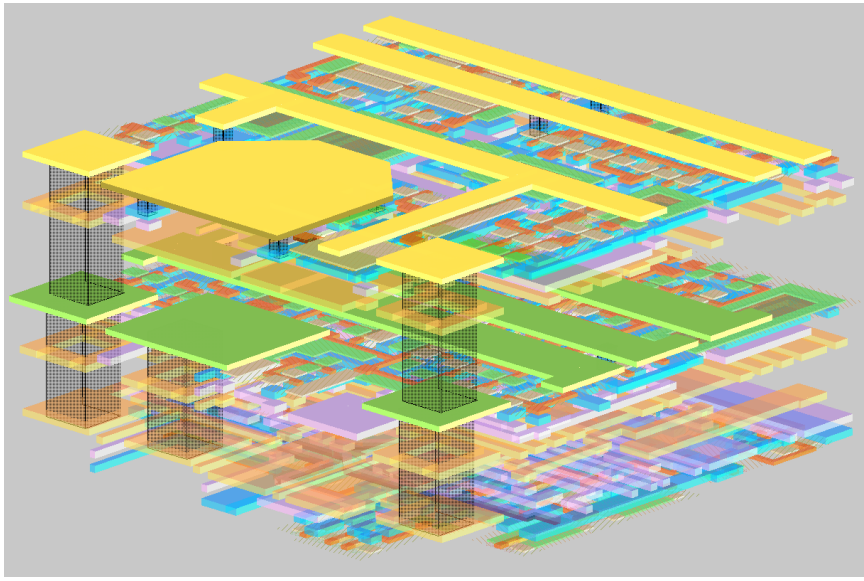
MIT-LL 3D Technology

- MIT-LL had developed a 3D technology which seemed an excellent match to HEP needs.
  - Demonstrated 50 micron thick bonded sensor/readout
  - 3 Tiers of 0.18 micron SOI CMOS
  - Bonding, thinning and detector laser anneal technology
- We were invited to participate in 2 DARPA-sponsored 3D runs.





VIP Chip



- Chip designed for ILC Vertex
  - Low power front end
  - Digital and and analog time stamp
  - Sparse scan readout
  - 20(VIP1) 24(VIP2a) micron pitch
- Initial submission had low yield and marginal functionality due to MIT-LL process issues.
- Second submission with a more conservative design worked well. Converted to 0.18 micron CMOS for 3D Tezzaron run VIP2b.
- This gave us experience and confidence - next steps:
  - Move to a commercial process (Tezzaron, Ziptronix)
  - FNAL designs for x-ray (VIPIC), LHC (VICTR), ILC (VIP2b) applications