Development and Evaluation of Event-Driven SOI Pixel Detector for X-ray Astronomy

TIPP2014 @ Amsterdam, The Netherlands　2014.06.02-06

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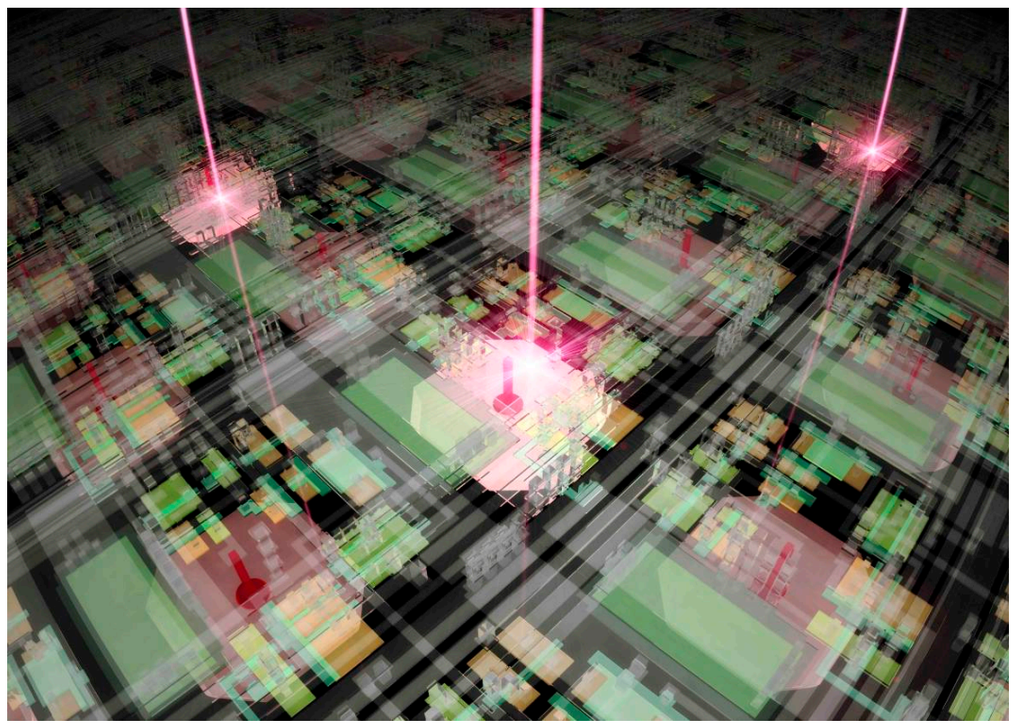
SOIPIX Group.

Outline

- **Introduction**
  -> **SOI Pixel Detector for Future X-ray Astronomy (XRPIX)**
- **XRPIX Design Description**
- **XRPIX Performance Tests**
- **Summary**



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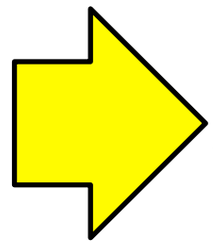
Standard Imaging Spectrometer of modern X-ray astronomical satellites



X-ray CCD

- Fano limited spectroscopy with the readout noise ~3 e- (rms).
- Wide and fine imaging with the sensor size of ~20 - 30 mm, pixel size of ~30 μm sq.
- High QE by BI and thick depletion (200 μm for ASTRO-H).

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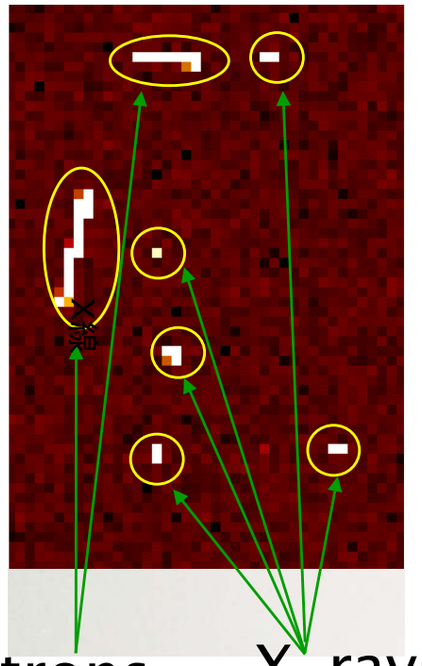
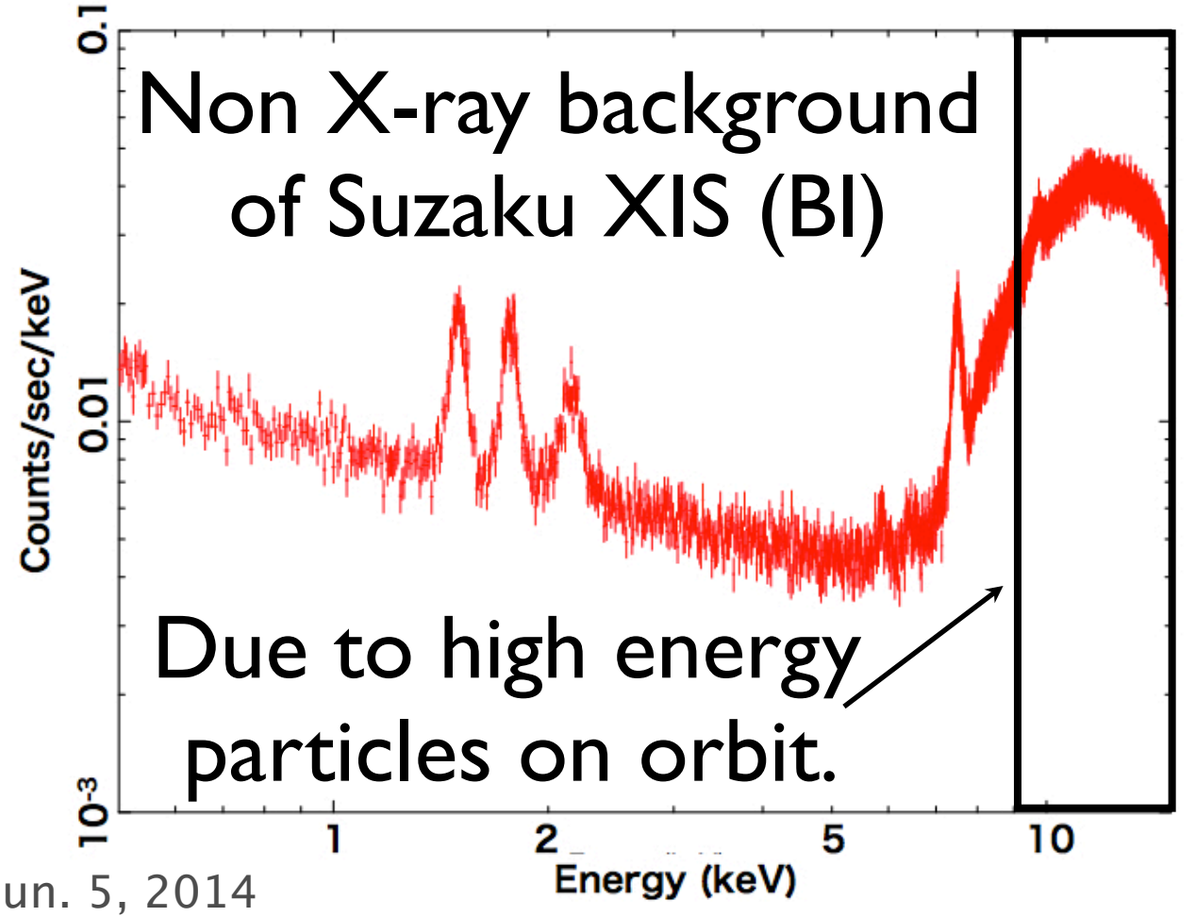
X-ray CCD Raw Image



Particle : Track
X-ray : One or adjacent pixels.

However …

- Non X-ray background above 10 keV is too high to study faint sources.
- The time resolution is too poor (~sec) to make fast timing observation of time variable source.



Introduction of SOI Pixel Detector

- A monolithic pixel detector with Silicon-on-Insulator (SOI) CMOS Technology -> 0.2 μm fully-depleted (FD) - SOI pixel process

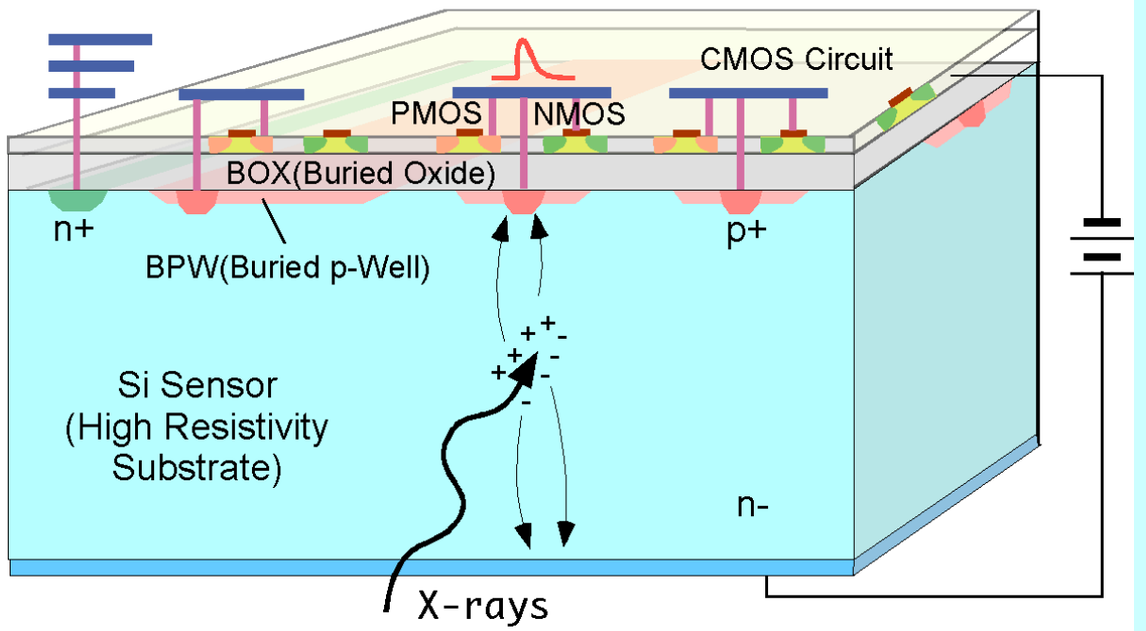
- SOI Pixel Detector (SOIPIX) : Processed by LAPIS Semi. Co., Ltd.

SOIPIX Advantages
- No mechanical bump bonding
  -> High Density, Low Parasitic Capacitance, High Sensitivity
- Standard CMOS circuit can be built
- Based on industrial standard technology

Basic Components
Circuit Layer : ~40 nm
Buried Oxide (BOX) : 200 nm
Sensor Layer : 100 - 725 μm

SOI Pixel Process
New Process to make pixel detector with SOI technology joint development with LAPIS Semi. Co., Ltd.

Our group presentations:
H.Matsumura (next presentation),
T.Miyoshi (5 Jun, I.b 12:20 -),
S.Honda (6 Jun, I.b 14:00 -),
K.Kasahara (6 Jun, I.d 15:00 -)



SOI Pixel Detector for Future X-ray Astronomy

The performance required of a future X-ray astronomical satellite is the following ...

Target Specification

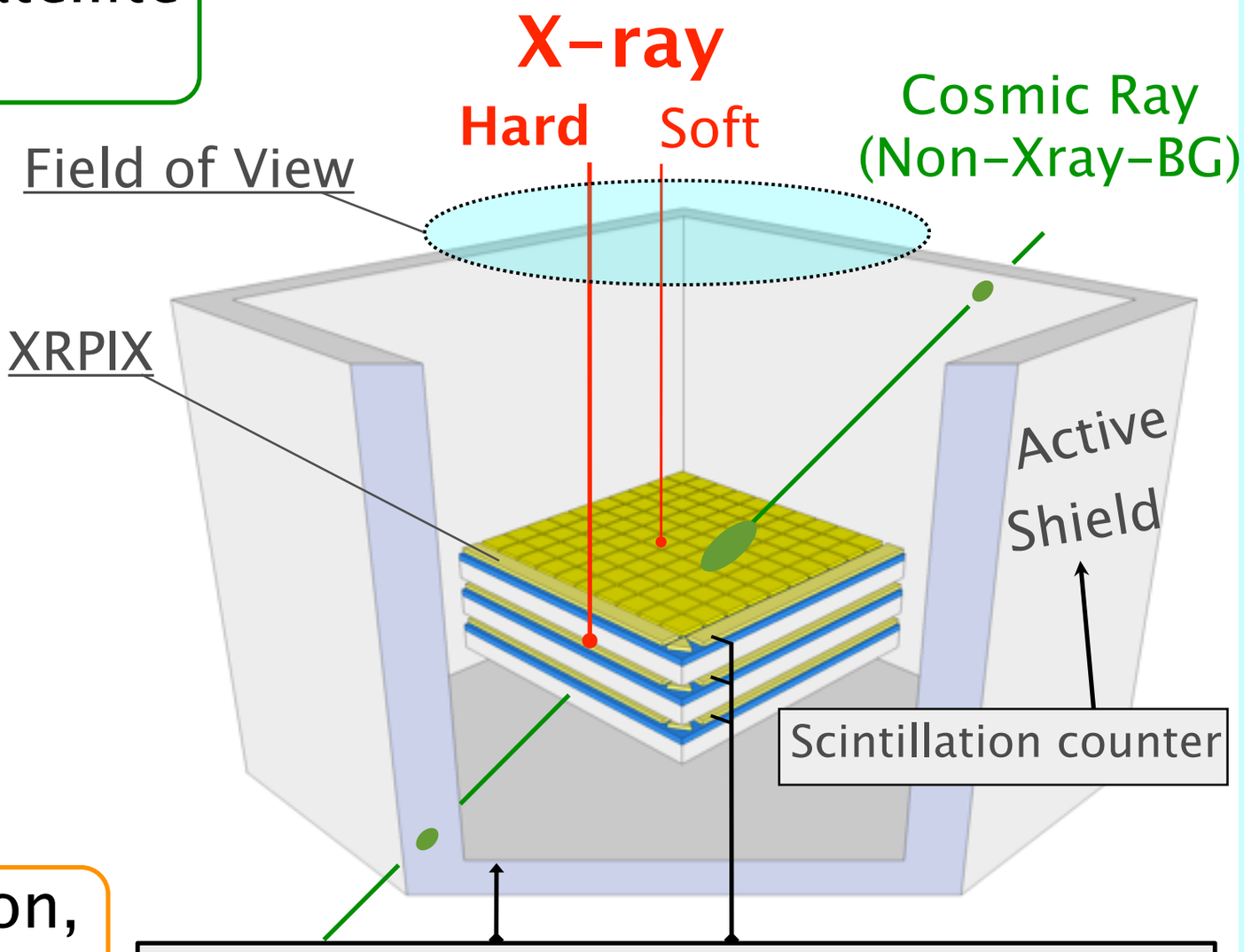
(1) FWHM ≤140 eV at 6 keV
Readout Noise :
req. ≤ 10 e-/ goal ≤ 3 e-
(2) <100 μm pitch pixel
(3) ~10 μs per event readout
(Trigger, Direct Pixel Access)
(4) Wide energy range : 0.3- 40 keV
(Thick Depletion Stacks)

In order to achieve specification, we have been developing X-ray SOI Pixel Detector (XRPIX).

XRPIX has self-trigger function !

-> Realization of Event-Driven

X-ray SOIPIX with Active Shield

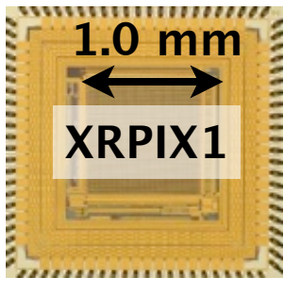


Onboard Processor

- Anti-coincidence (NXB rejection)
- Hit-pattern Selection (NXB rejection)
- Direct Pixel Access (X-ray Readout)

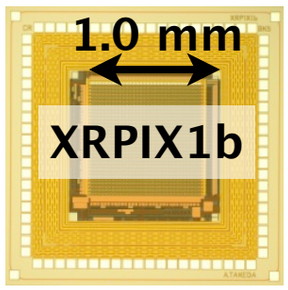
XRPIX Series

2010 2011 2012 2013 2014

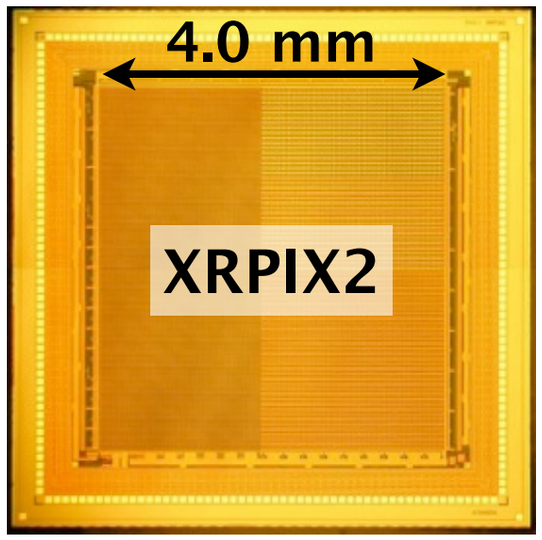


2.4 mm

First Model
Trigger Output
(Event-Driven readout)

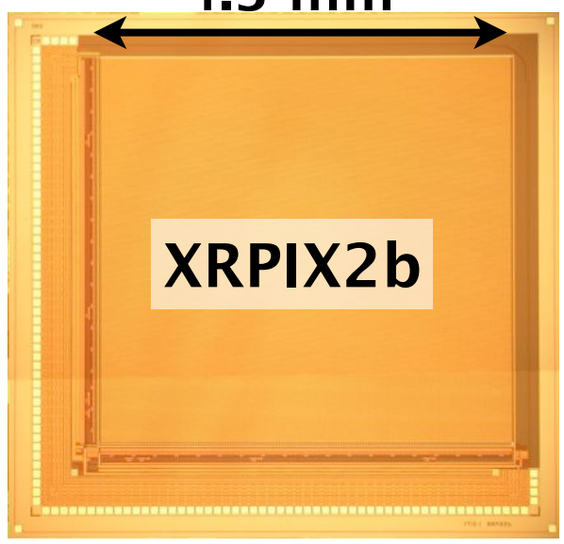


2.4 mm



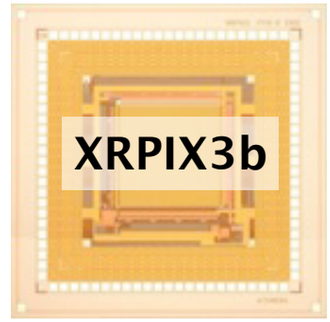
6.0 mm

Middle Size



6.0 mm

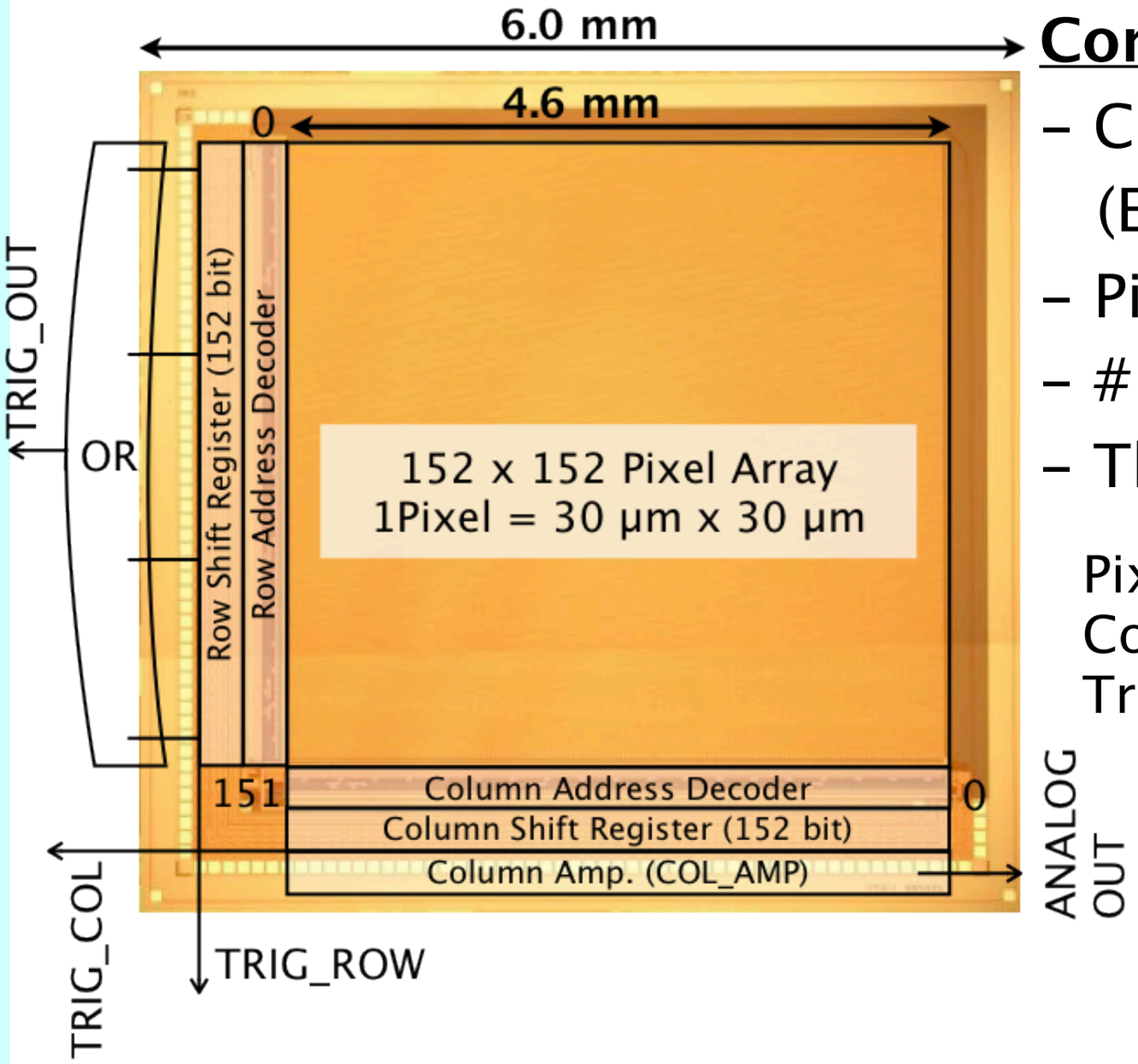
Buttable



Charge Sensitive
Amplifier

Design Specification : XRPIX2b

- Optimization of a pixel design / Confirmation of uniformity
  -> It is based on the design of XRPIX1/1b/2.



Components

- Chip size : 6.0 mm sq.
  (Effective area : ~ 4.6 mm sq.)
- Pixel size : 30 μm sq.
- # of pixel : 152 x 152 (~ 23k)
- Thickness of sensor layer : 260 μm

Pixel Circuit :
Correlated Double Sampling (CDS),
Trigger information output function.

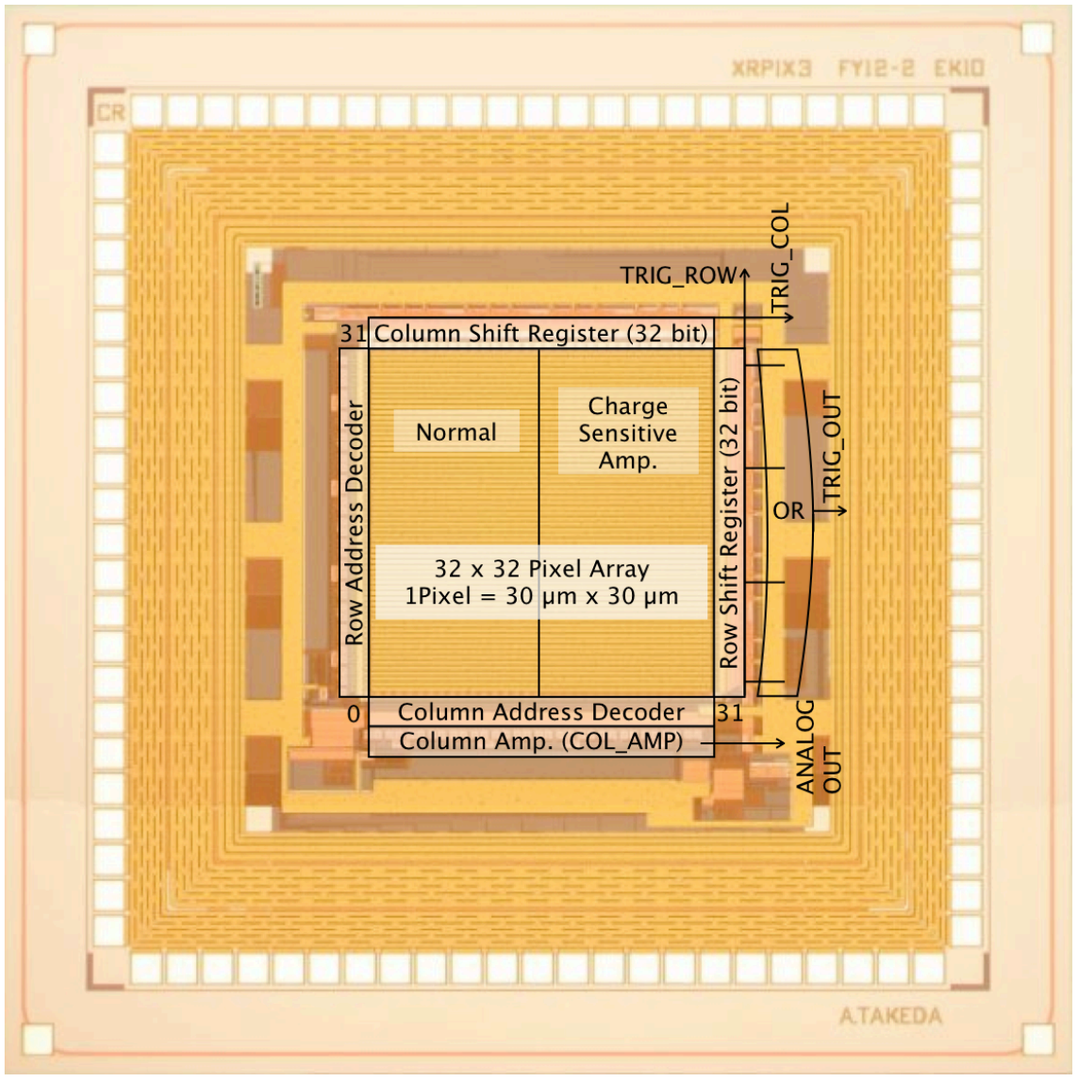
Design Specification : XRPIX3

Components

- Chip Size : 2.9 mm sq. (Effective Area : 1.0 mm sq.)
- Pixel Size : 30 um sq.
- # of Pixel : 32 x 32 (= 1,024)

  -> Normal : 32 x 16 (Left) , CSA : 32 x 16 (Right)

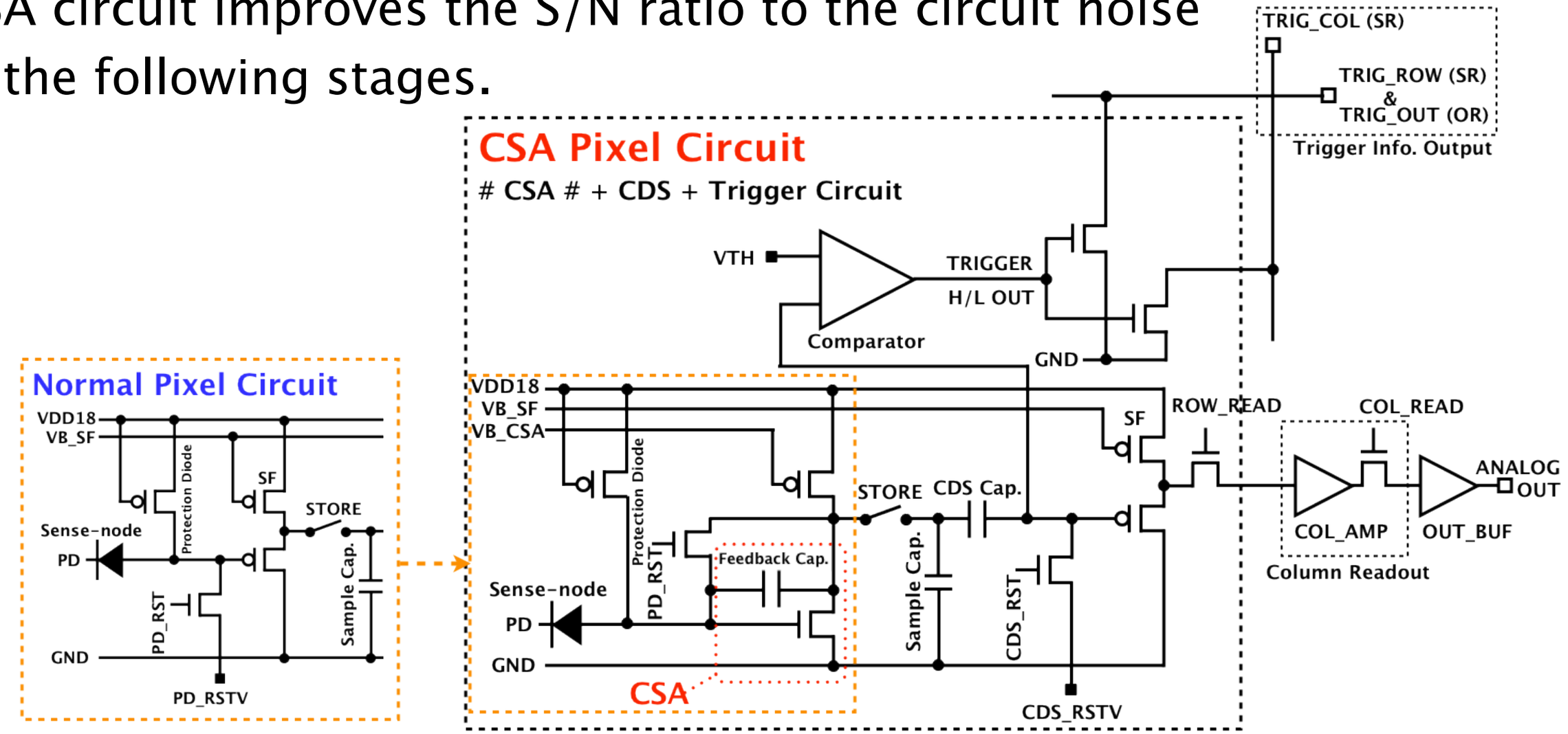
First prototype of XRPIX CSA circuit.
Comparison of Normal and CSA pixel.
(Fabricated Jun, 2013)



Pixel Circuit : XRPIX3

- Normal and CSA pixels have different circuit configuration of preceding stage.
  -> Normal : Source Follower (SF) by Common-Drain of a PMOS transistor (**the same circuit as XRPIX2b**)
  -> CSA : pre-amplifier by Common-Source of a NMOS transistor and a feedback capacitance (1 fF)

CSA circuit improves the S/N ratio to the circuit noise in the following stages.



Normal and CSA Circuit Calibration

- Calibration plot by ^{55}Fe and ^{109}Cd.
- The pixel circuit with CSA works good. (3.4 times higher gain)

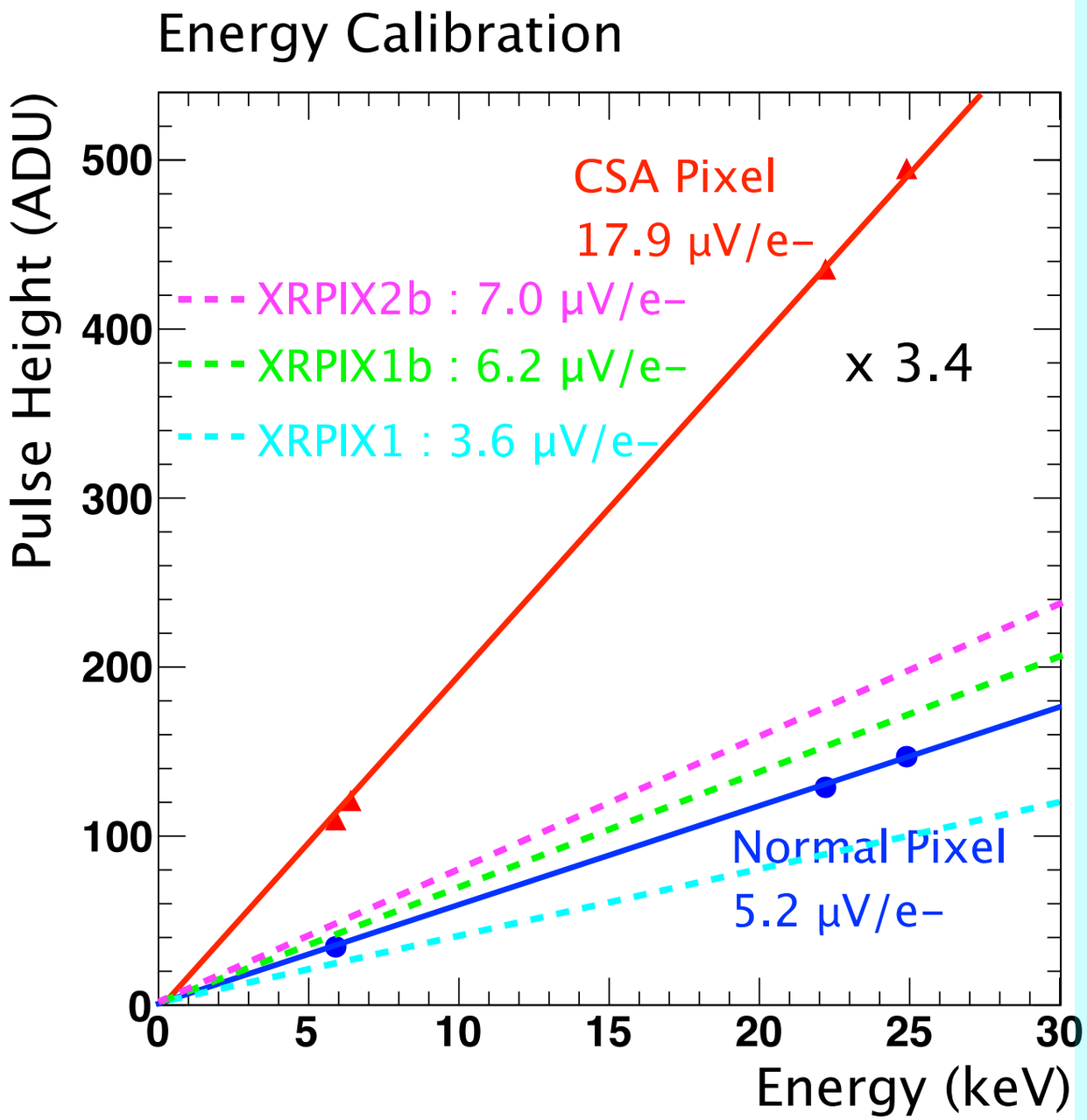
Gain

Normal : 5.2 μV/e-

CSA : 17.9 μV/e-

Since parasitic capacitance of sense node increased, the gain fell from XRPIX2b by XRPIX3.

Observed gain (17.9 μV/e-) is lower than the design (50 μV/e-), which would be due to parasitic capacitance.

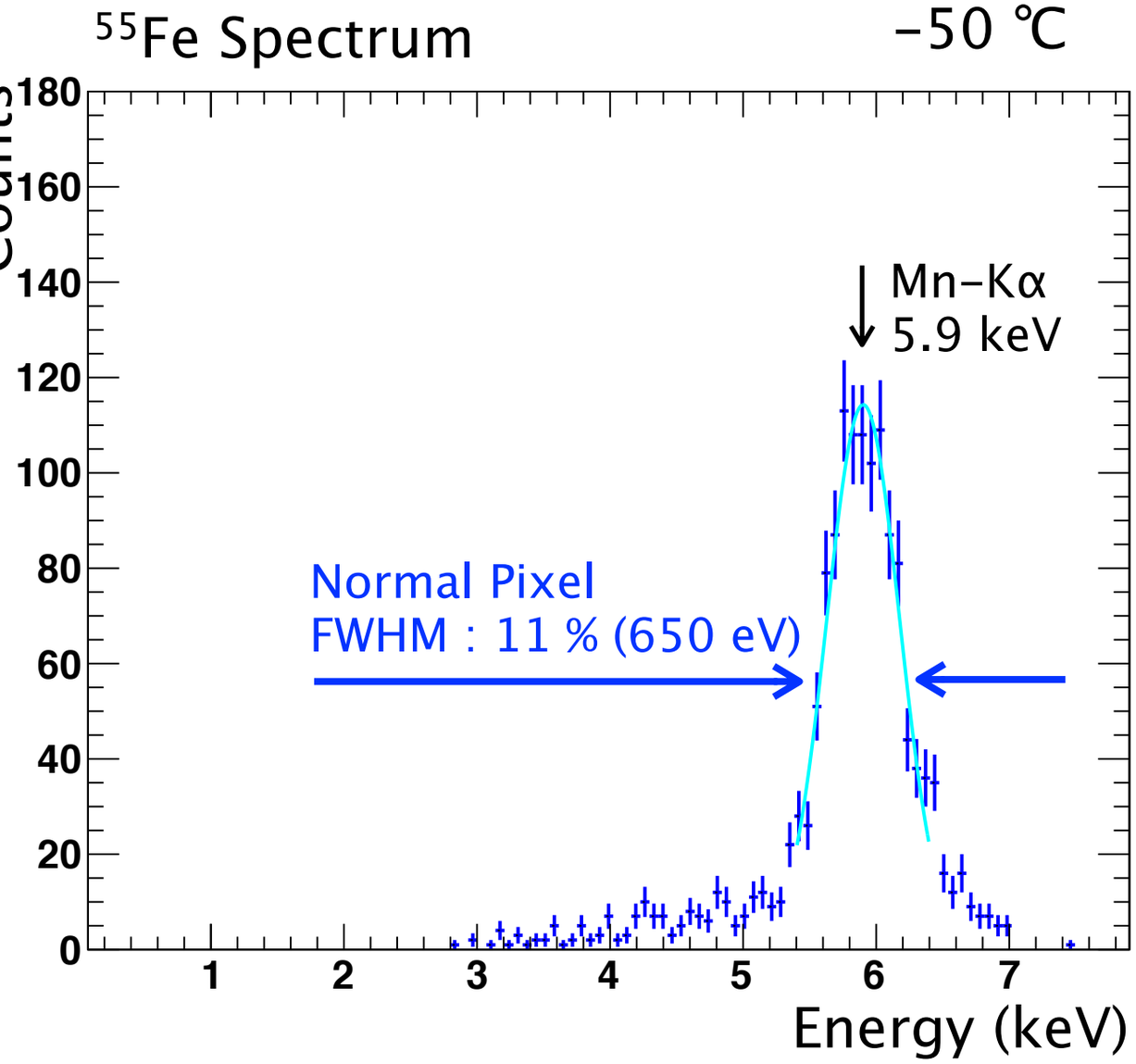


1 Analog Digital Unit (ADU) = 244 μV (= 1 V / 12 bit)

Comparison of Normal and CSA Pixel

- The CSA Pixel succeeded in improvement of energy resolution.
  Comparison of ^{55}Fe energy spectrum at Normal and CSA
  (obtain by Frame readout mode, not use Event-Driven)
  -> Readout noise (-> obtained from the pedestal peak)
    Normal : 76 e- (rms)

  -> Mn-Kα @ 5.9 keV
    Normal : 650 eV / 11 % (FWHM)



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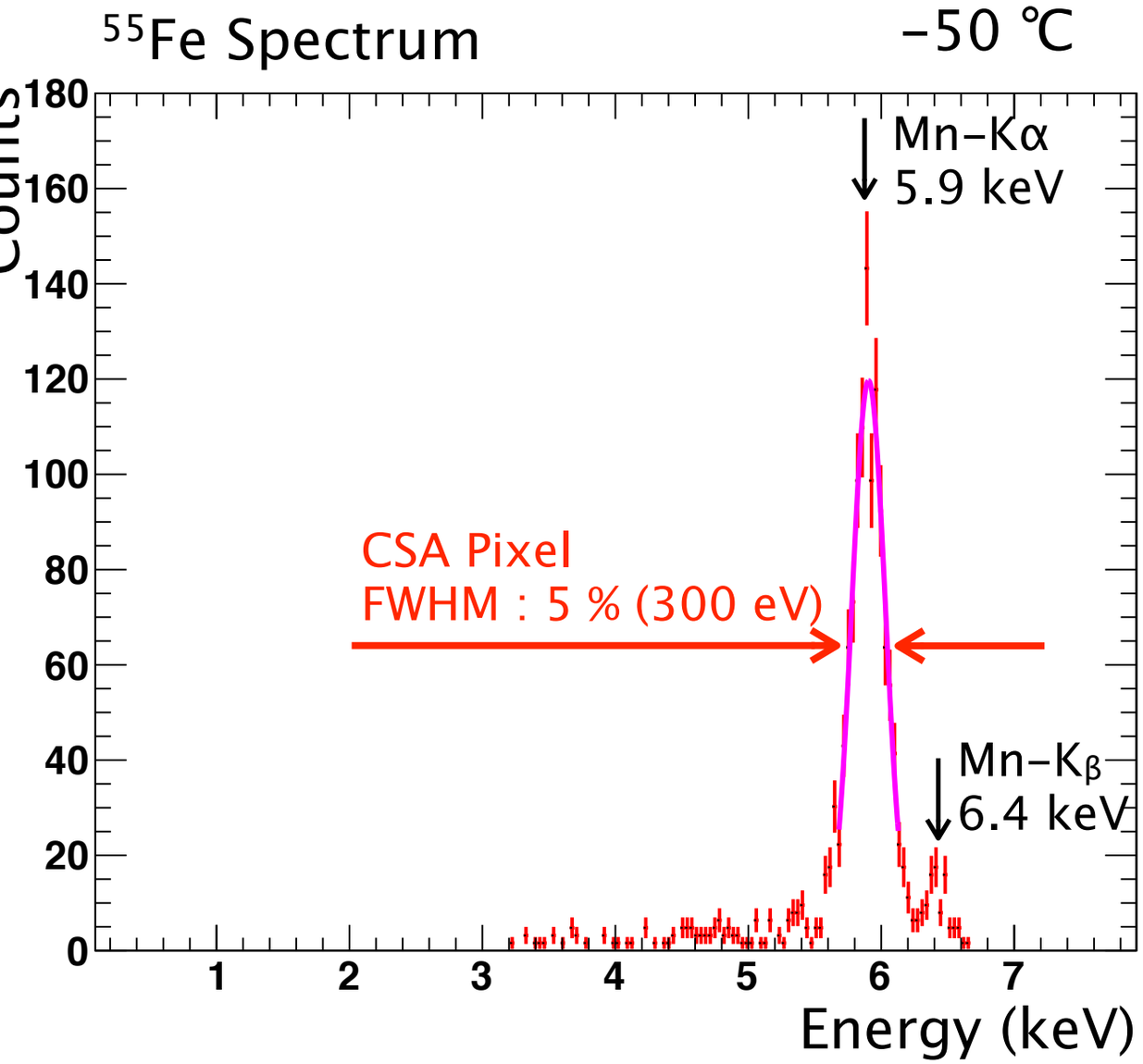
  Comparison of ^{55}Fe energy spectrum at Normal and CSA
  (obtain by Frame readout mode, not use Event-Driven)
  -> Readout noise (-> obtained from the pedestal peak)
    Normal : 76 e- (rms)
    CSA : 33 e- (rms)
  -> Mn-Kα @ 5.9 keV
    Normal : 650 eV / 11 % (FWHM)
    CSA : 300 eV / 5 % (FWHM)

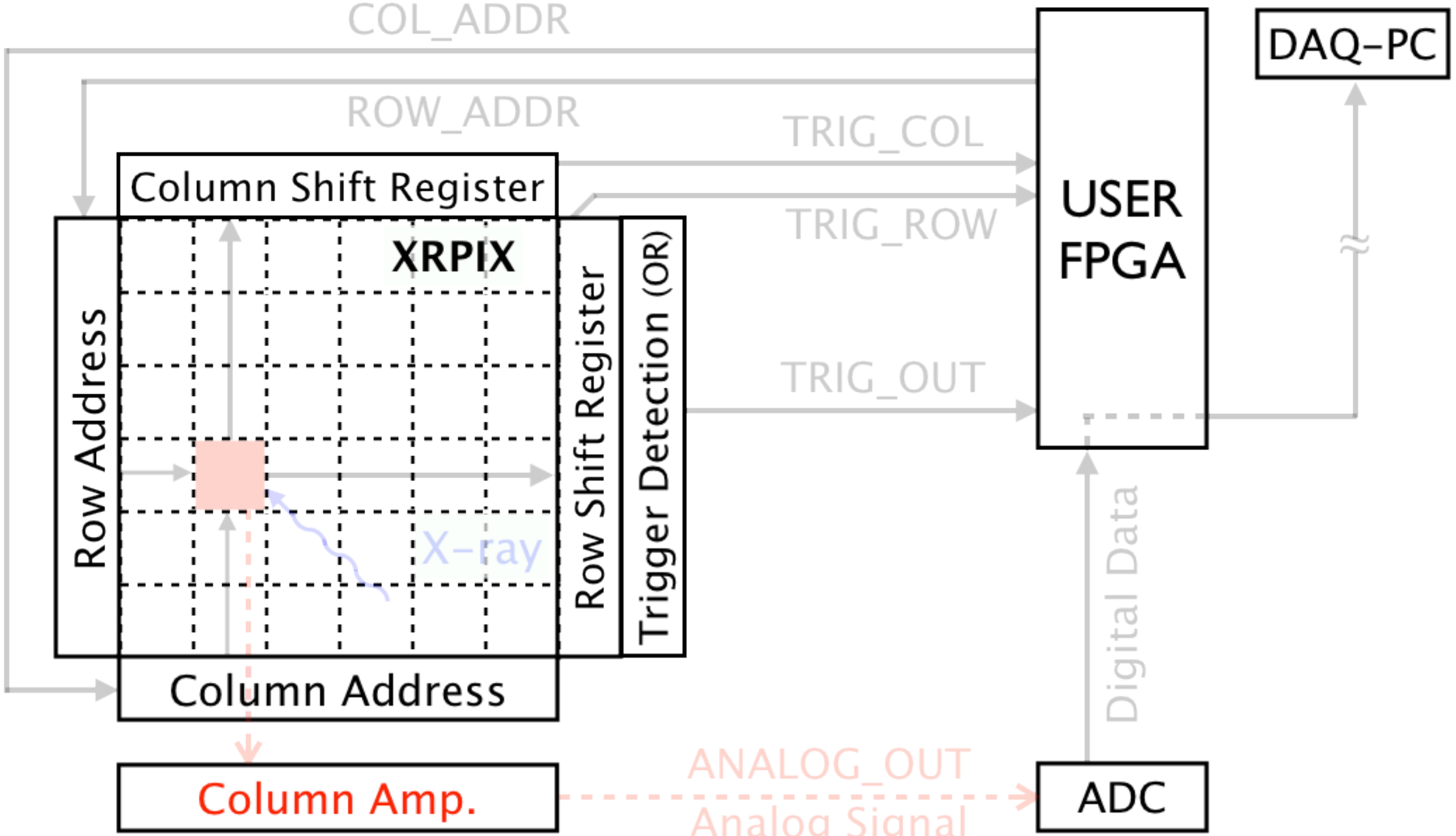
Resolved Mn-K_α and Mn-K_β successfully by CSA circuit !
-> Improvement of spectrum performance

We achieve the target readout noise 10 e- (rms) by optimization of CSA circuit.



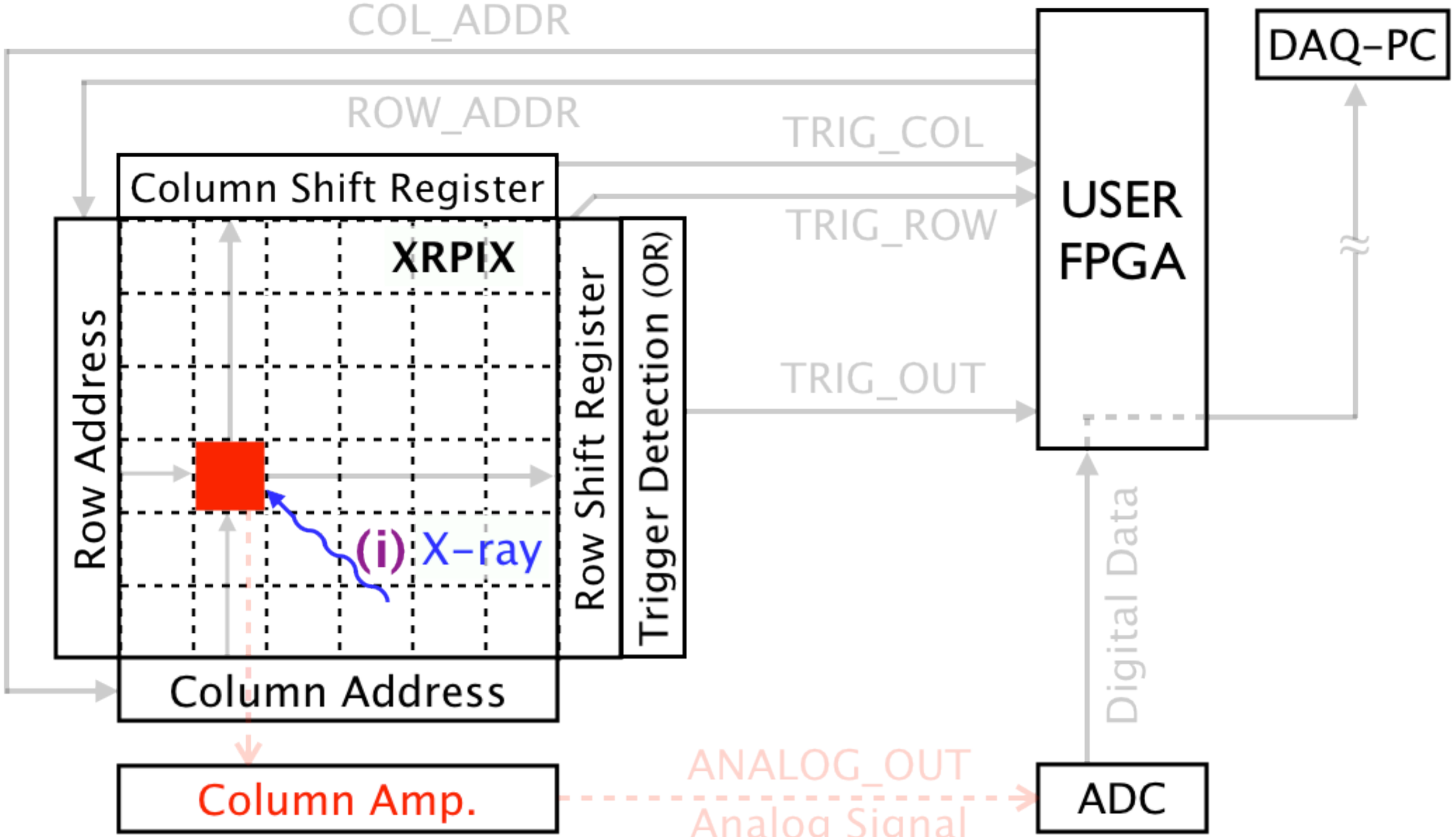
Event-Driven Readout Mode

- The following figure show the flow chart.



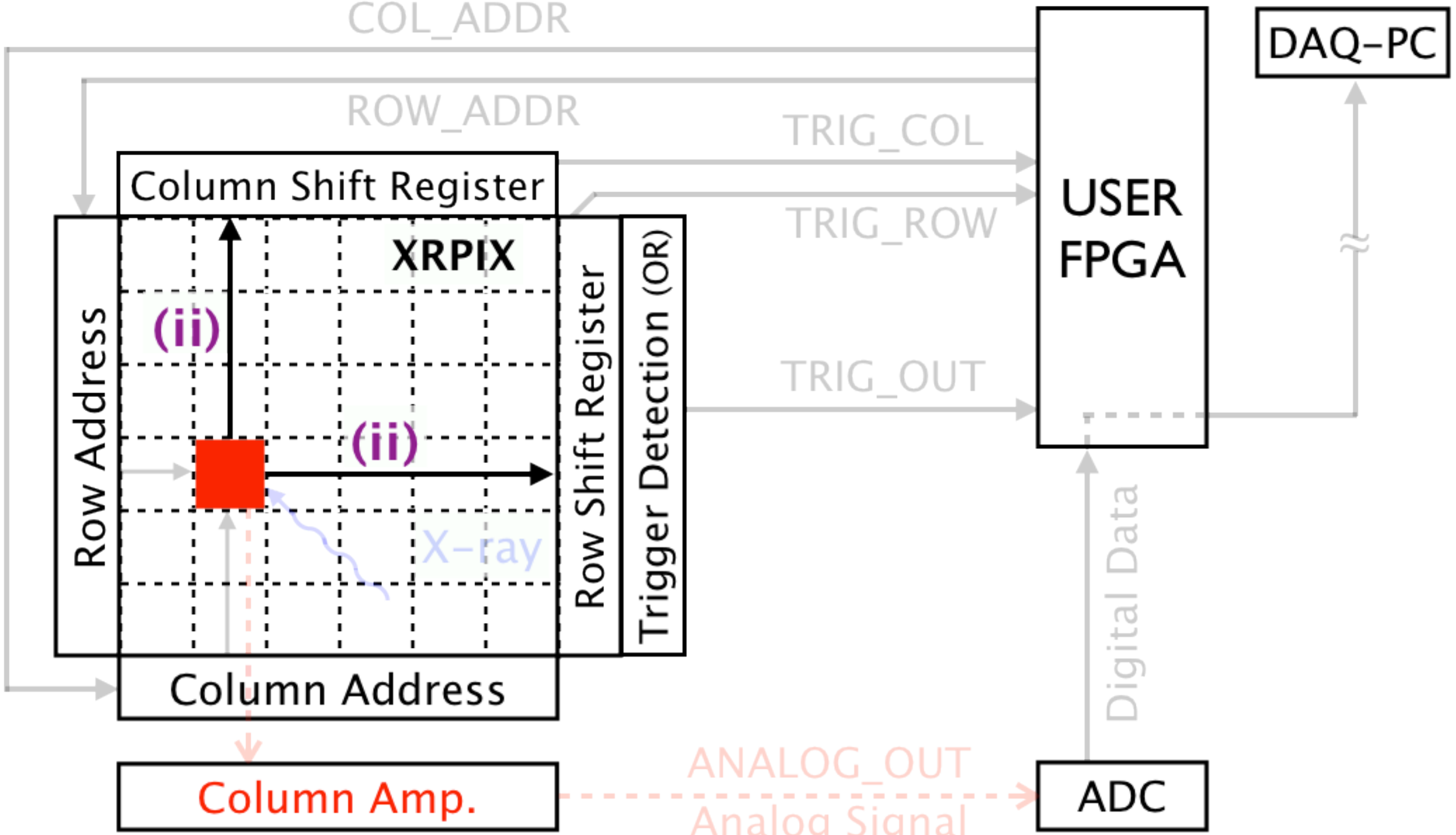
Event-Driven Readout Mode

(i) X-ray signal is detected by a pixel.



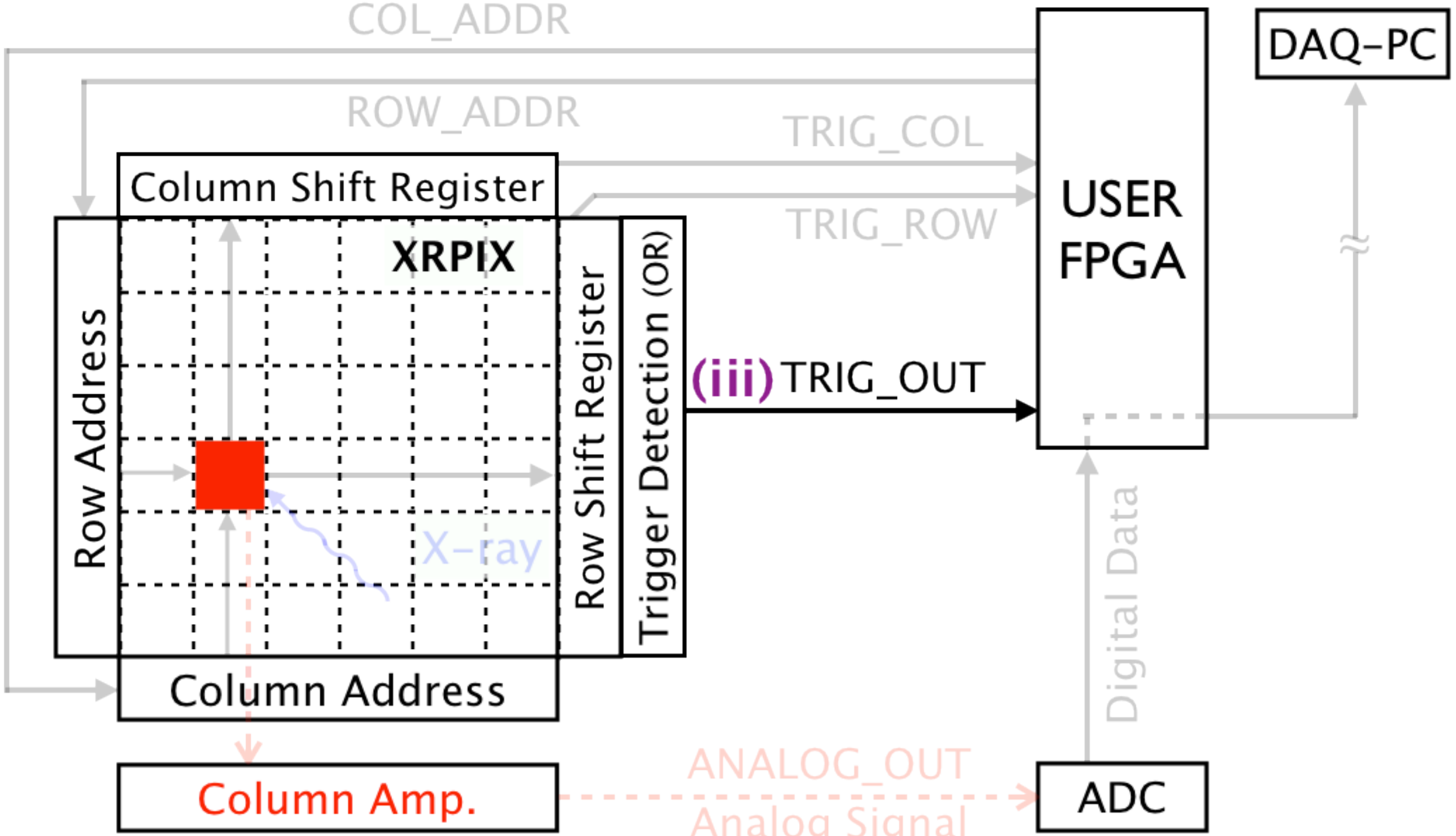
Event-Driven Readout Mode

(ii) If the X-ray signal exceeds a threshold voltage, trigger signals are transferred to row and column direction.



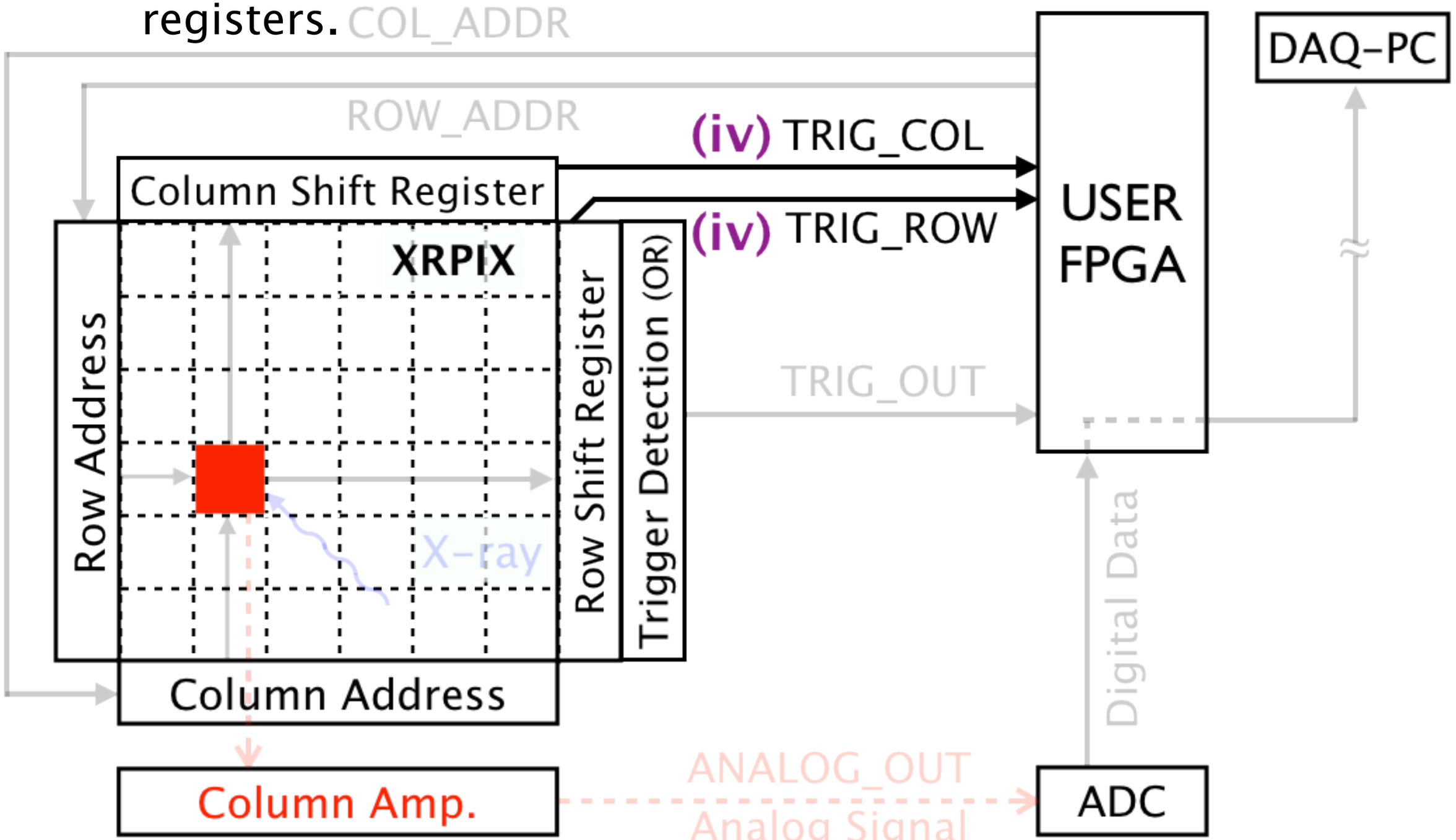
Event-Driven Readout Mode

(iii) OR'ed signal (TRIG_OUT) of the trigger is generated.



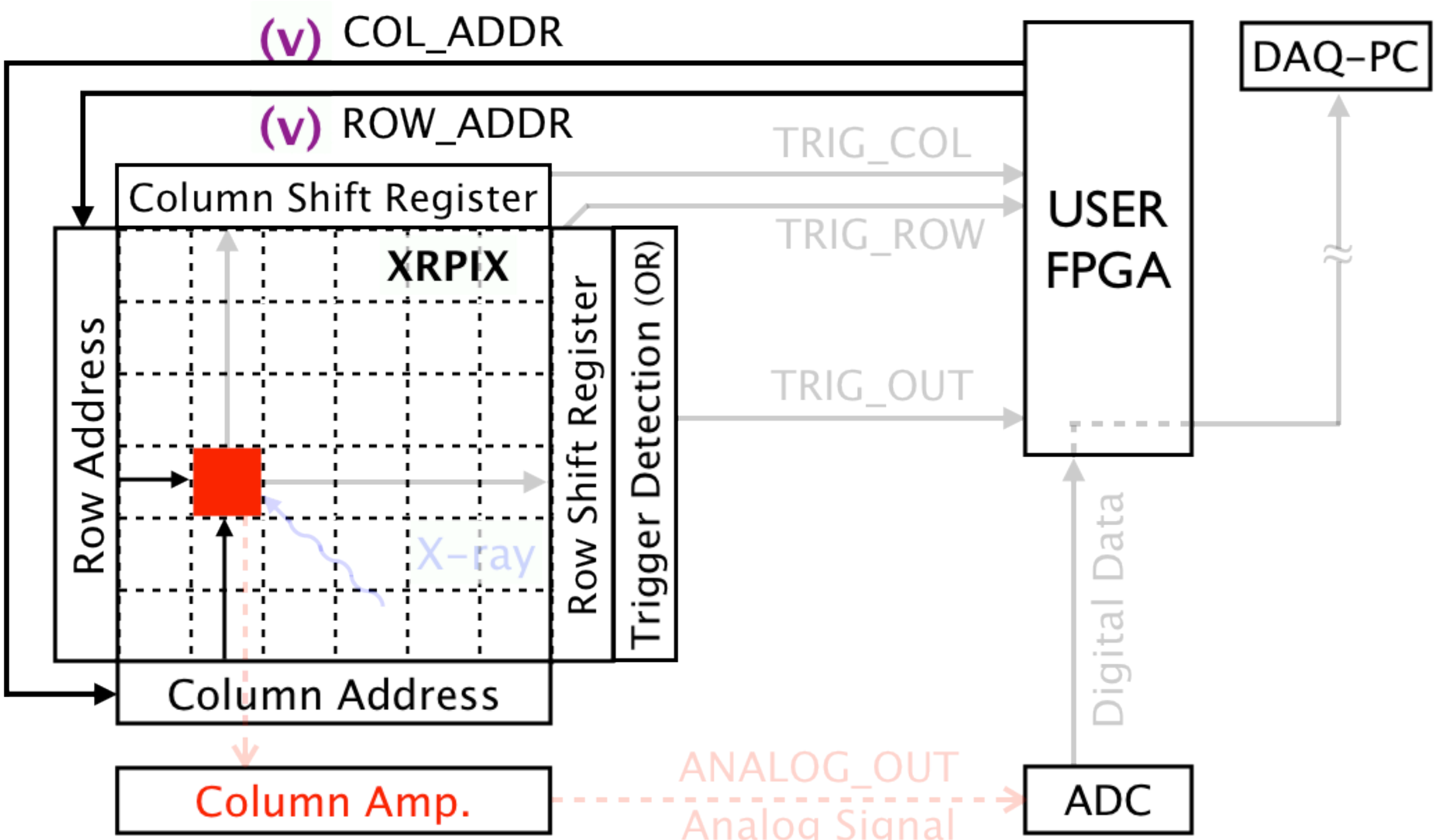
Event-Driven Readout Mode

(iv) By receiving the TRIG_OUT signal, USER-FPGA start to read the hit address information from the row and column shift registers.



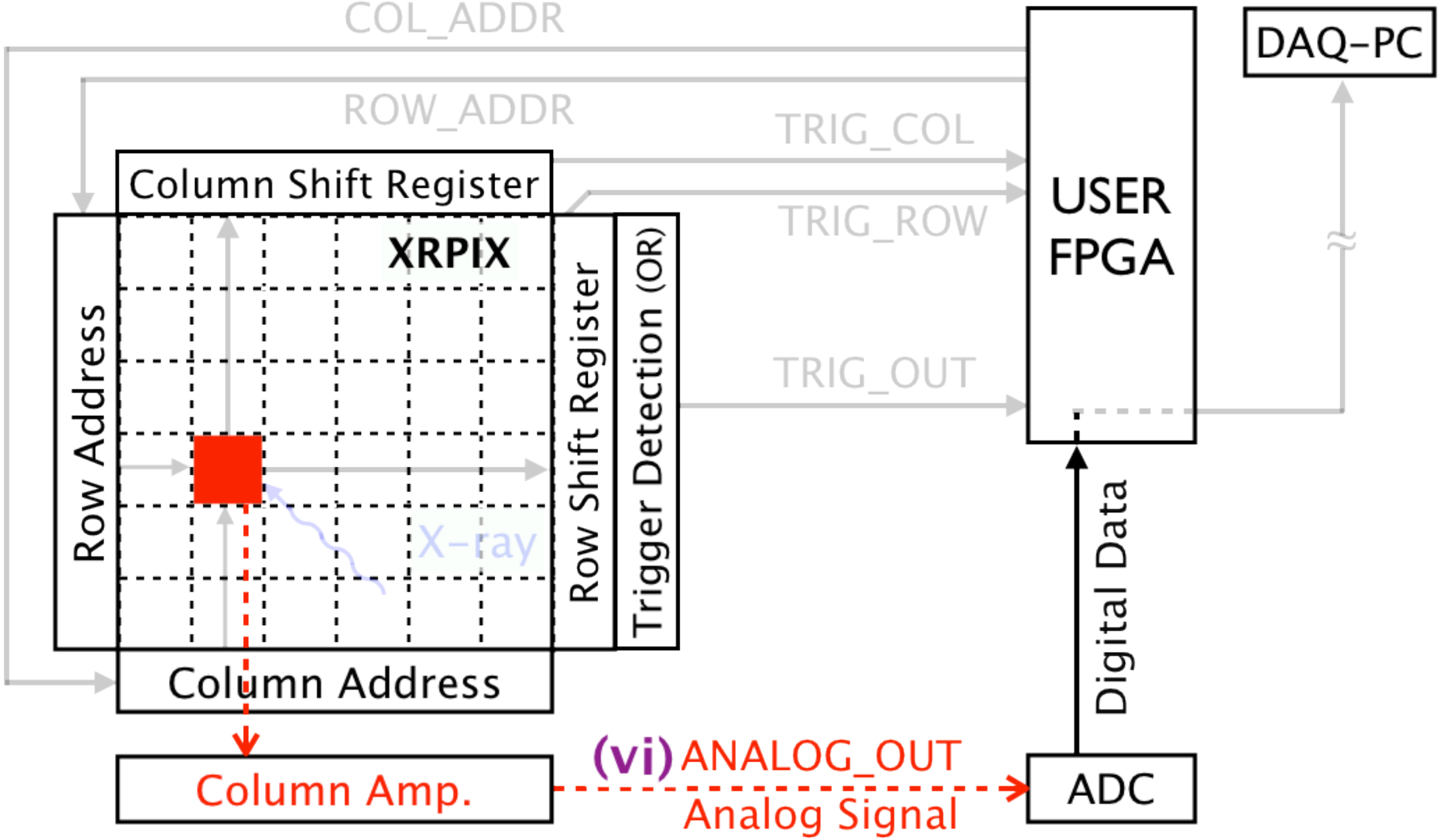
Event-Driven Readout Mode

(v) The USER-FPGA accesses the hit pixel directly by asserting the obtained address.



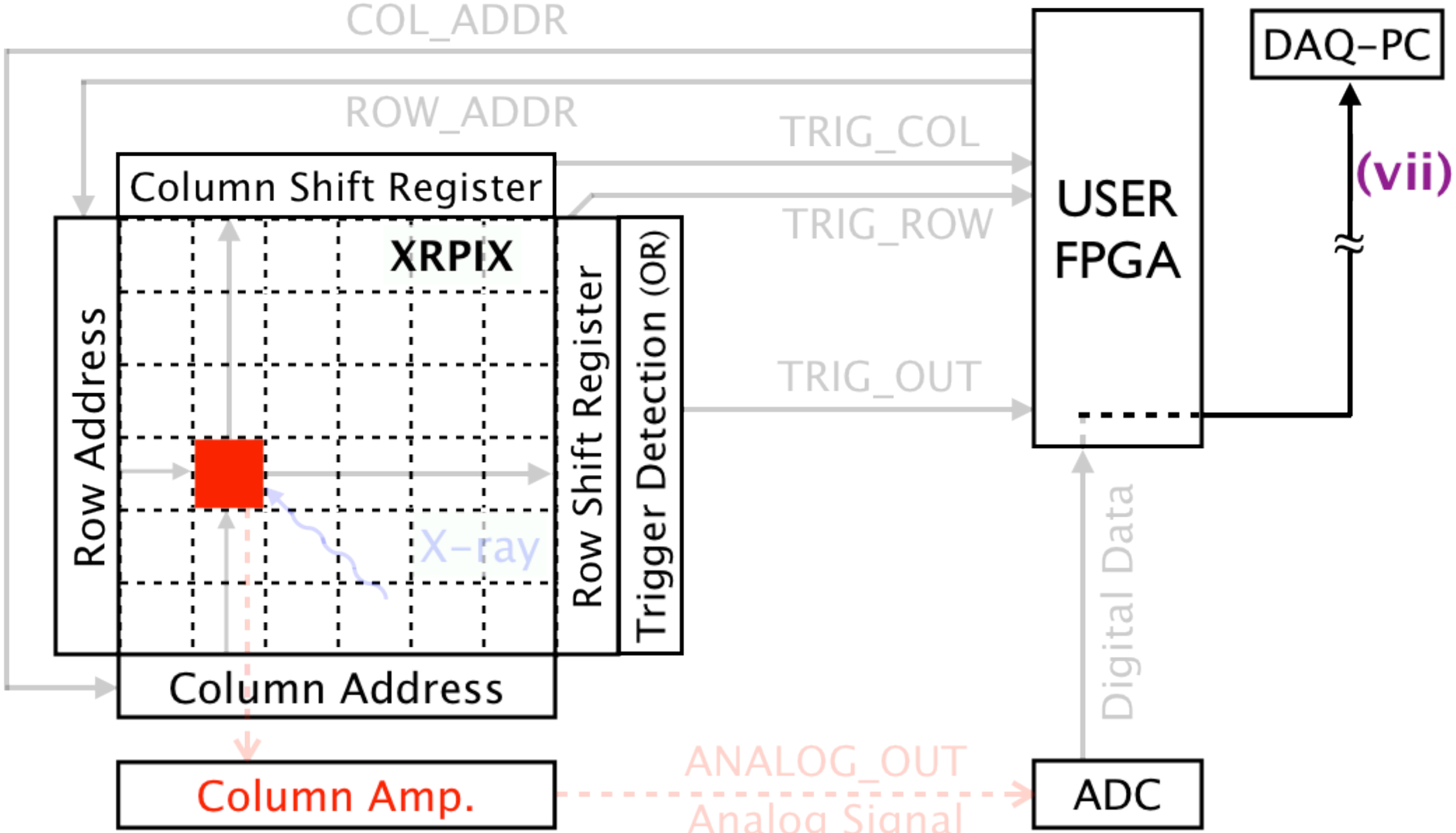
Event-Driven Readout Mode

(vi) The USER-FPGA reads out the analog voltage (signal and pedestal levels) through the ADC.



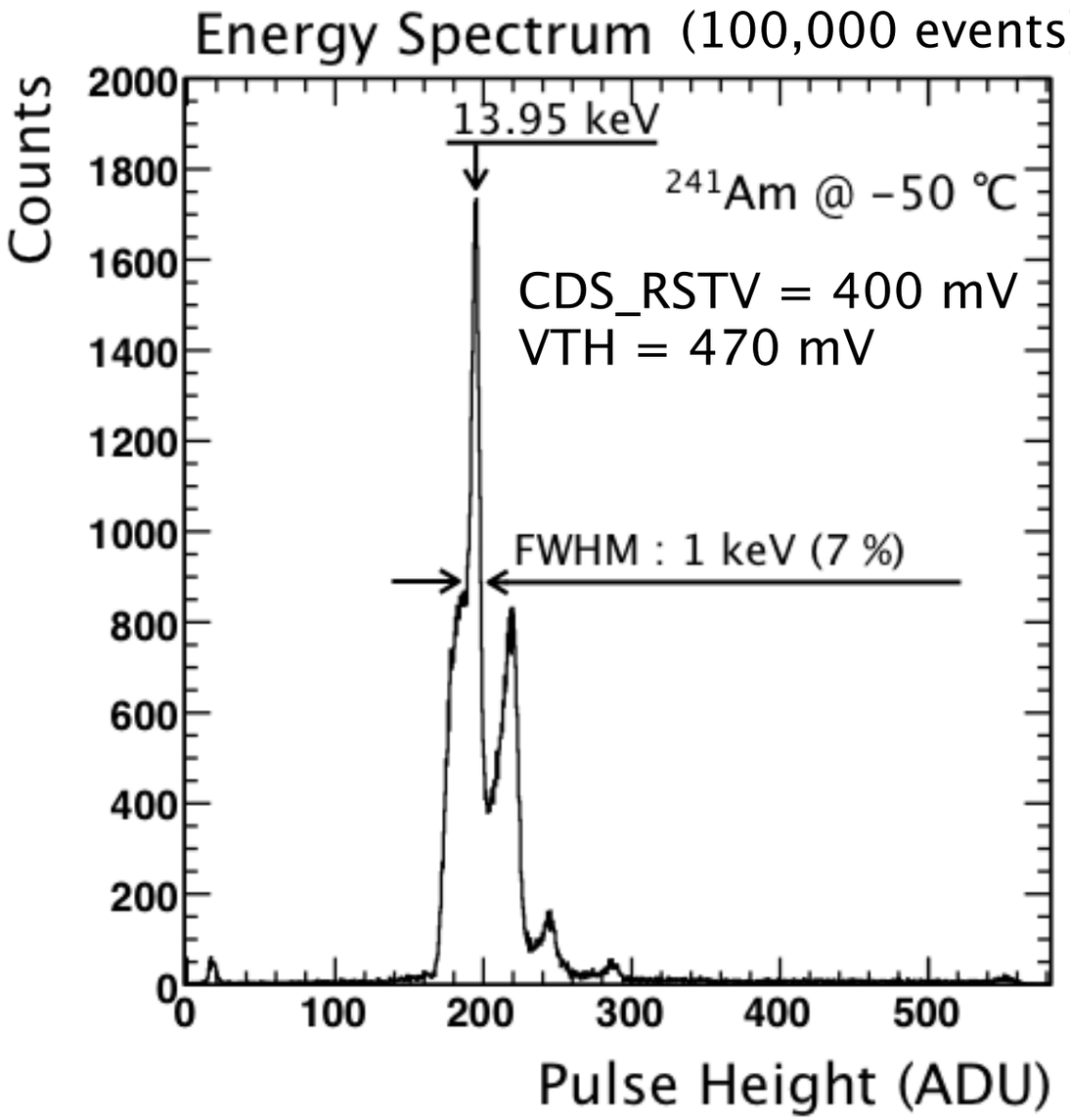
Event-Driven Readout Mode

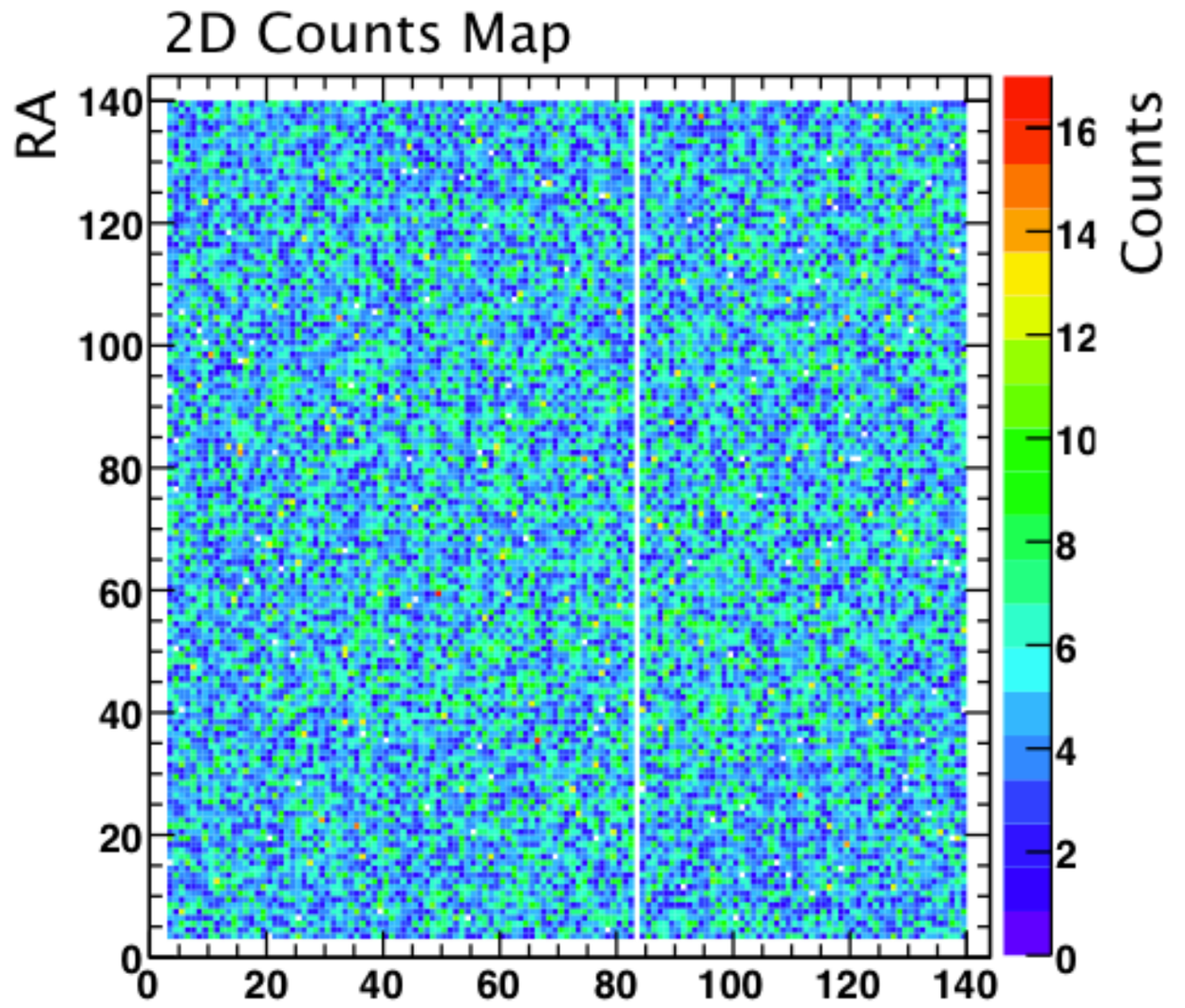
(vii) Finally, the obtained digital data is transmitted to the DAQ-PC.



Event-Driven Spectrum by XRPIX2b

- X-ray spectrum by event-driven readout mode.
  -> Capacity of event rate > 1 kHz.
- FWHM : 1 keV (7 %) @ 13.95 keV
  -> It is not good compared with Frame readout mode.
  (We already understand this reason.)





Bad pixel mask set :
-> 4 pixels of the surround / CA88 line

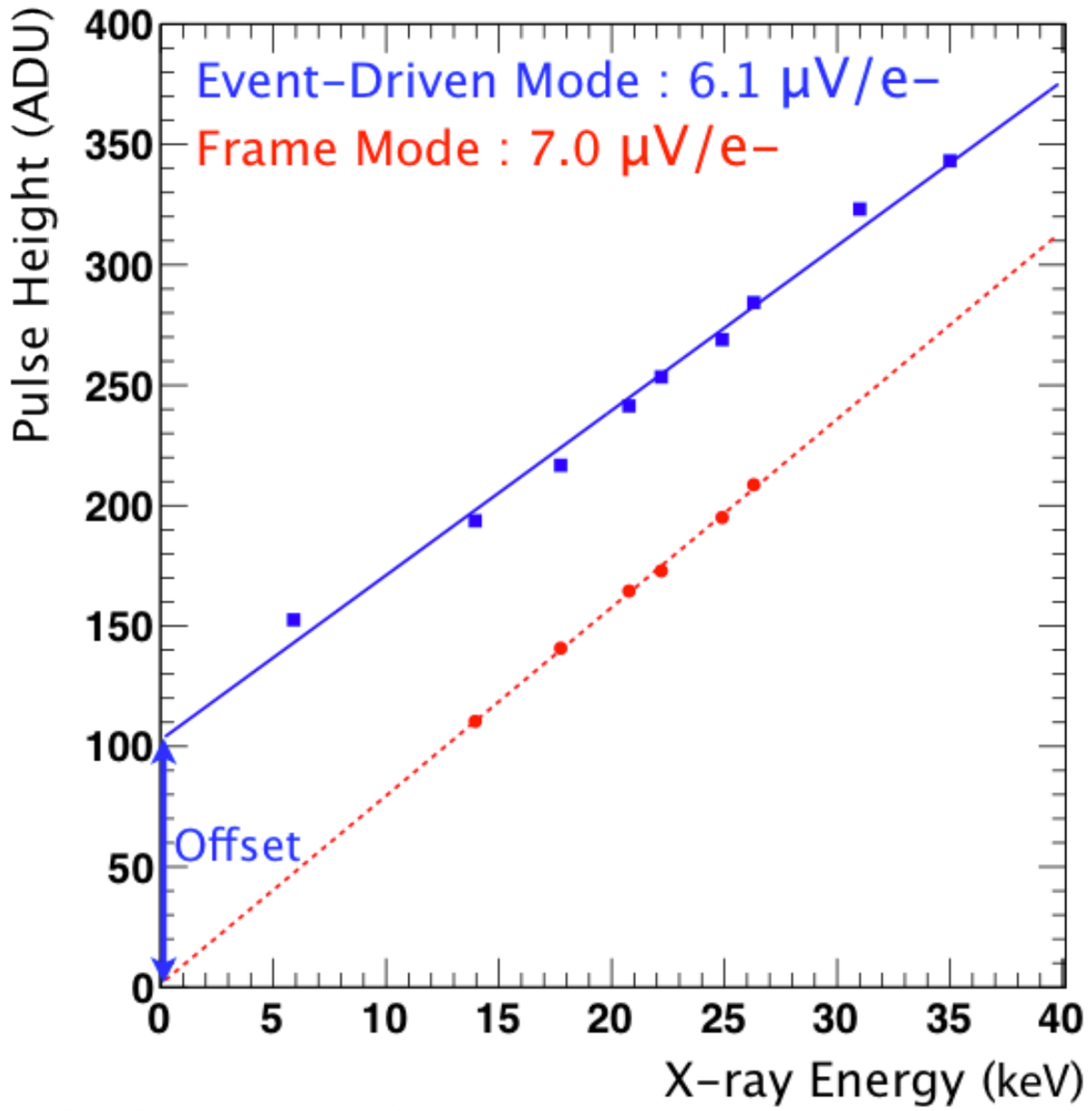
Event-Driven Calibration

- Calibration plot by ^{55}Fe, ^{241}Am, ^{109}Cd, and ^{133}Ba

some problems

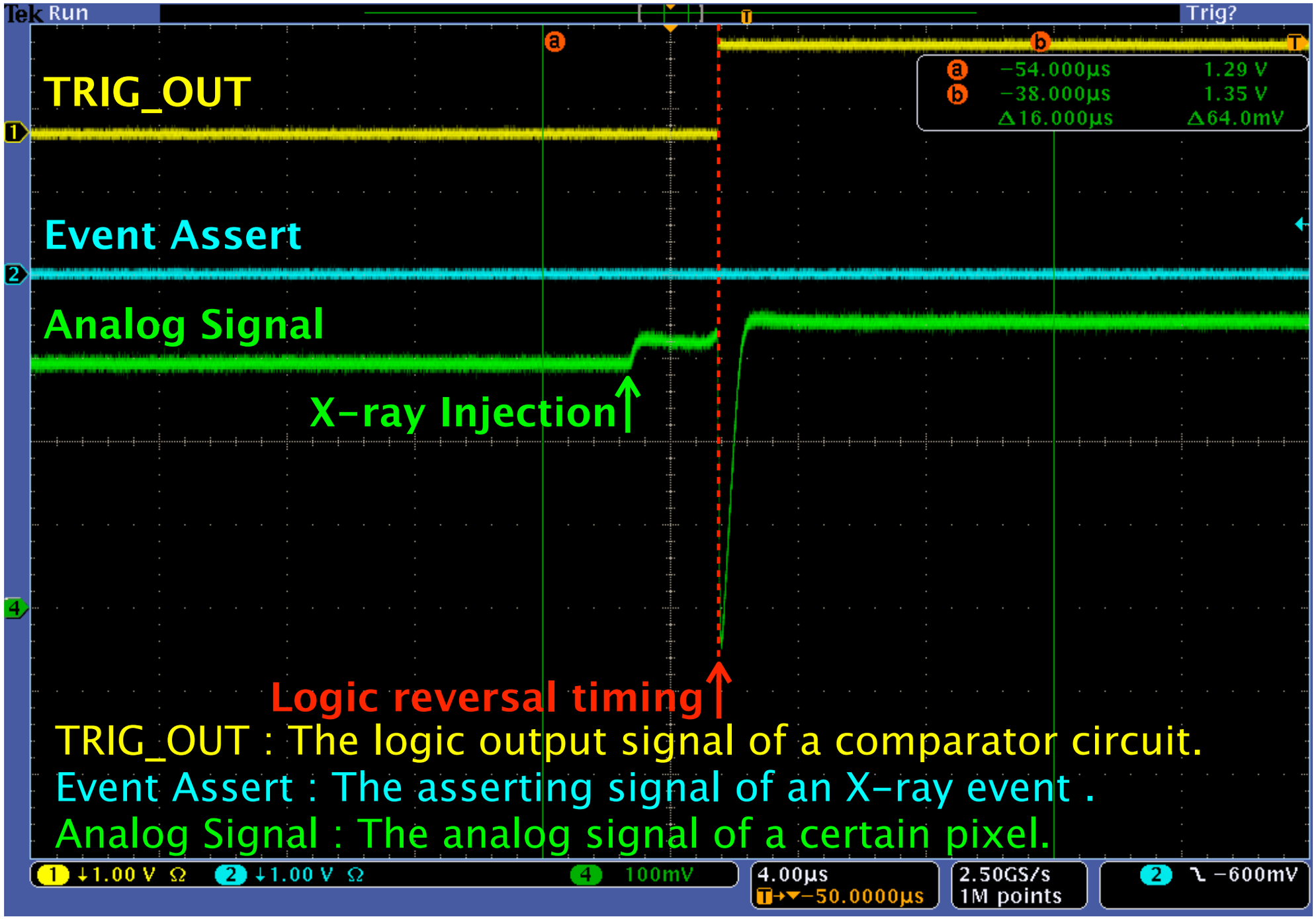
-> The gain is different. / There is offset.

The linearity of fitting decreases and variation is large.
(There is a problem in a comparator circuit. -> modification is required...)



What happens by X-ray injection?

- The waveform of an oscilloscope when X-rays enter (^{109}Cd : 22.2 keV).
  -> The analog signal has 4 problems.



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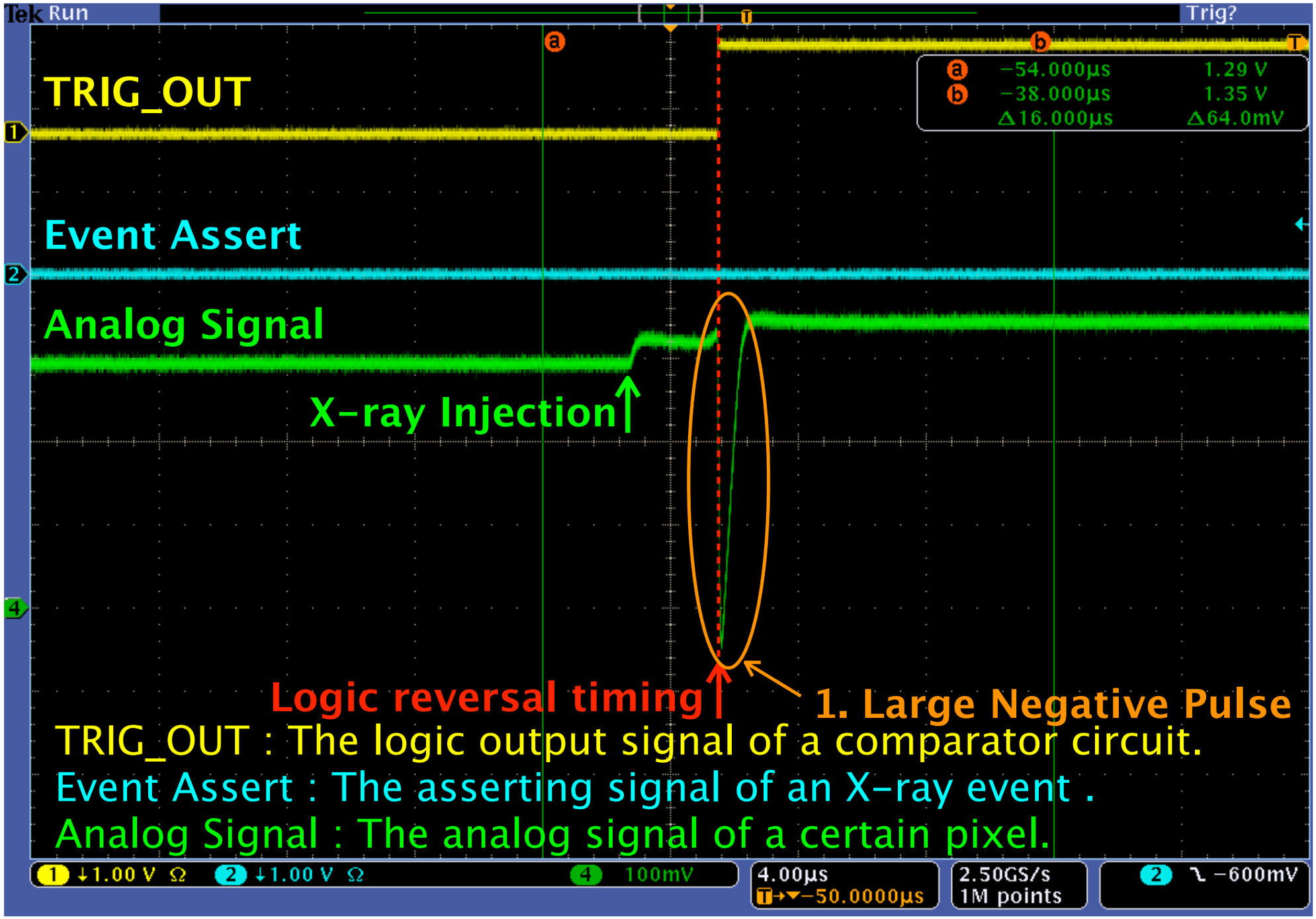

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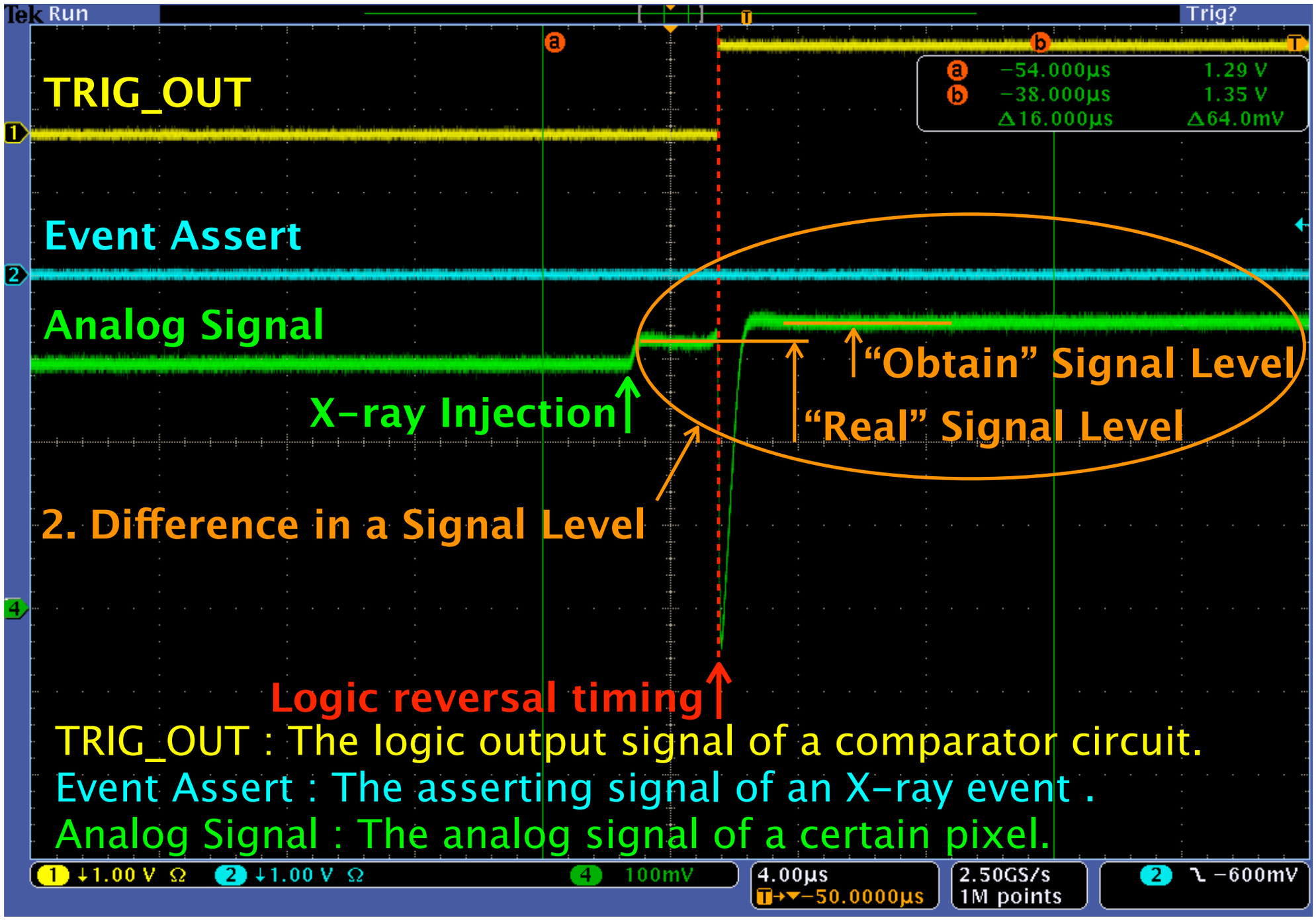

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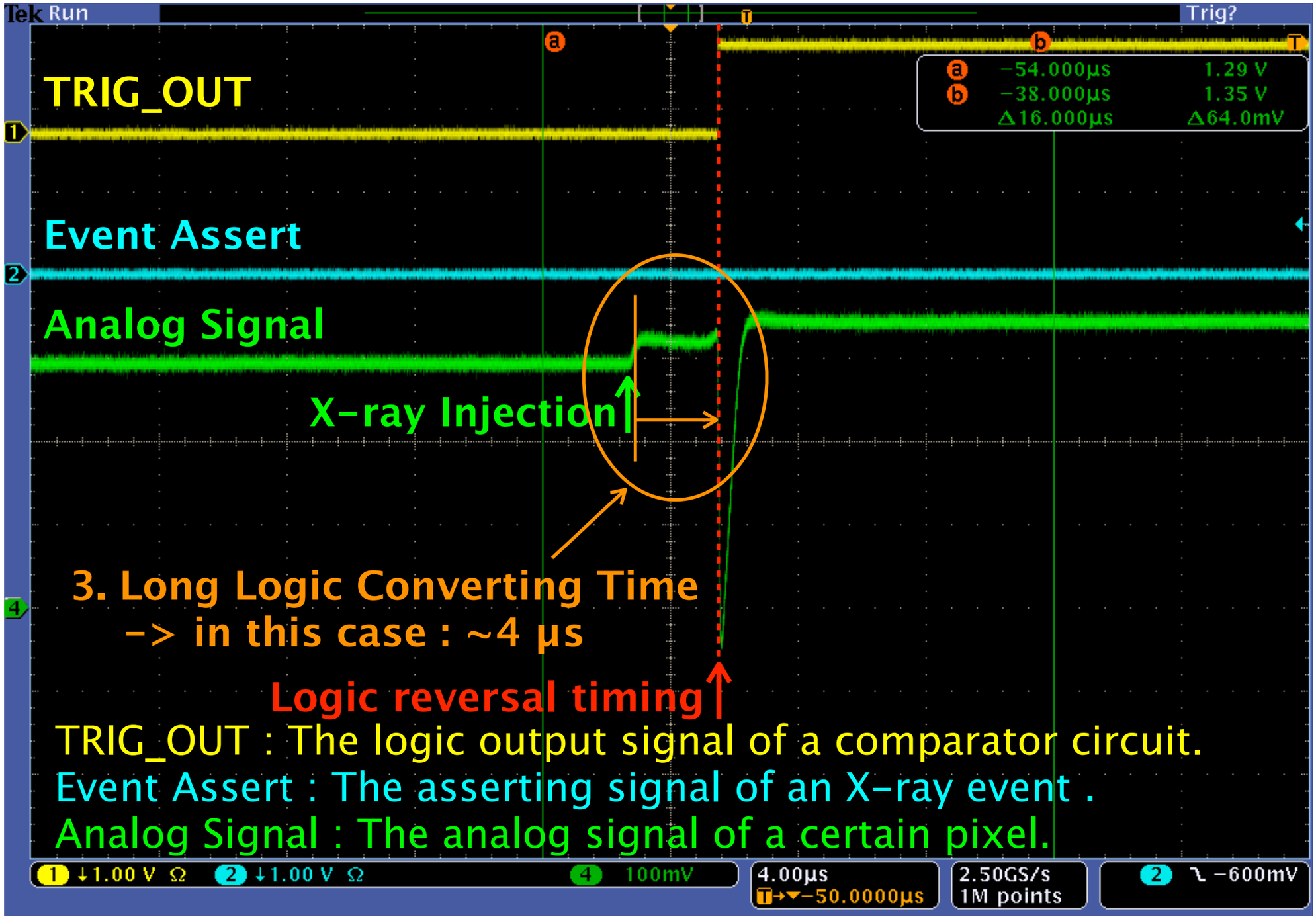

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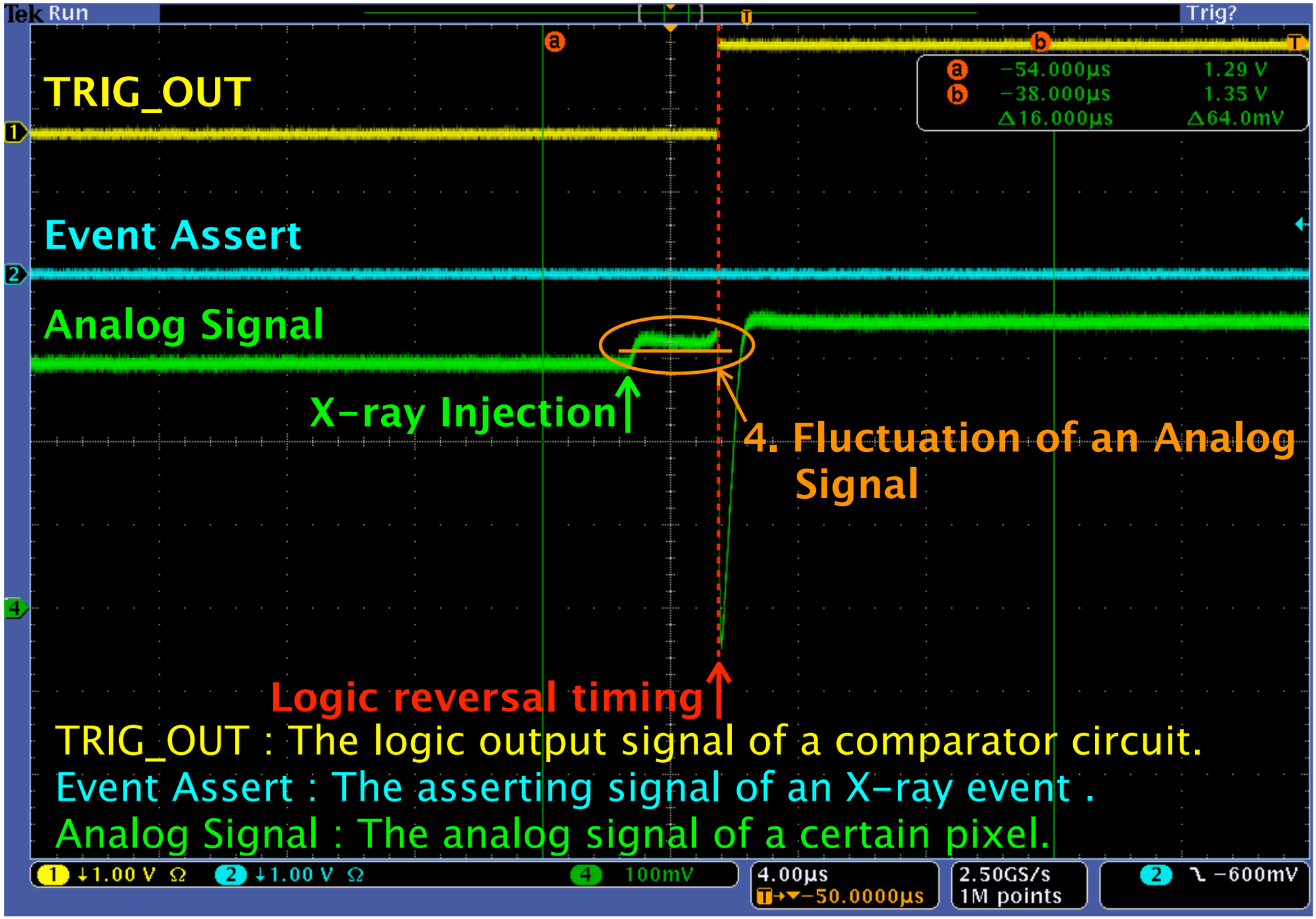
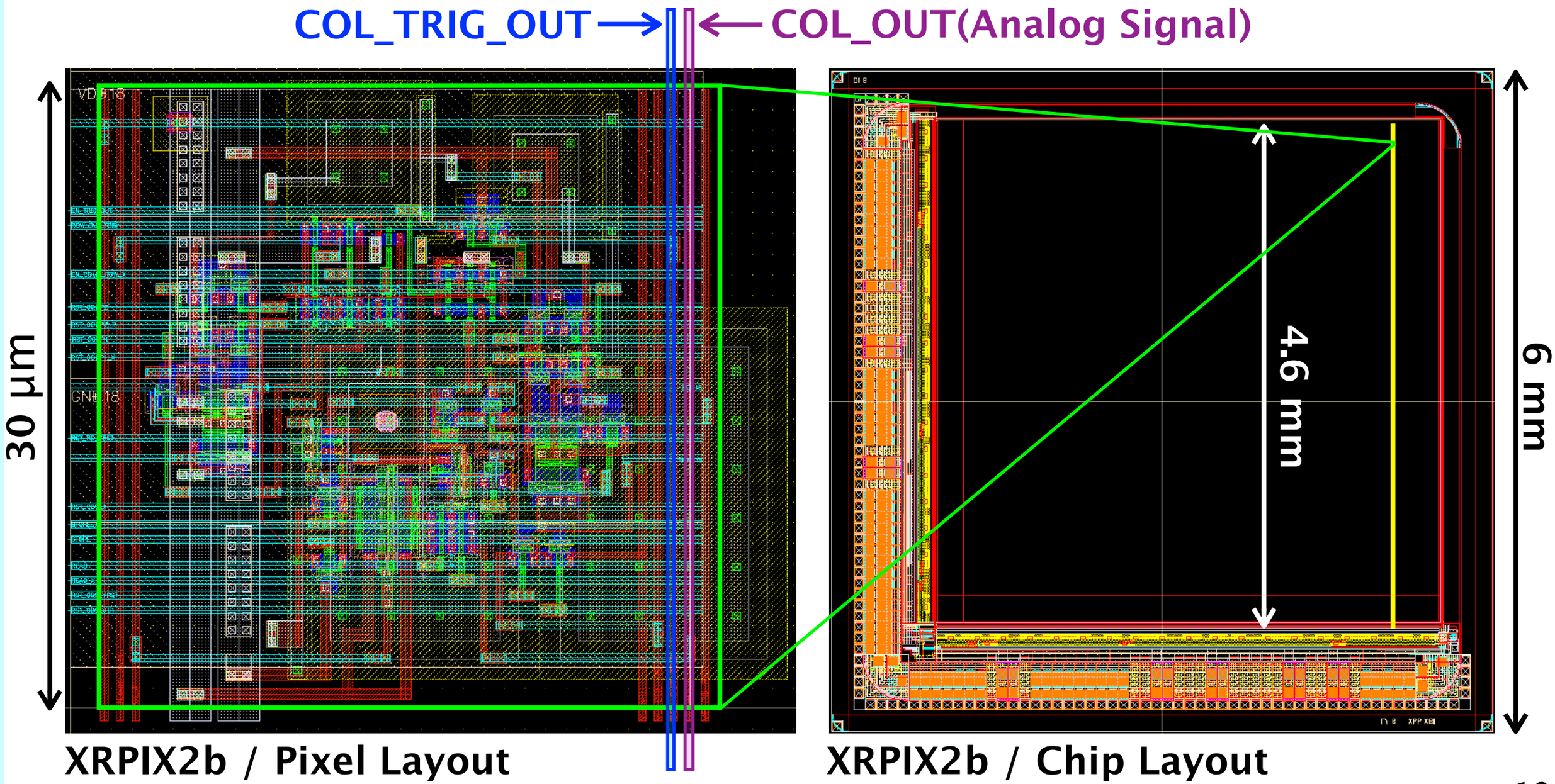


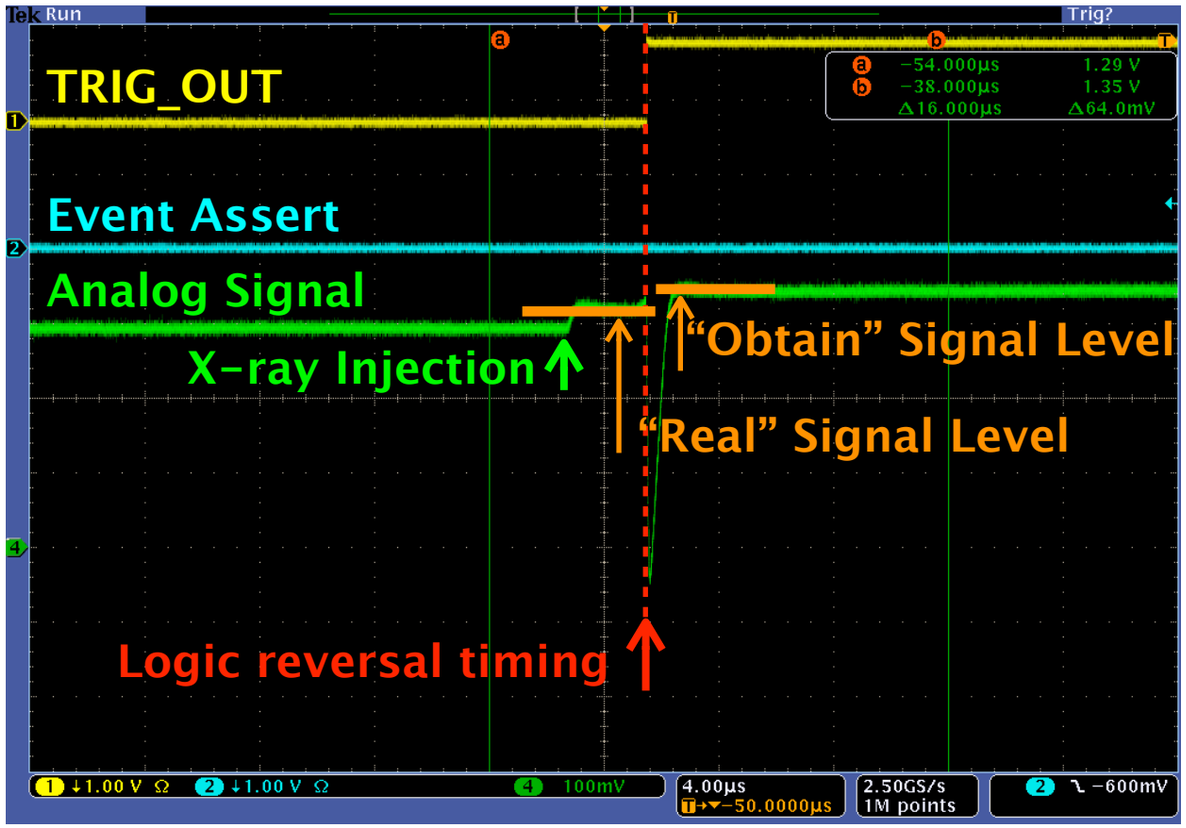
1. Reason for Negative Pulse

- Wiring of an analog signal line (COL_OUT) and a trigger signal (COL_TRIG_OUT) adjoined each other with the pixel layout. (Distance : 0.4 μm, Length : 4.6 mm)
  -> This has large parasitic capacitance by wiring (~ 50 fF).
- This is the phenomenon of appearing only when a pixel is specified and observed.
  -> It has checked also by HSpice simulation.



2. About the Difference in a Signal Level

- The reason for a cause is not understand yet.



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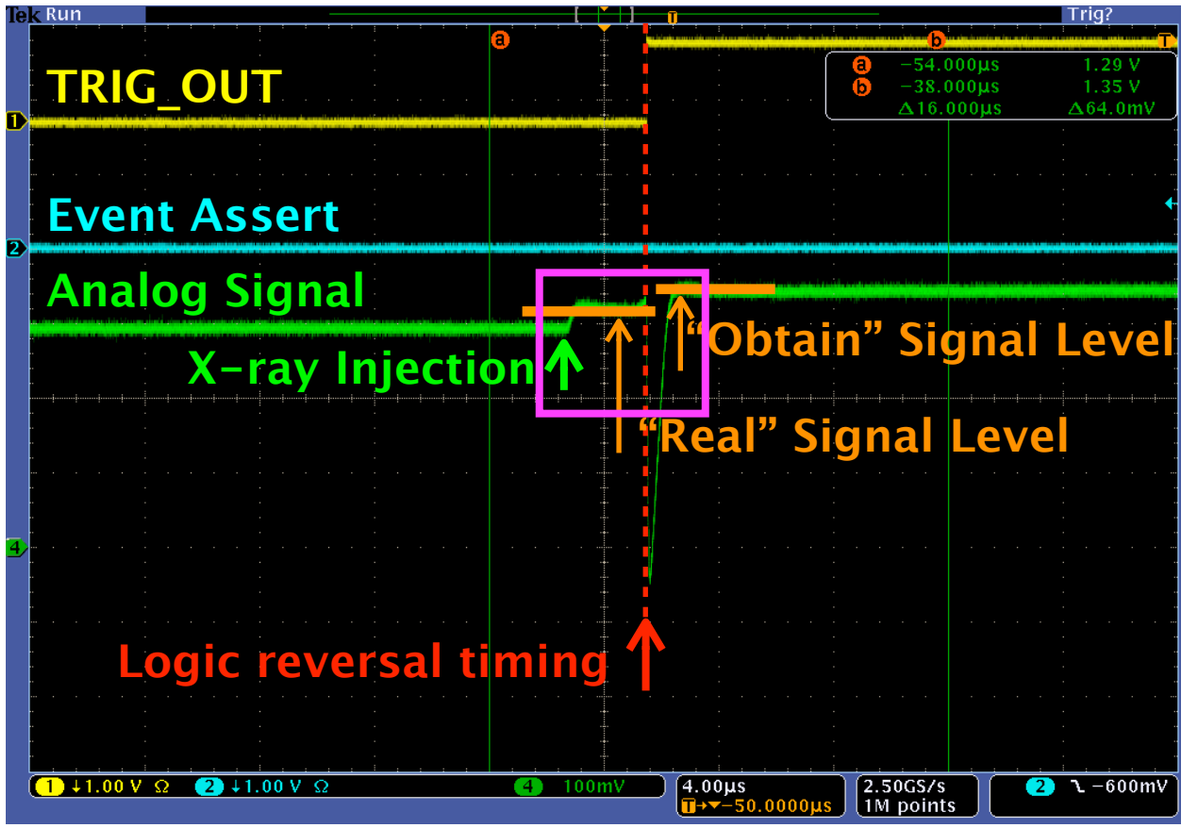
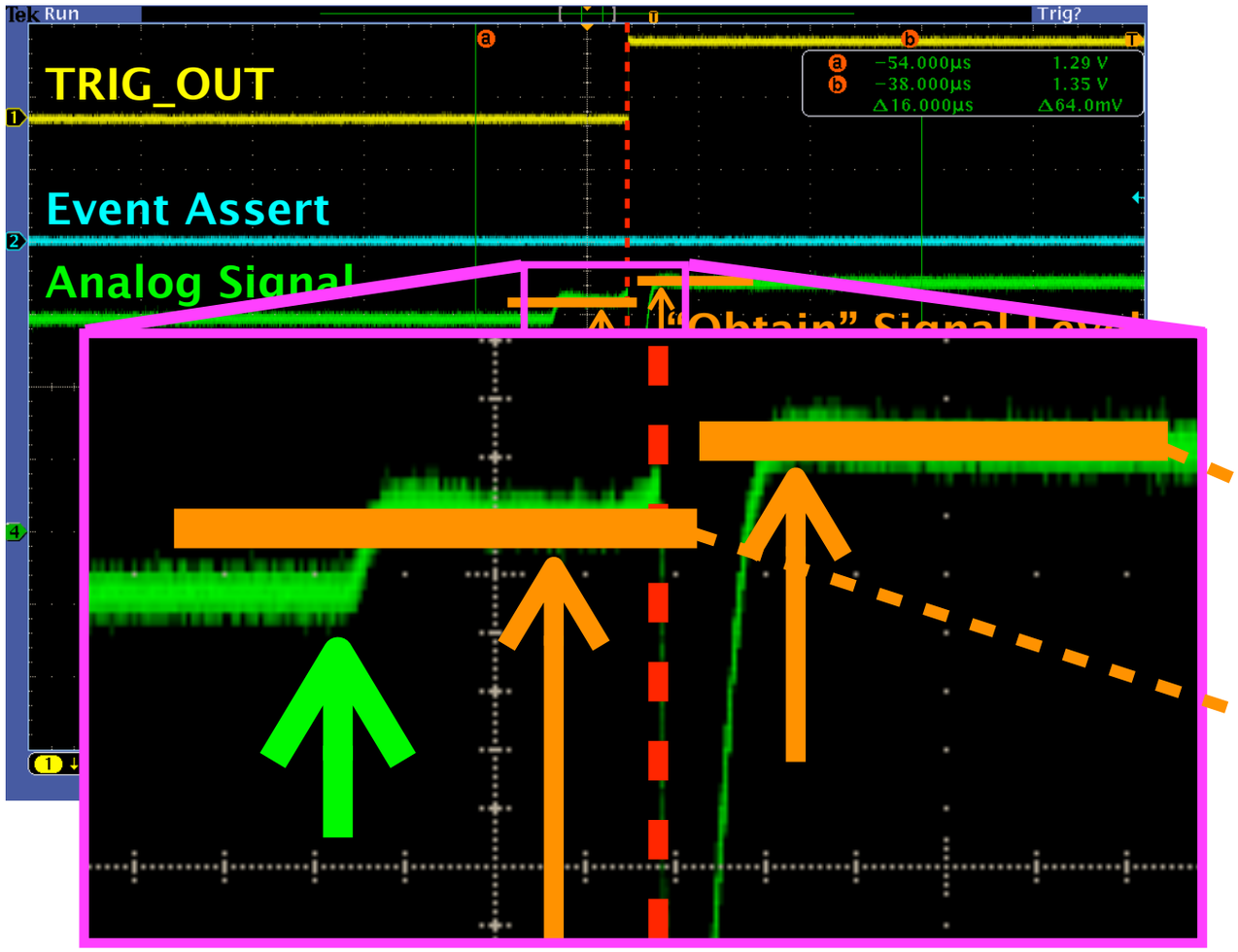
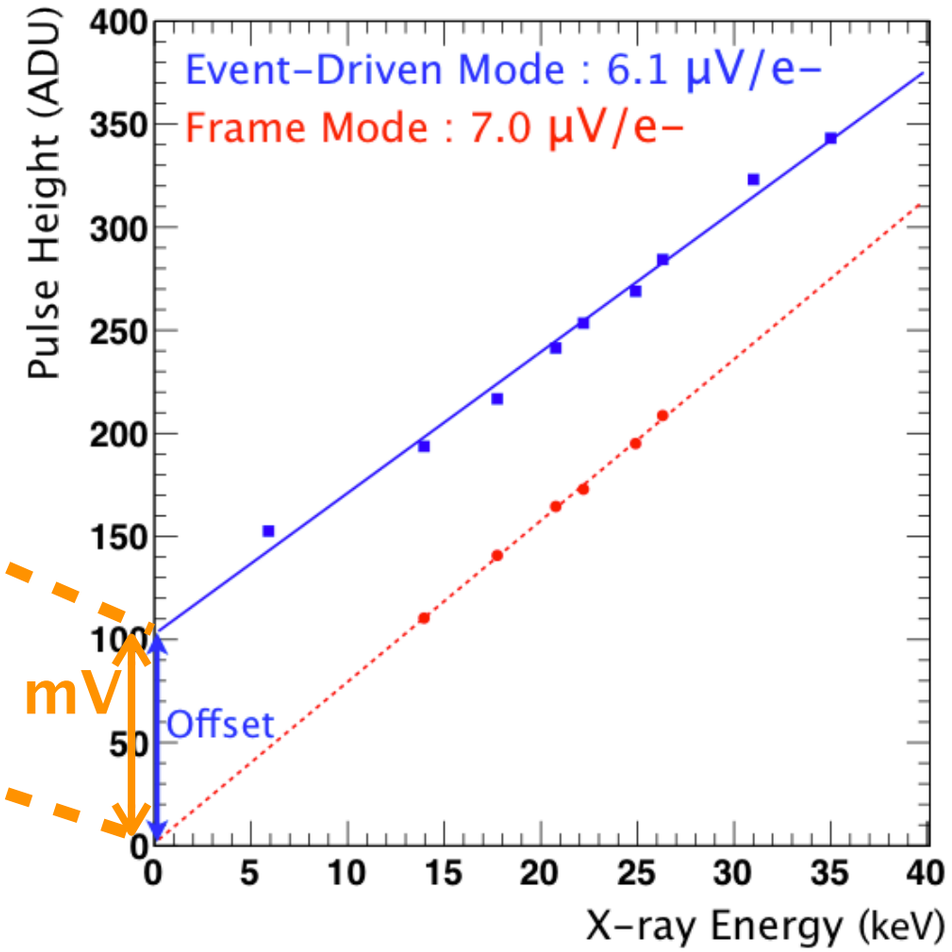


2. About the Difference in a Signal Level

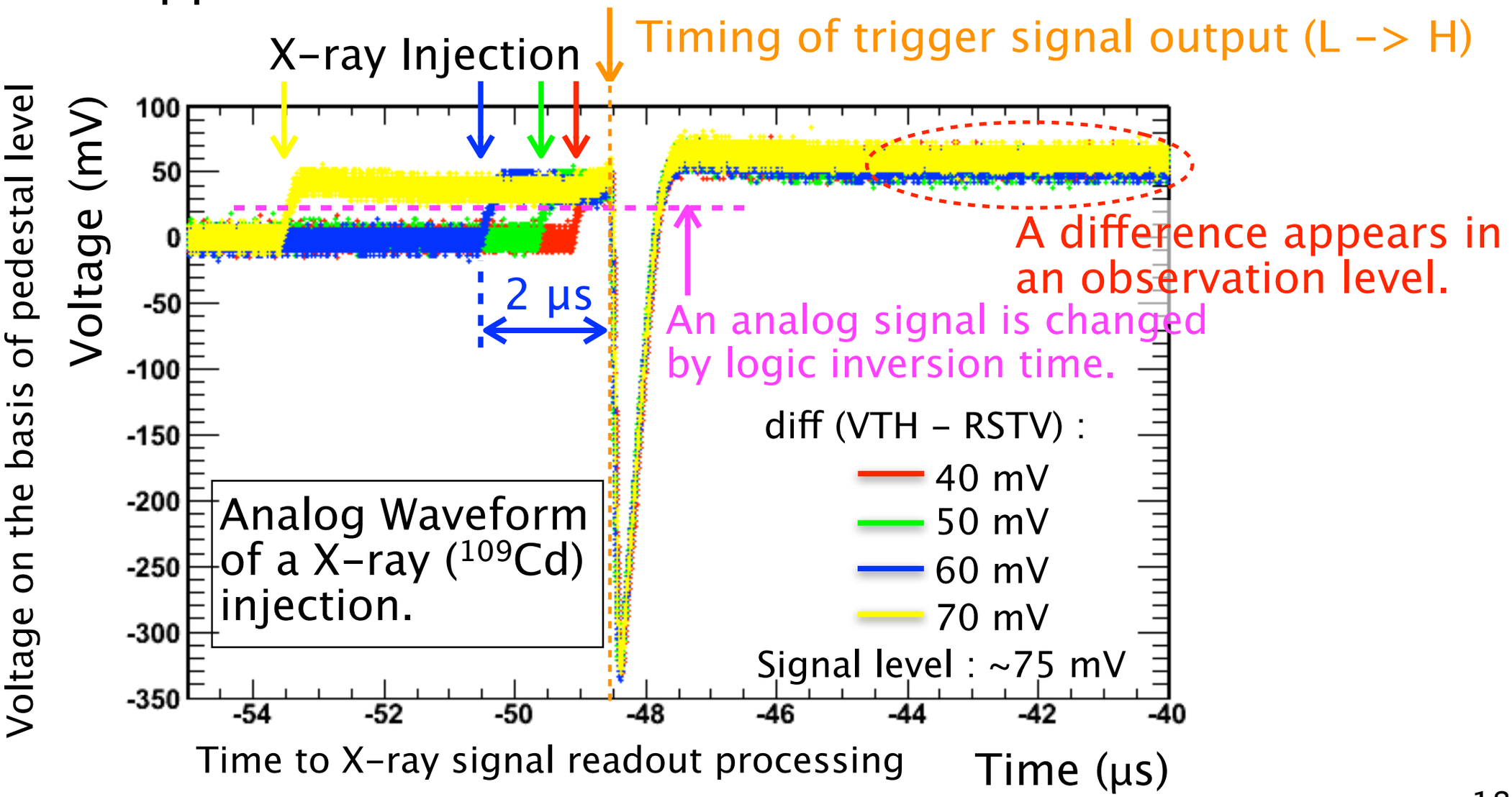
- The reason for a cause is not understand yet.
- However, it is equivalent to offset of a calibration plot (~25 mV).
  -> This is not a serious problem.





3. Long Logic Converting Time
4. Fluctuation of an Analog Signal

- Logic converting time is long (typ : ~50 ns).
- As the difference of a signal and a threshold level is small, logic converting time becomes longer.
  -> This is the characteristic of a comparator circuit.
- A difference appears in an observation level.

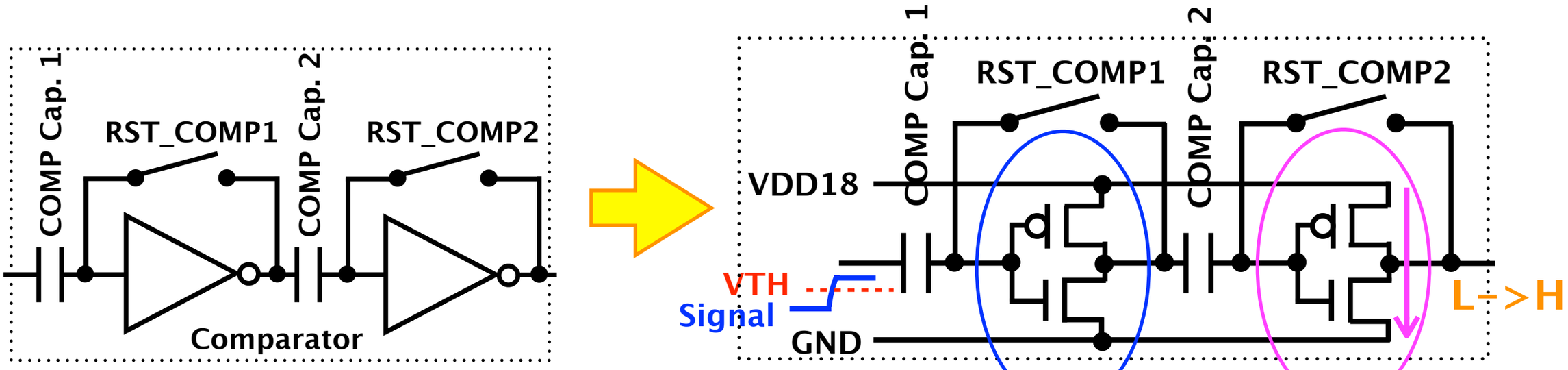


3. Long Logic Converting Time
4. Fluctuation of an Analog Signal

The present comparator circuit ...

-> Inverter chopper type (CMOS Inverter circuit)
(to apply the current to this circuit at the time of logic reversal.)
-> Low power

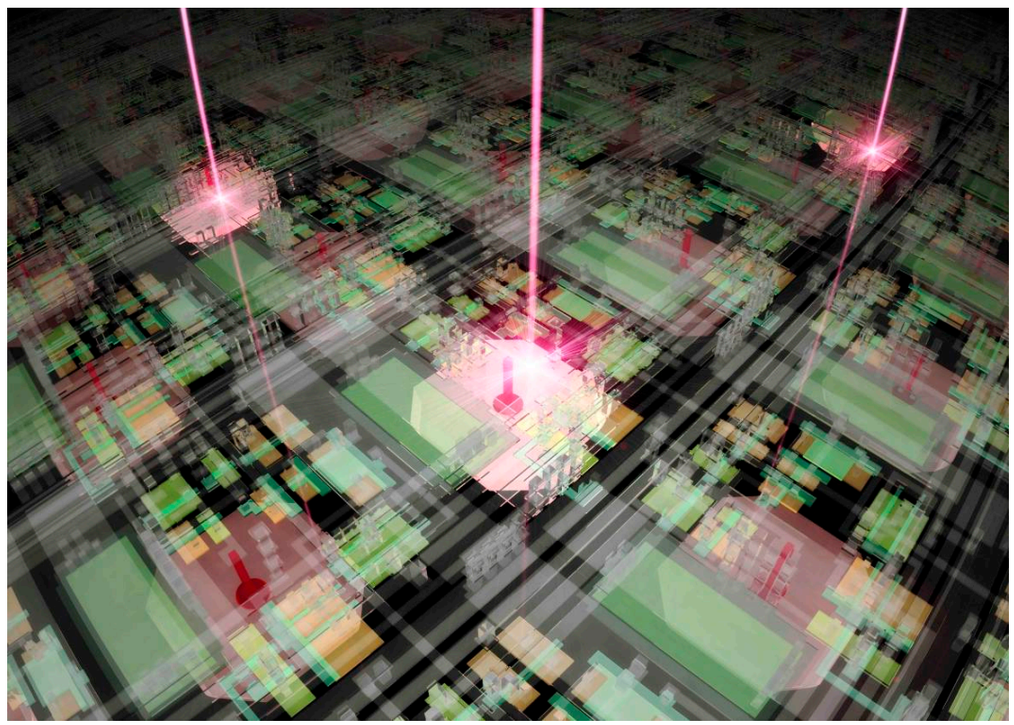
- When a signal and the difference of a threshold level are small, movement of the electric charge of an inverter circuit is small, and time is needed for logic conversion.
- Since the intermediate state of logic flows current most in a CMOS circuit, long logic inversion time affects surrounding analog circuitry.
  -> It has checked also by HSpice simulation.
- Change of a circuit configuration is required.



Summary

- We have been developing Event-Driven SOIPIX sensor, “XRPIX”, for future X-ray astronomical satellite mission.
- Realize the Event-Driven readout mode and very low non-X-ray background by the function of the trigger signal output.
- By CSA pixel circuit, we improved energy resolution successfully.
  -> The readout noise : 33 e- (rms)
  Mn-Kα @ 5.9 keV : 300 eV / 5 % (FWHM)
- We already successfully obtained X-ray data in Event-Driven mode.
  -> However, it has 4 problems.
  -> The comparator circuit modification is required.

Backup



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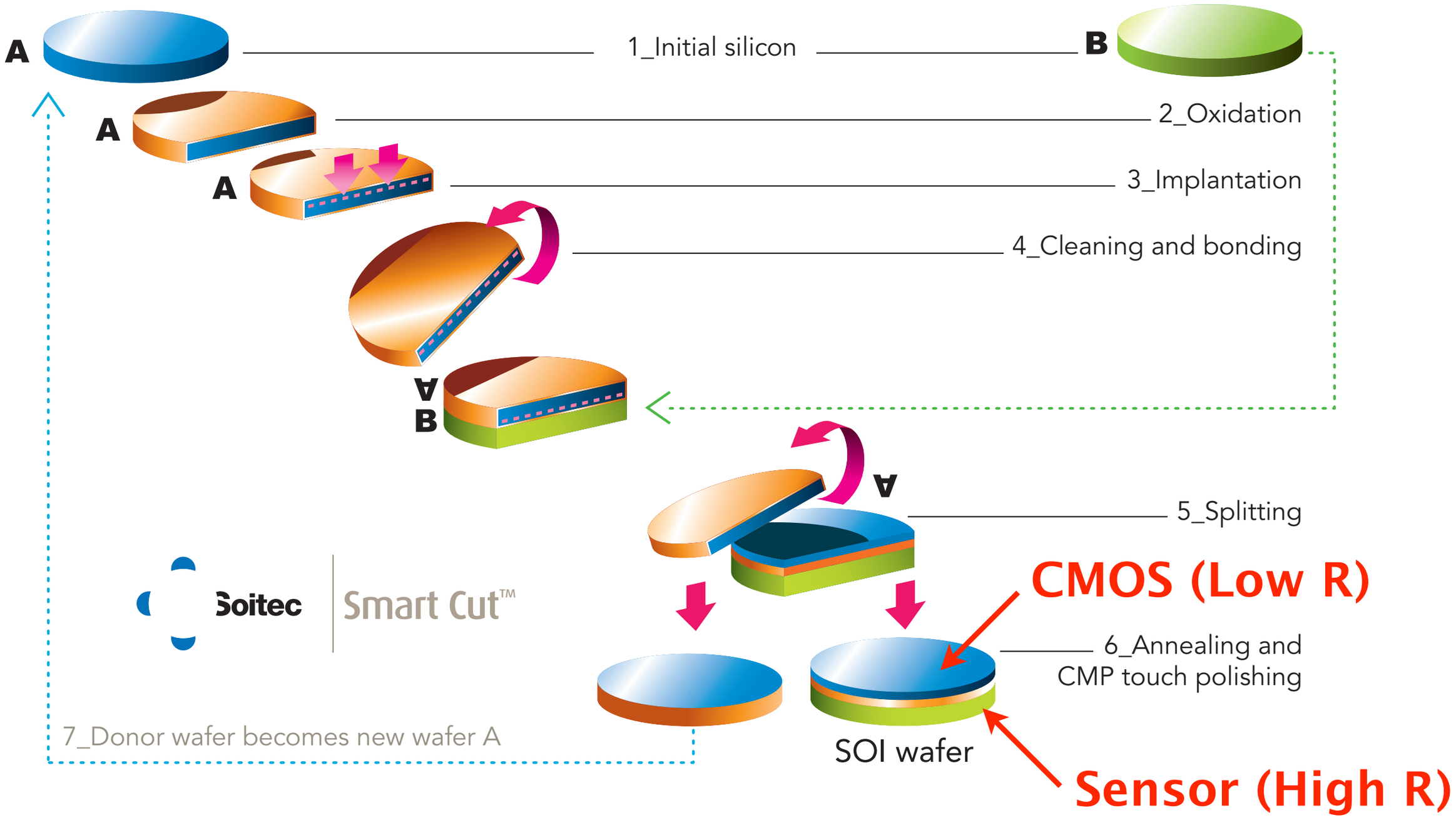
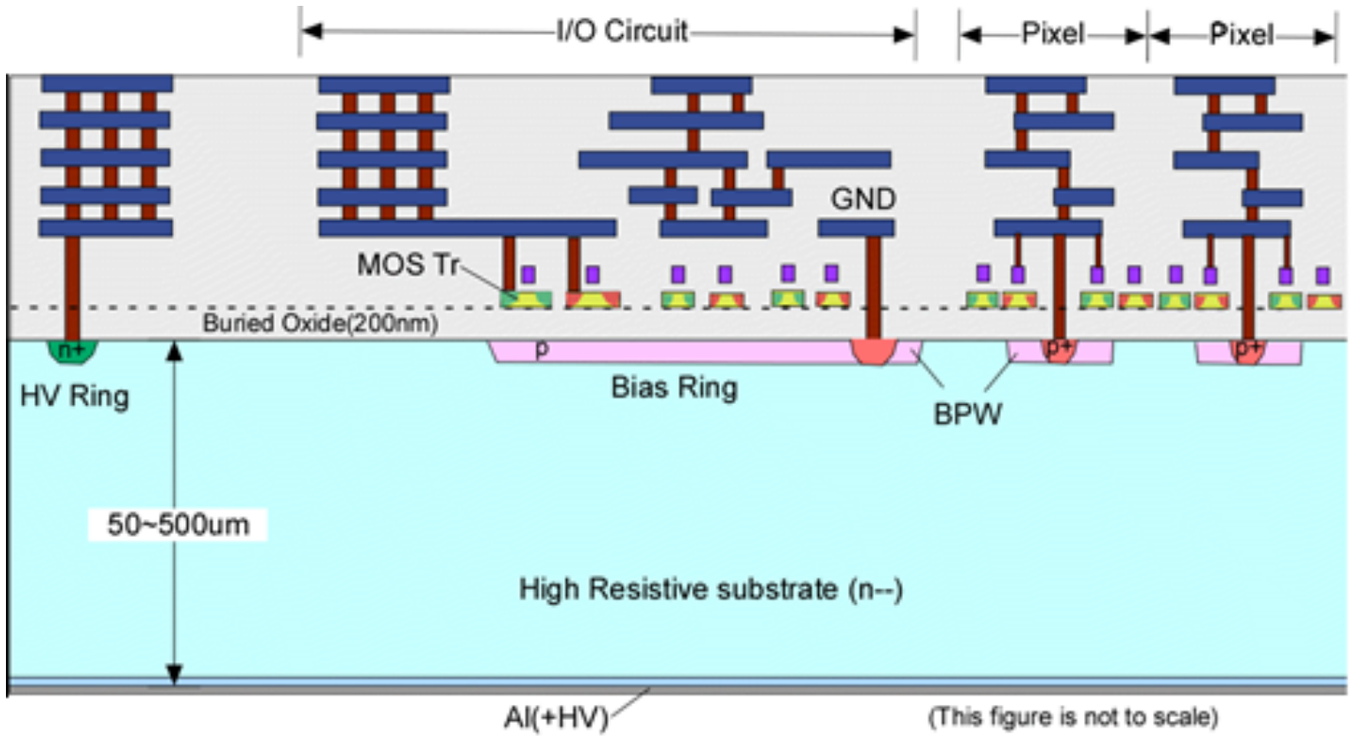

A
1_Initial silicon
B
A
2_Oxidation
A
3_Implantation
4_Cleaning and bonding
A
B
A
5_Splitting
CMOS (Low R)
6_Annealing and
CMP touch polishing
SOI wafer
Sensor (High R)
7_Donor wafer becomes new wafer A
Soitec
Smart Cut™

LAPIS 0.2 μm FD-SOI Pixel Process

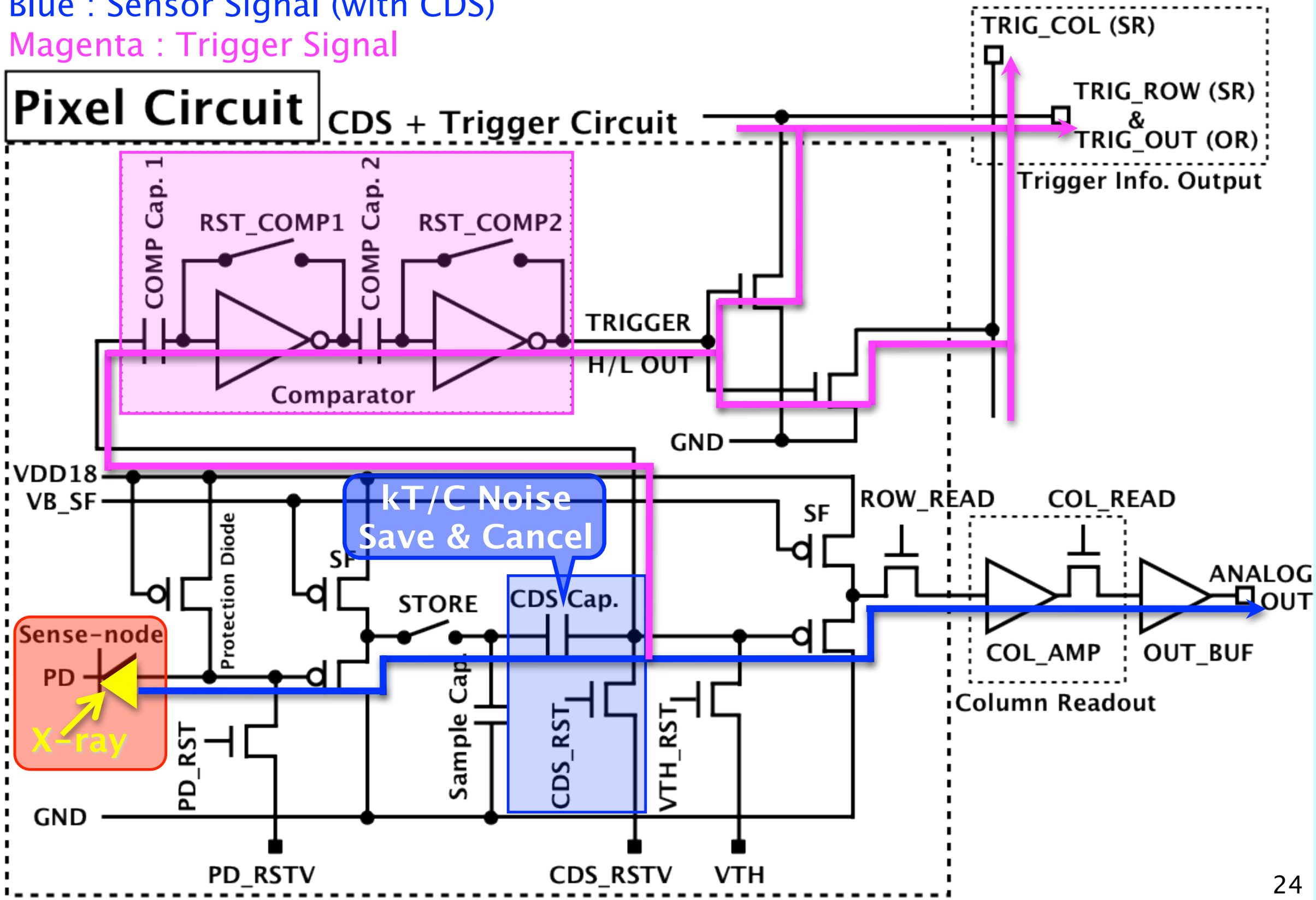
Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (LAPIS) 1 Poly, 5 Metal layers, MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 725 um thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz(n) ~700 Ω-cm, FZ(n) ~7 kΩ-cm, FZ(p) ~40 kΩ-cm
Backside	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating



Design Specification : Pixel Circuit

Blue : Sensor Signal (with CDS)

Magenta : Trigger Signal



Timing Diagram