Contribution ID: **76** Type: **Oral**

Associative Memory computing power and its simulation.

Friday, 6 June 2014 11:40 (20 minutes)

The associative memory (AM) system is a computing device made of hundreds of AM ASICs chips designed to perform "pattern matching"at very high speed. Since each AM chip stores a data base of 130000 pre-calculated patterns and large numbers of chips can be easily assembled together, it is possible to produce huge AM banks. Speed and size of the system are crucial for real-time High Energy Physics applications, such as the ATLAS Fast TracKer (FTK) Processor. Using 80 million channels of the ATLAS tracker, FTK finds tracks within 100 micro seconds.
The simulation of such a parallelized system is an extremely complex task if executed in commercial computers based on normal CPUs. The algorithm performance is limited, due to the lack of parallelism, and in addition the memory requirement is very large. In fact the AM chip uses a content addressable memory (CAM) architecture. Any data inquiry is broadcast to all memory elements simultaneously, thus data retrieval time is independent of the database size. The great computing power is also supported by a very powerful I/O. Each incoming hit reaches all the patterns in the AM system within the same clock cycle (10 ns).
We report on the organization of the simulation into multiple jobs to satisfy the memory constraints and on the optimization performed to reduce the processing time. Finally, we introduce the idea of a new computing unit based on a small number of AM chips that could be plugged inside commercial PCs as coprocessors. This unit would both satisfy the need for very large memory and significantly reduce the simulation time due to the use of the highly parallelized AM chips.

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Session Classification: III.c Embedded Software

Track Classification: Data-processing: 3c) Embedded software