TOWARDS A L1 TRACKING TRIGGER FOR THE ATLAS EXPERIMENT

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INTRODUCTION

Expedited tracking planned for later stages of ATLAS trigger (FTK project@TIPP14: Gentsos, Luciano, Sotiropoulou, Volpi)

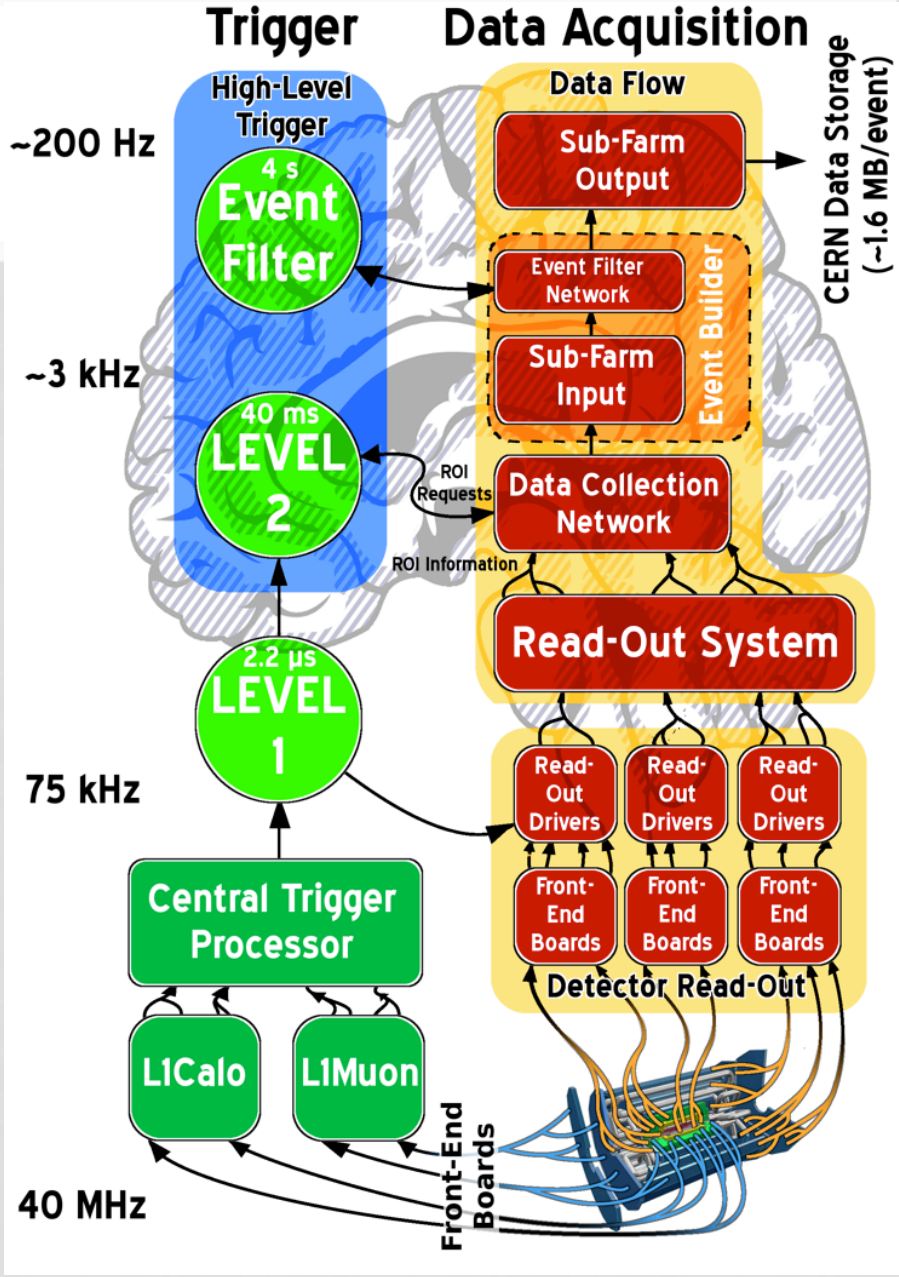
ATLAS intends to complement with a L1 Trigger implementation to improve event selection (LHCC-2012-022)

- Context
  - LHC & ATLAS Upgrades
  - Why tracking in the ATLAS Trigger system?
- Performance
- Architecture Proposals
  - Detector read-out
  - Track finding and Pattern Matching

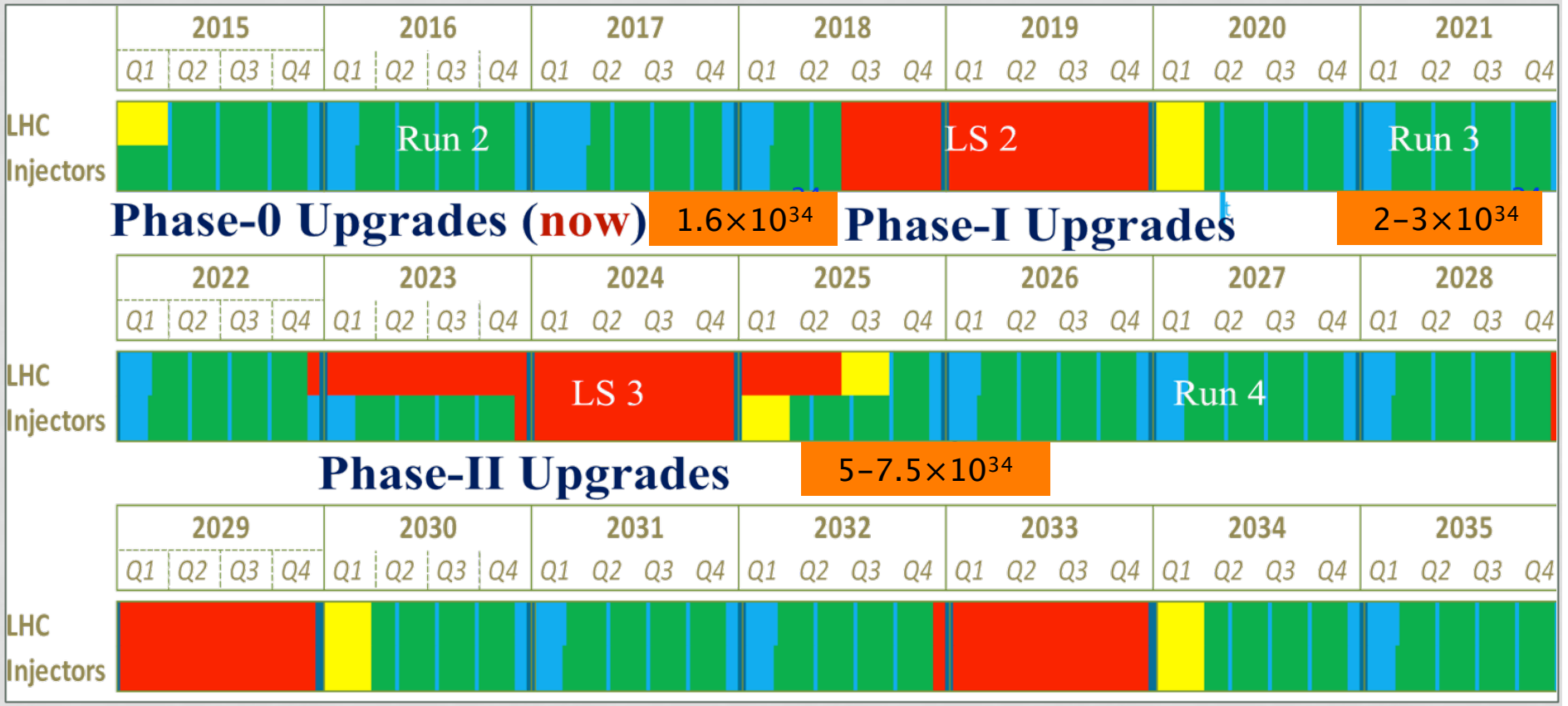
THE ATLAS RUN I TRIGGER

3-tier system

- Level-1 → HW implementation
- L2+L3 commercial CPU
- L1→HLT via Regions of Interest



LHC FUTURE



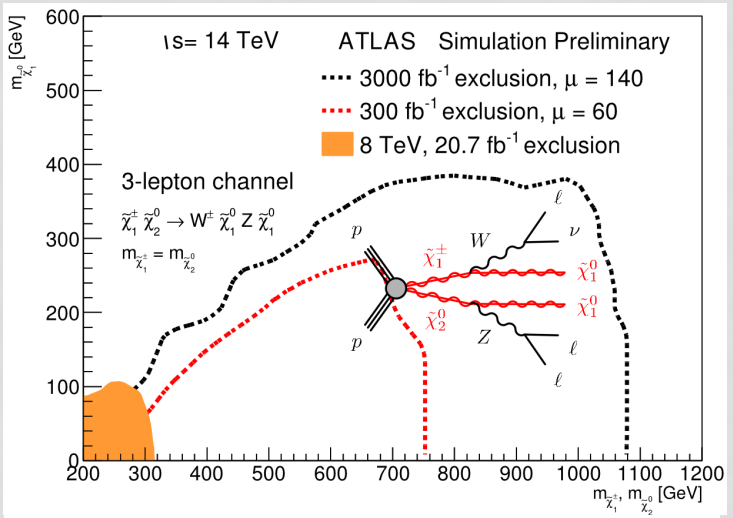
HL-LHC: Major upgrades for LHC+detectors

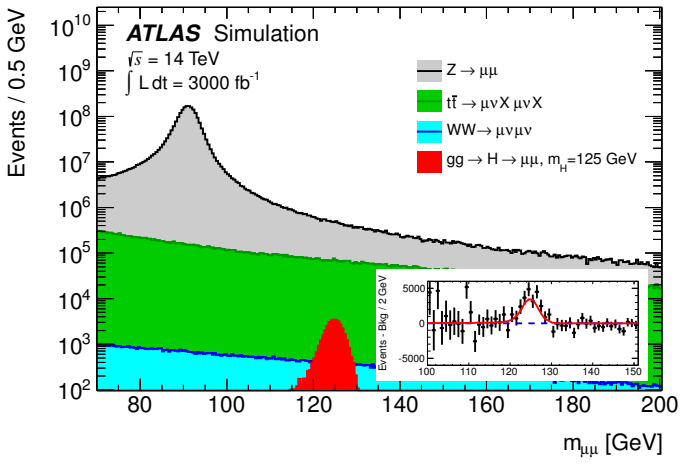
New project ⇒ significant R&D ongoing

WHAT PHYSICS @ 5×10^{34}?

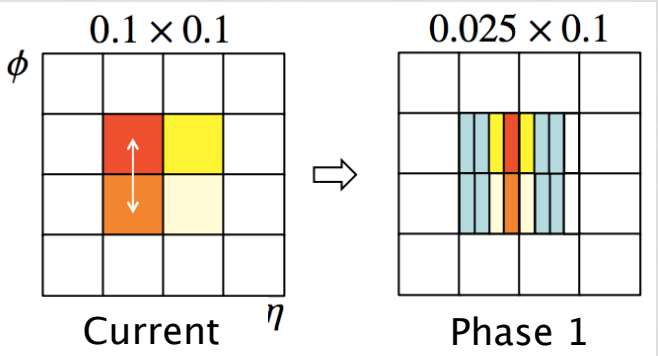
- Goal: $\int \mathscr{L}\sim 3$ ab^{-1} i.e. 300 fb^{-1}/yr
- Access to large SUSY phase space (ATL-PHYS-PUB-2013-011):
  - Direct χ ($\pm$ and 0) production → 3ℓ (gauge boson mediated)
- 7σ H→$\mu\mu$ with S/B~3×10^{-3}

Challenging conditions:
<μ>~140





PHASE I TRIGGER UPGRADES (2019)

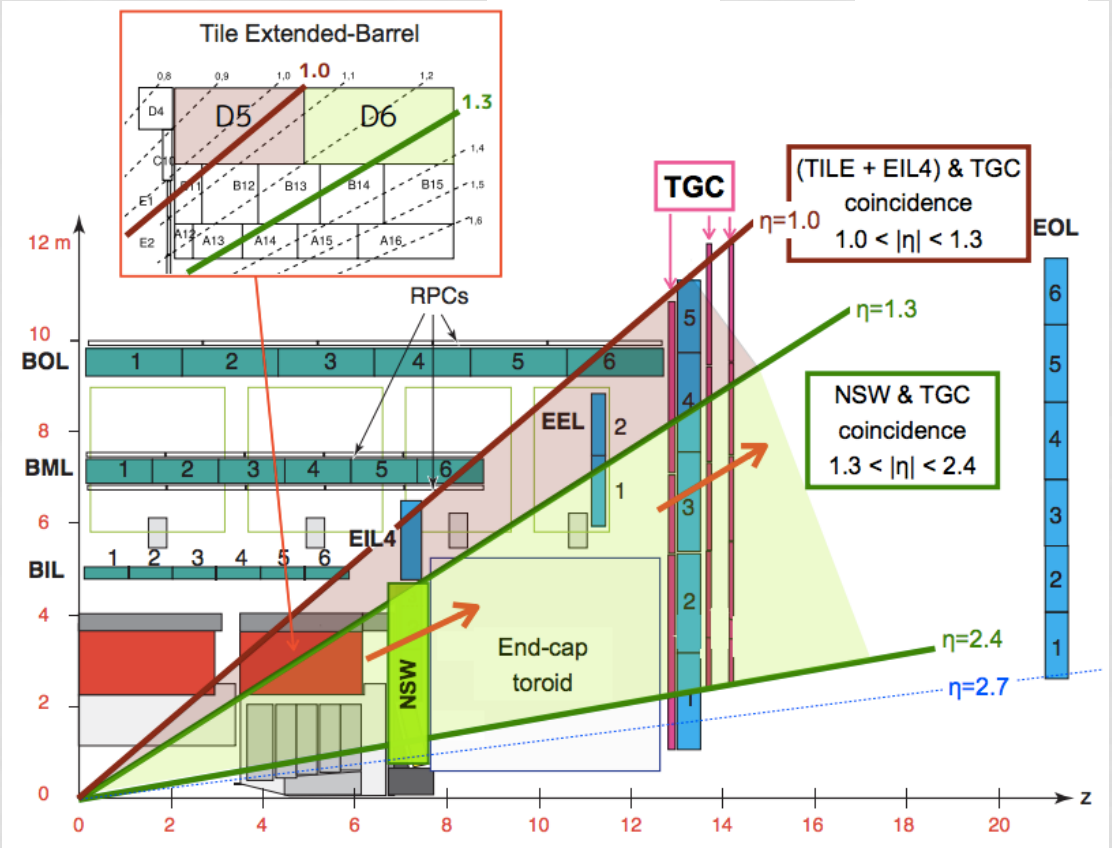


Phase 0:

- L2+EF → HLT
- FTK: global tracking for HLT (installation completed with phase I)
- Topological capabilities at L1
- Improved pile-up suppression In L1Calo

Phase I:

- Refine L1Calo granularity (see I. Hristova's talk)
- New muon small wheel (NSW)

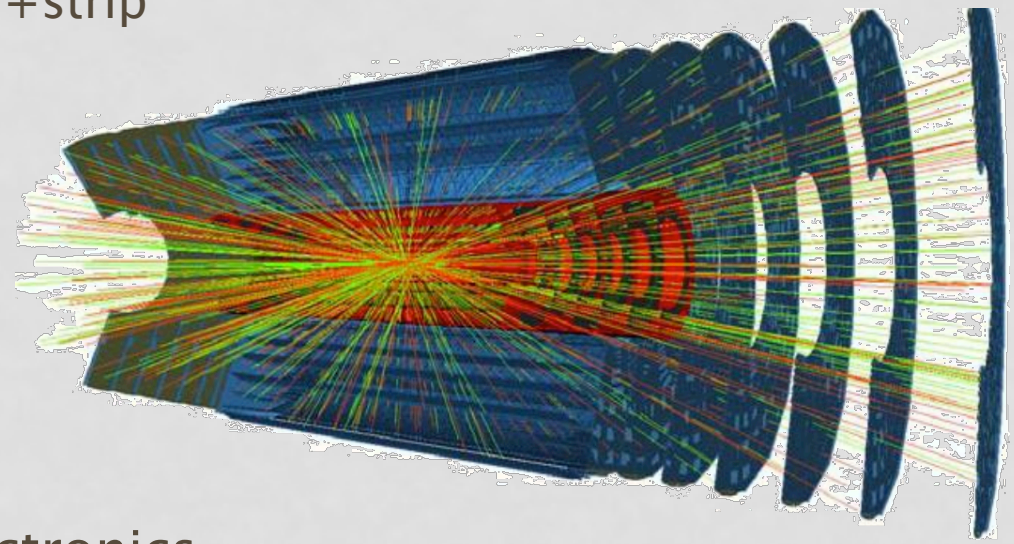


Reduced fakes, improved resolution

ATLAS FOR HL-LHC (2023)

- Software and Computing
- Detector:
  - Brand-new Si detector
    - Inner tracker (ITK): pixel+strip
  - LAr calo electronics
  - Muon drift chamber
  - Forward detector
  - Shielding
- Trigger:
  - L1 Track Trigger (L1TT)
  - μ barrel & big wheel electronics

<μ>~140 @ 25ns x-rate
⇒ 2-3×10^{16} 1 MeV $neutron_{eq}/cm^2$



INNER DETECTOR

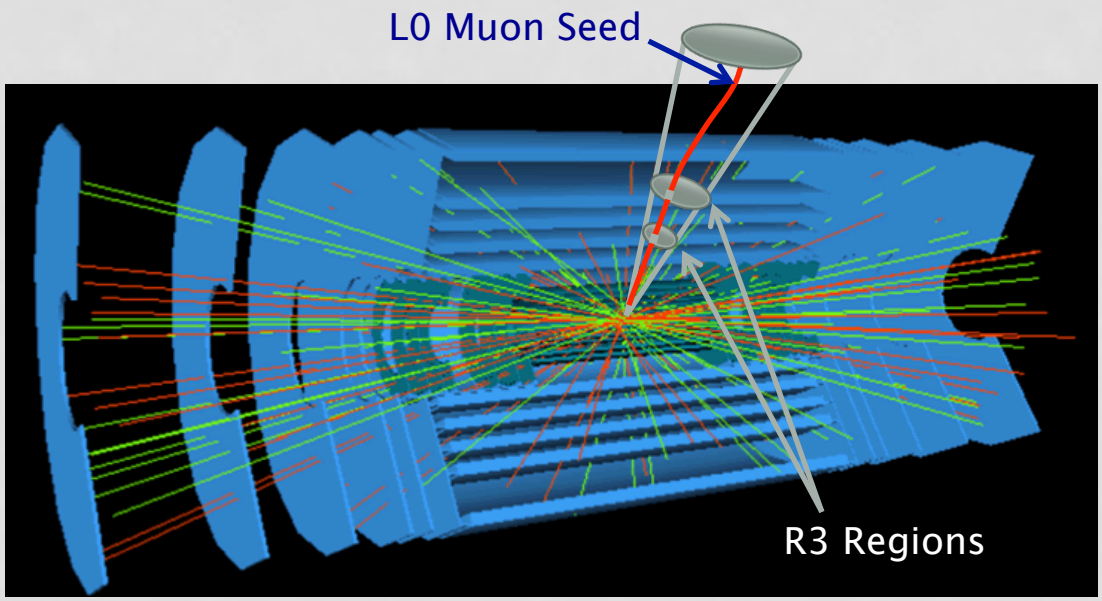
- Facing x5 fluence
- Higher η coverage
- Lighter
- Up to 14 hits/track

Pixels

- 80 → 638 Mchan.
- 50×400→ 25×150/50×250 μm^2
- 1MHz Readout

Double-sided strips

- 6 → 74 Mchan.
- 2.45-4.9 cm
- 74.5 μm pitch
- 40 μrad st. angle
- Slower read-out (chip size & placement)



- RoI concept moved to new L0 (pre-L1) :

  500 KHz → 200 KHz

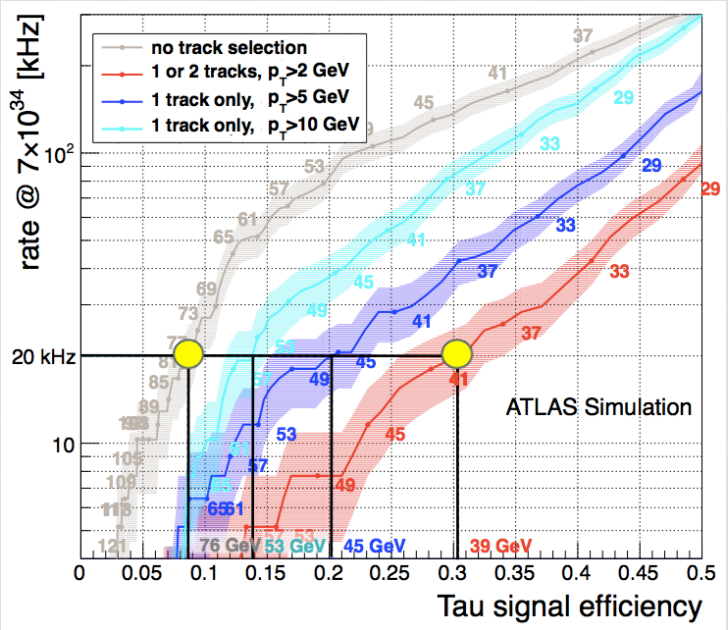
- Full readout after L1 decision

L1 TRACK TRIGGER

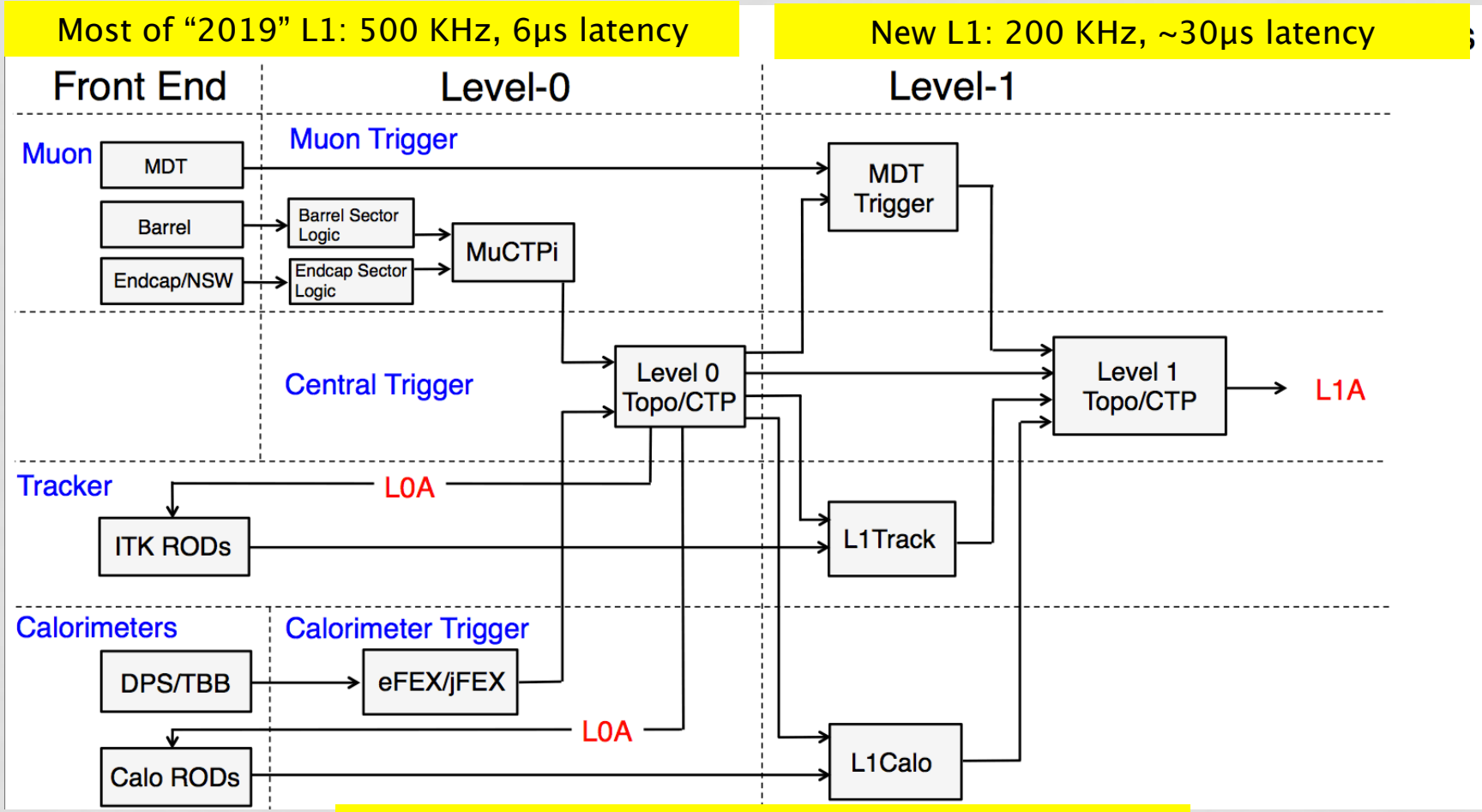
Object(s)	Trigger	Estimated Rate	
		no L1Track	with L1Track
e	EM20	200 kHz	40 kHz
γ	EM40	20 kHz	10 kHz*
μ	MU20	$>$ 40 kHz	10 kHz
τ	TAU50	50 kHz	20 kHz
ee	2EM10	40 kHz	$<$ 1 kHz
$\gamma\gamma$	2EM10	as above	$\sim$5 kHz*
$e\mu$	EM10_MU6	30 kHz	$<$ 1 kHz
$\mu\mu$	2MU10	4 kHz	$<$ 1 kHz
$\tau\tau$	2TAU15I	40 kHz	2 kHz
Other	JET + MET	$\sim$ 100 kHz	$\sim$ 100 kHz
Total		$\sim$ 500 kHz	$\sim$ 200 kHz

$\mathscr{L}=5\times10^{34}$, based on L0 RoI information

- Track association ⇒ improve μ, τ and EM selection:
  - ×10 rate reduction on EM_18
  - 8% → 30% (E_T>20 GeV) τ efficiency with 20 KHz budget



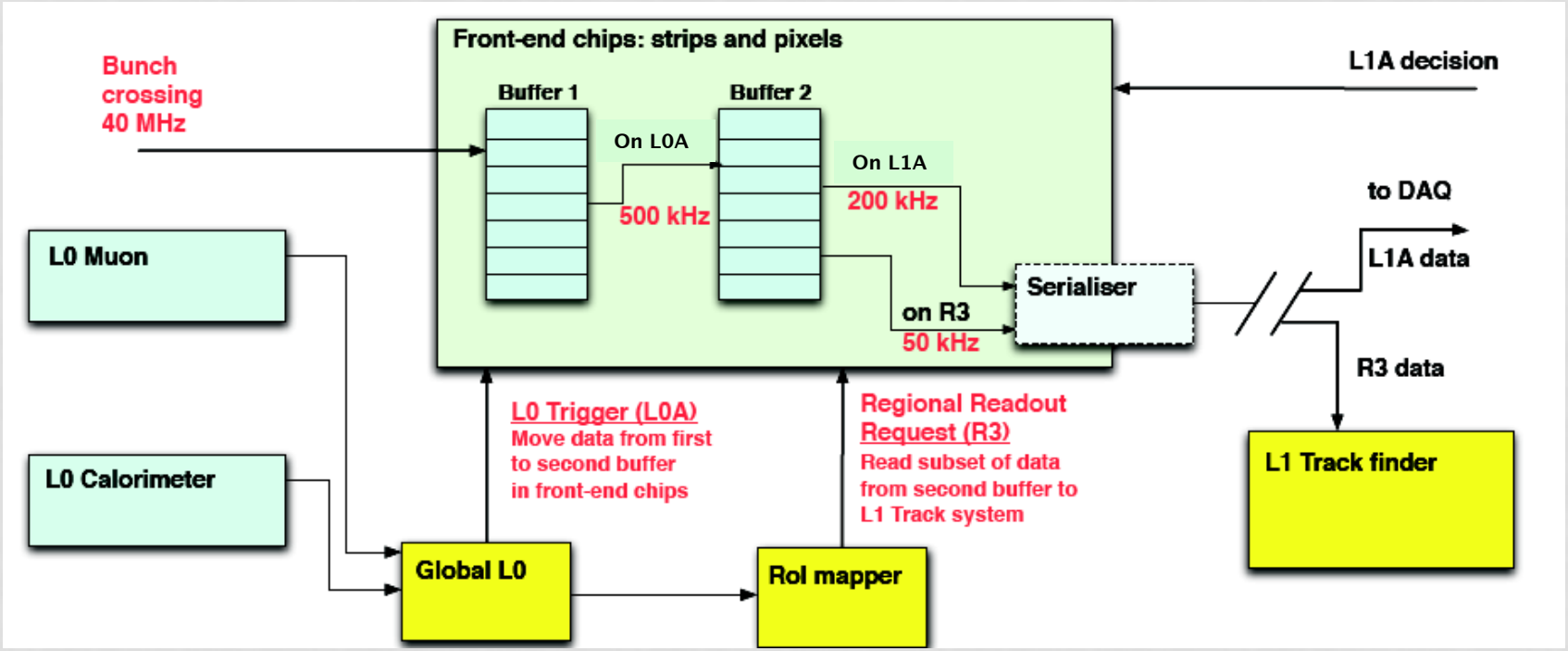
ATLAS HL-LHC TRIGGER ARCHITECTURE



STRIP TRACKER READOUT

New trigger level ⇒ new readout buffer layer

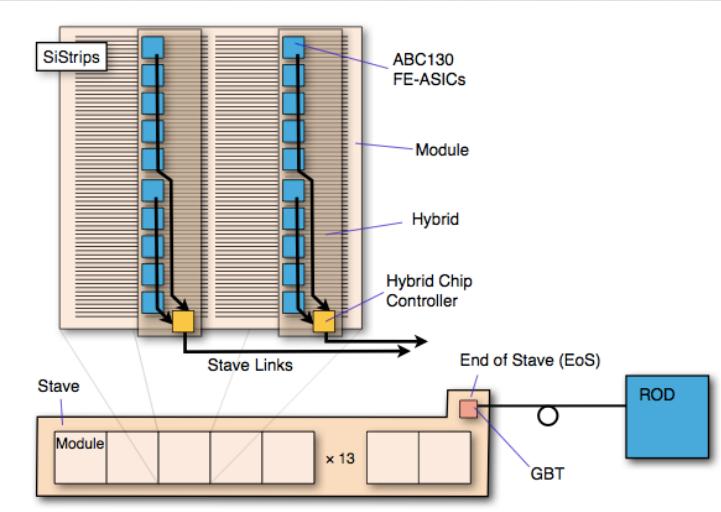
Implemented in Q4/2013 “ABC130” tracker FE ASIC

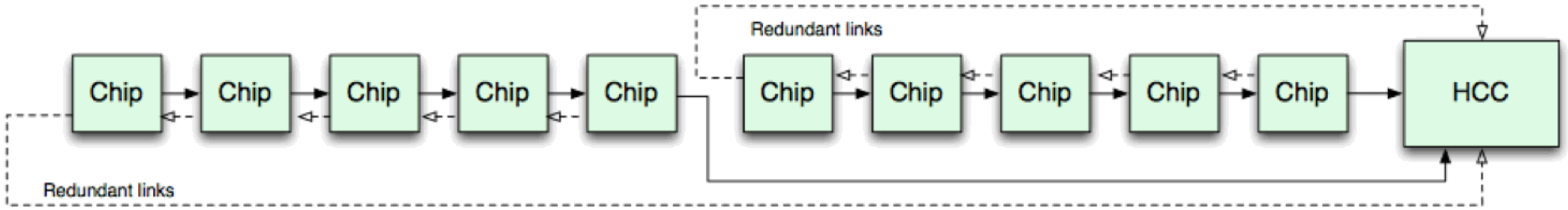


L0: 10% R3 → 50 kHz, L1: 200 kHz

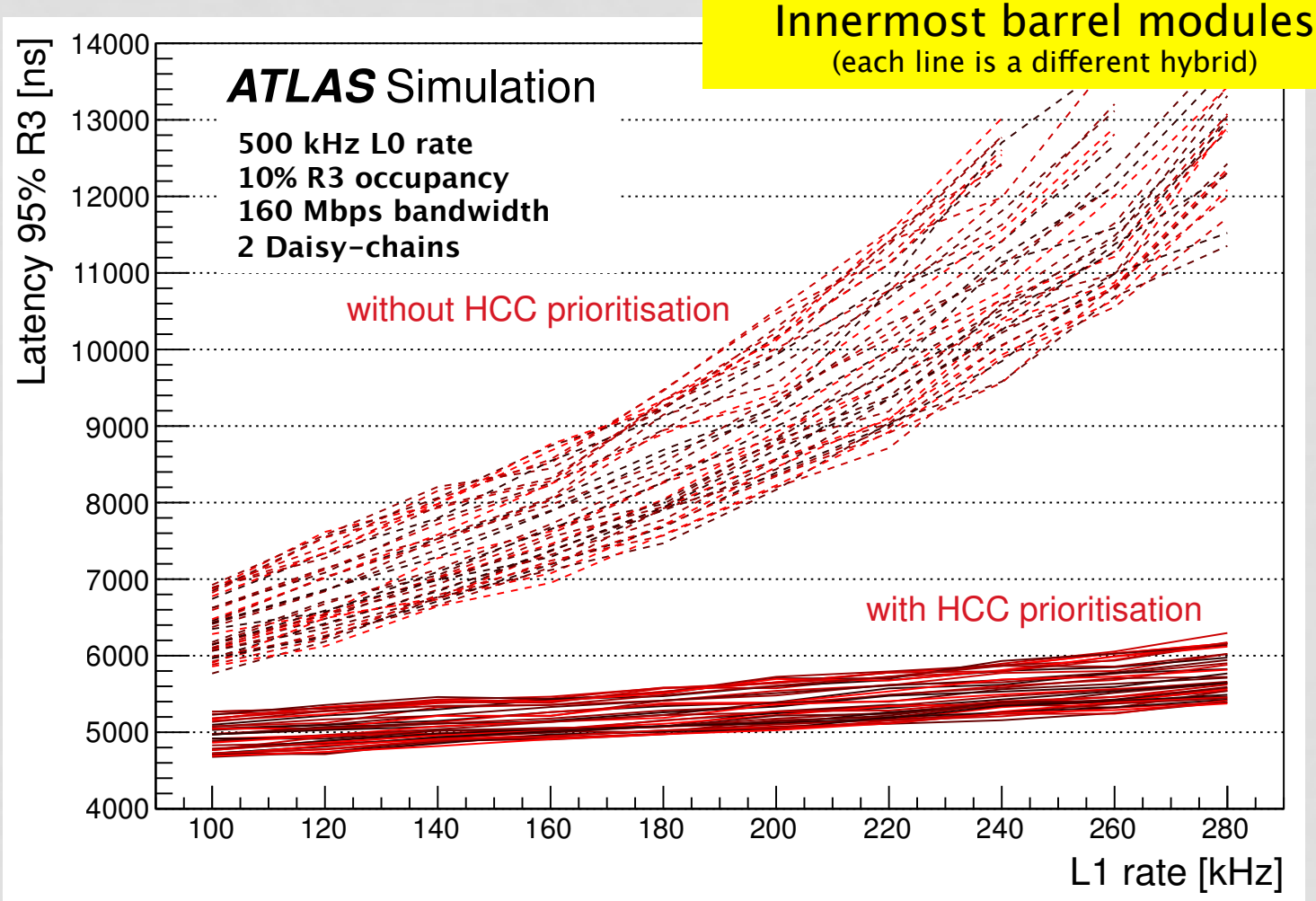
READOUT LATENCY

- Multiple ABC130 daisy-chained
- Bottleneck addressed by:
  - Prioritization of R3 vs L1A data
  - Increase HybridChipController BW
    (160 → 320 Mbps)
  - Increase FIFO depth
  - Increase daisy-chain links

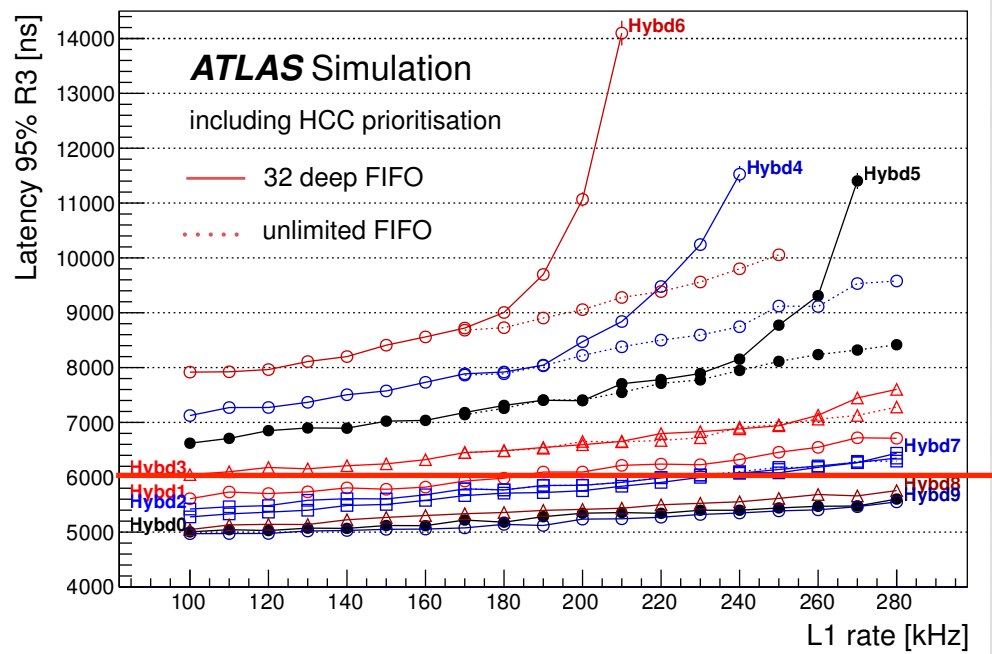


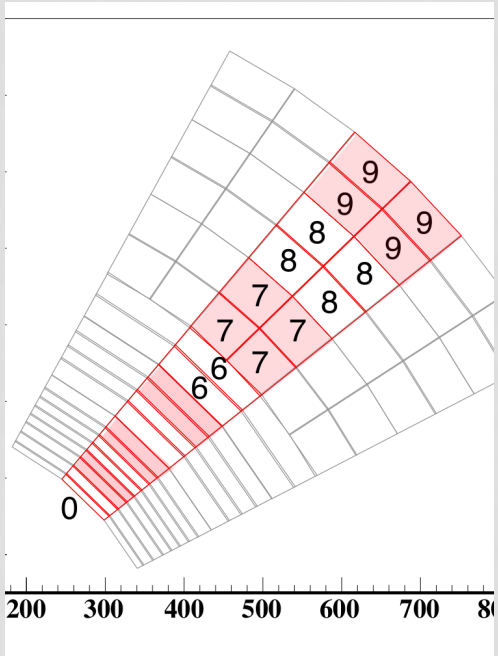


READOUT LATENCY



LATENCY BY GEOGRAPHY



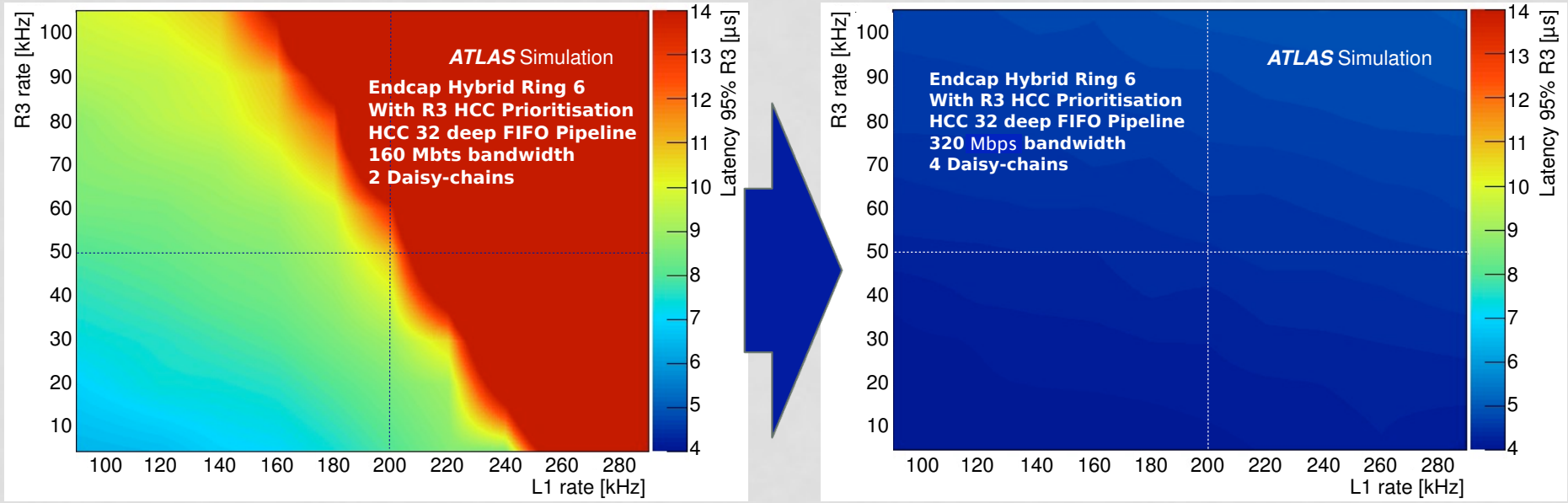


Longer daisy-chains (up to 12) in EC detectors
prioritisation is not enough!

END-CAP RING 6

Exploit:

1. Redundant daisy-chain link
2. Increase in off-detector bandwidth



Problem solved with optimised use of existing resources

FINDING TRACKS: FTK STYLE

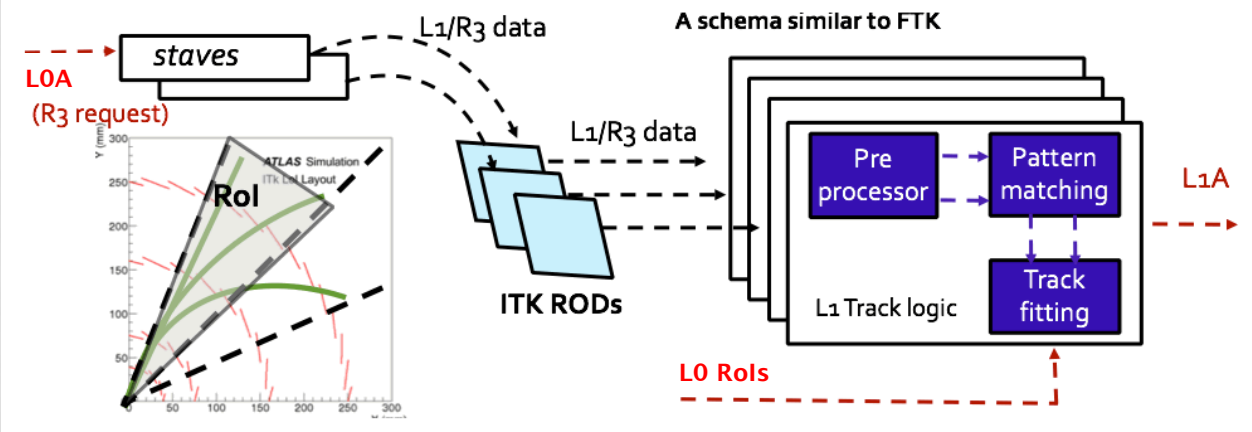
- L1TT input B/W:
  - Limit with fine η×ϕ segmentation:

    p_T>4 GeV

    ↕

    0.05×0.05

    (126000 towers)



- How many patterns?

$$N_{\text{Pattern}} \propto N_{\text{Pileup}} \cdot \frac{1}{p_T} \cdot N_{\text{Layer}}$$

  - Current FTK design based on 8000 AMChip6 ⇒ 10^9 patterns (higher capacity AMChip evolutions possible →Gentsos presentation)
  - FTK → L1TT:
    - Same detector
    - x2-3 pile-up increase
    - 8/12 → 12/14 layers

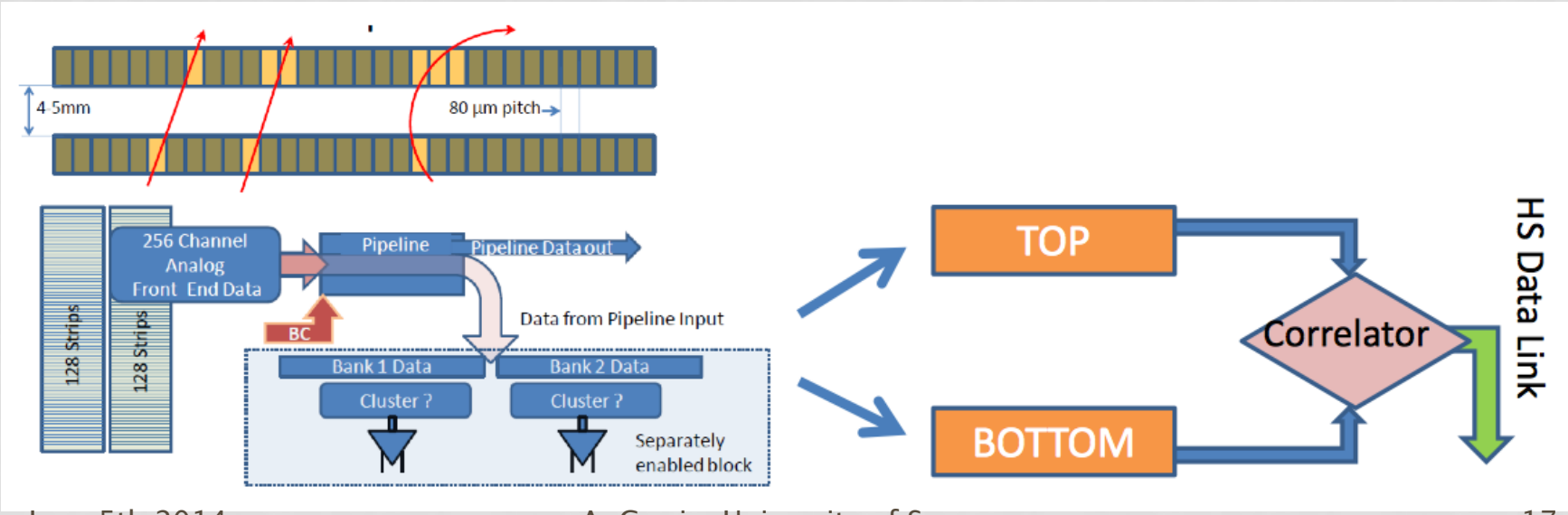
Possible with mitigation from RoI-based concept? Increase pT threshold?

ALTERNATIVE APPROACH

RoI-less hierarchical approach:

- Limit off-detector data flow:
  - On-detector "stub" finding based on double-sided detectors
  - Match 2-3 "stubs" for further pT discrimination
  - Fast cluster-finding in pixel detector
- Compatible 4 Gb/s readout rate per detector stave

- Variation (sketch below): detector layer doublets at 4-5 mm distance



CONCLUSIONS

- Tracking at L1
  - x3-x10 rejection improvement
- 6/30 μs L0/L1 latency splitting possible with proposed double buffering scheme
  - 1-10% of detector R3
  - 500 kHz L0 and 200 kHz L1 rates
- Additional flexibility in the ATLAS TDAQ pipeline

Next steps:

2015: full specifications for L1TT

2016: Inner TracKer TDR

BACK-UP MATERIAL

L0/L1 LATENCIES

	Latency (μs)
From L0A	6
RoI Mapping → ITK	1.25
Region readout from ITK	6
Transmission to L1TT	2
Tracking in L1TT	6
Merge L1 triggers from L1A	1
Distribute L1A	1
Total	23.25

- Optimal use of MDT buffers → 30 μs latency
- L1Track budget:
  - R3: Regional Readout Requests data extraction
  - Data processing

  Depends (non-linearly) on:
    - L0 rate
    - #RoI
    - Available readout BW