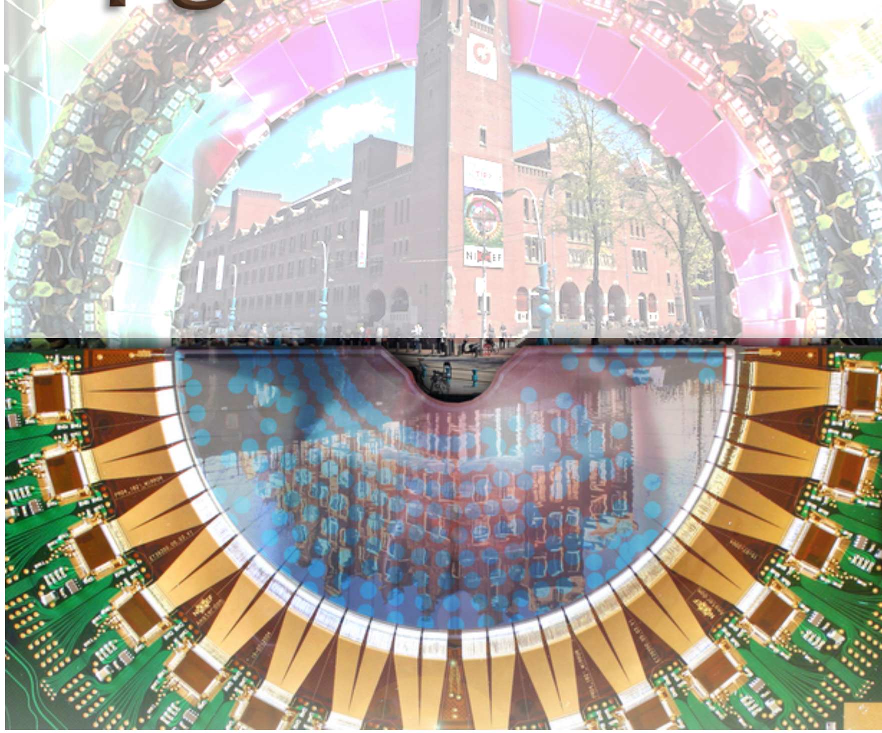
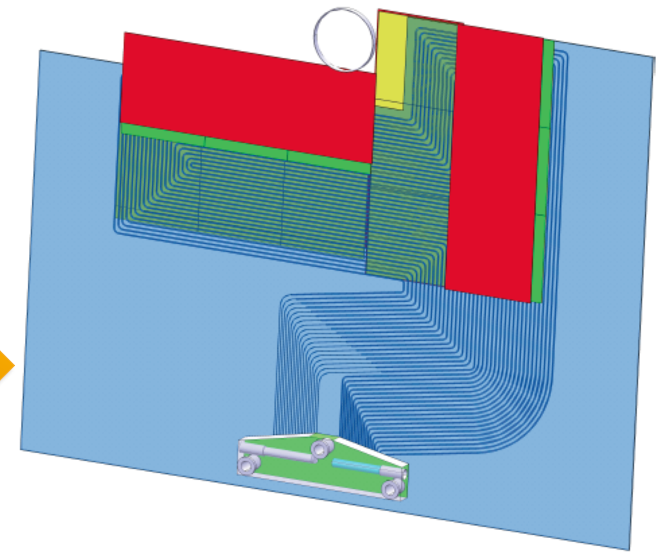
Upgrade of the LHCb VErtex LOcator





Kazu Akiba – Federal University of Rio de Janeiro
On behalf of the VELO Upgrade Project

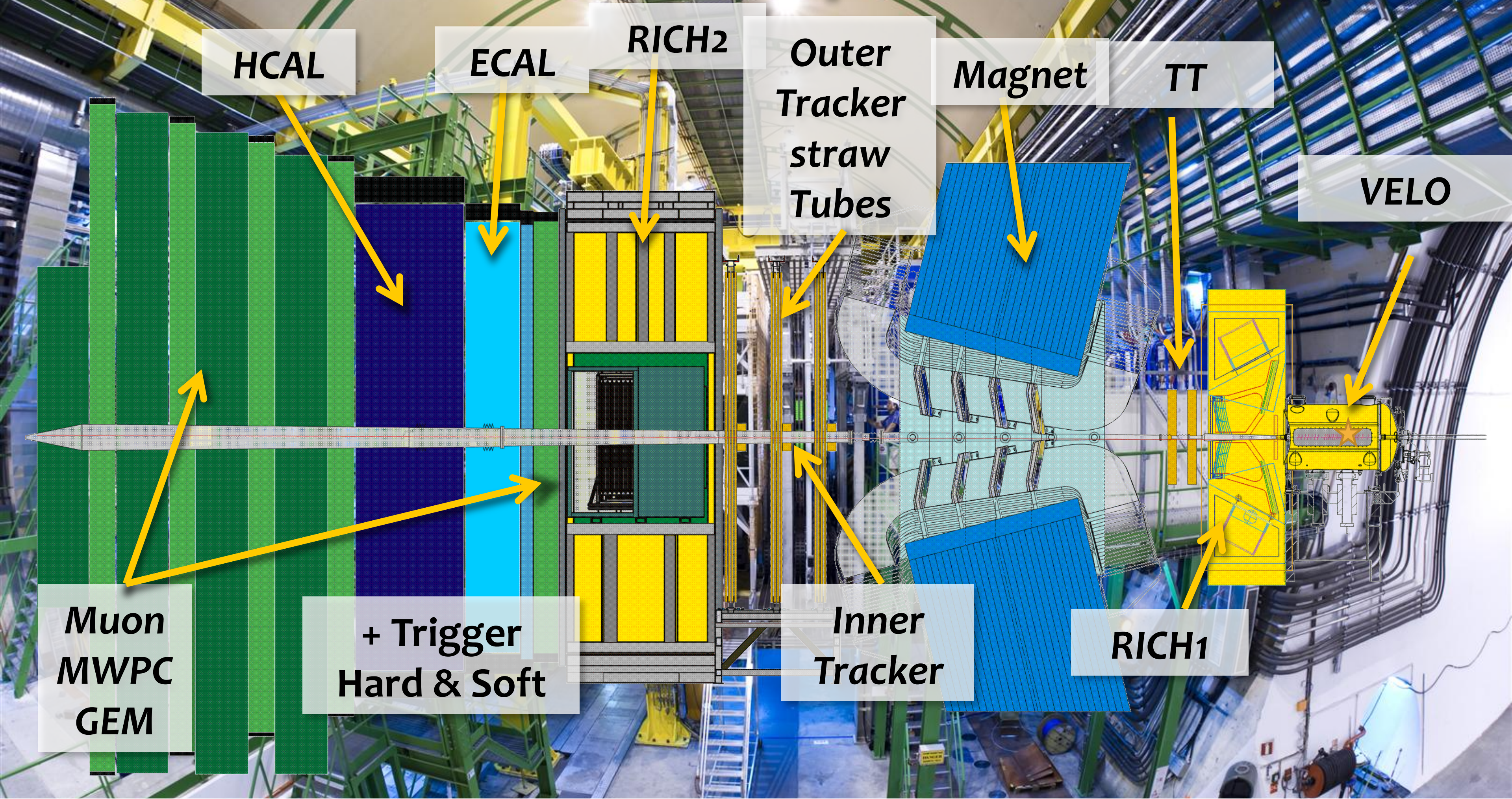
TIPP '14

International Conference on Technology and Instrumentation in Particle Physics

2 – 6 June 2014 / Amsterdam, The Netherlands

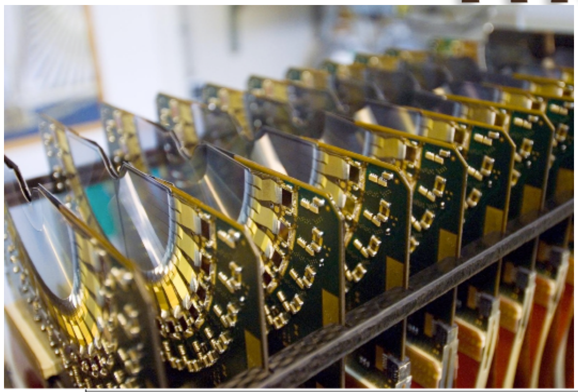
"Instrumentation as enabler of Science"

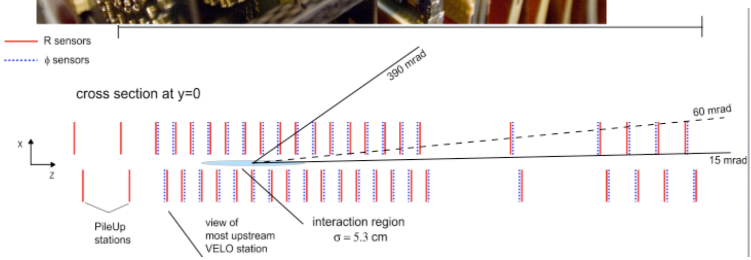
The LHCb Experiment

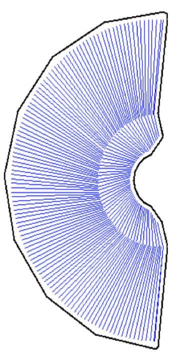


Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

The current VELO







88 silicon sensors

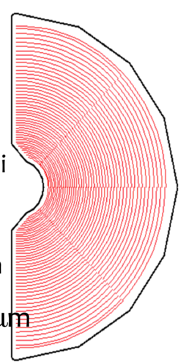
R-ϕ design

300 μm, n^+n Si

2048 strips

r_{active} = 8.2mm

$pitch_{min}$ = 40 μm



Moves away every fill and **centers around the beam** with self measured vertices

Poster:
The LHCb Vertex Locator
- Performance and Radiation Damage
https://indico.cern.ch/event/192695/contribution/7

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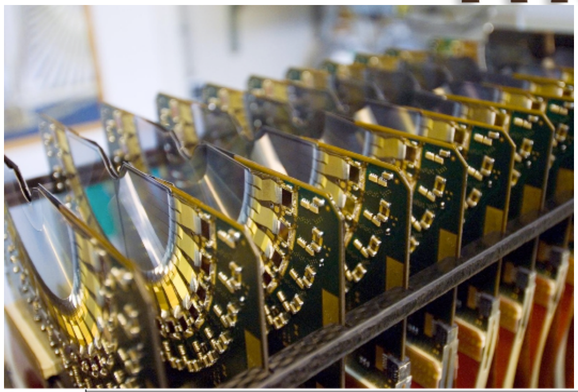

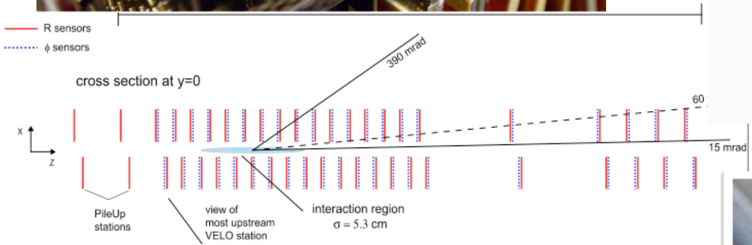

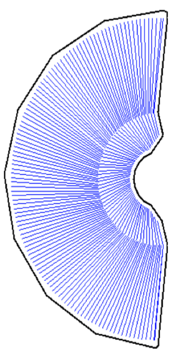

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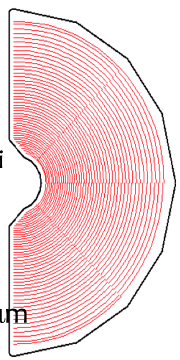

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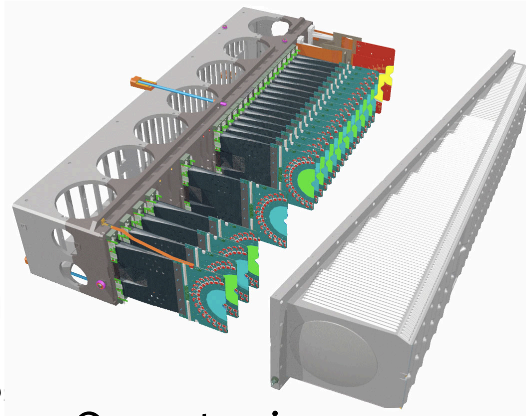
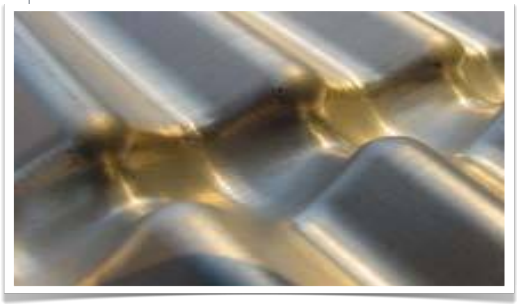


Operates in vacuum



Separated from primary vacuum by thin RF foil with complex shape
-- Protection from beam pickup

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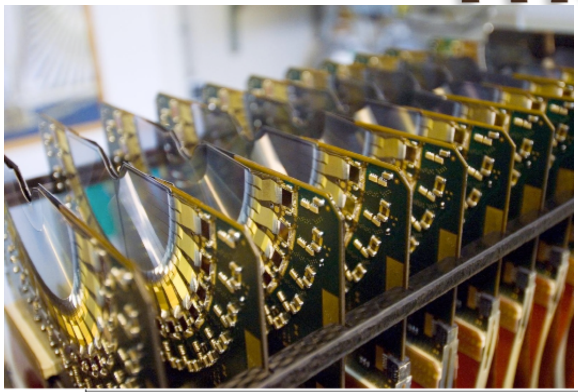

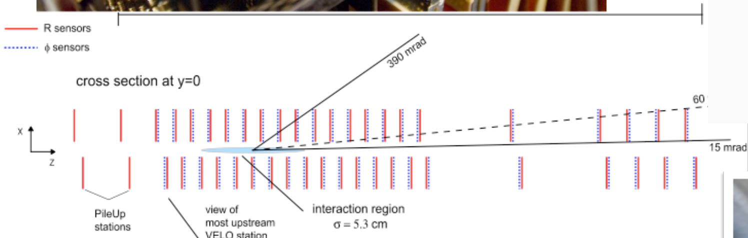

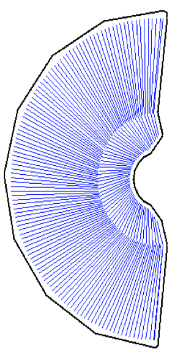

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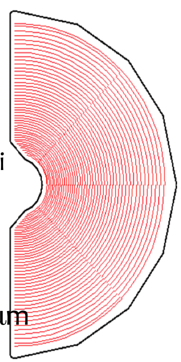

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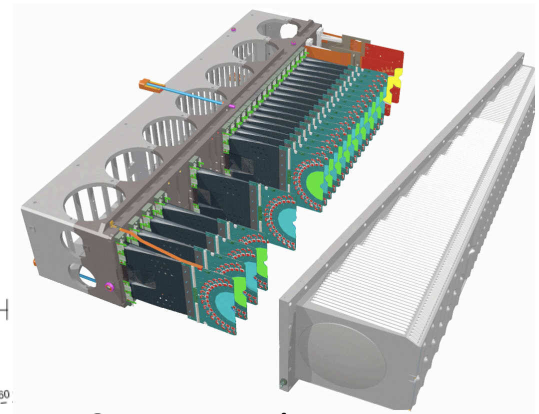

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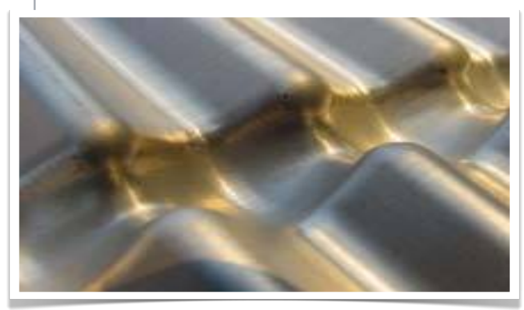


Separated from primary vacuum by thin RF foil with complex shape
-- Protection from beam pickup

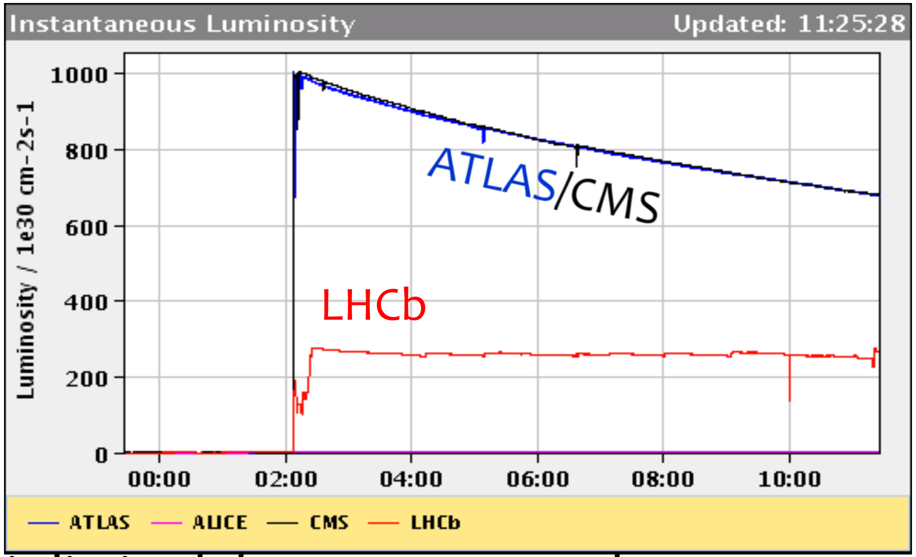
Active cooling

CO_2

Poster:
The LHCb Vertex Locator
- Performance and Radiation Damage
https://indico.cern.ch/event/192695/contribution/7

Why upgrade LHCb

- Currently LHCb can cope with a inst. lumi. higher than design
  - LHC still provides more than what we can handle:



  - Current detector is limited due to 1 MHz readout.
  - Higher Luminosities do not translate to higher physics: need smart Trigger.
- The upgrade is planned as a major Trigger/Readout upgrade:
  - From 1 to 40 MHz full readout ➔ Every collision read out to a computing farm
  - Higher instantaneous Luminosity ➔ Higher occupancies/Faster Ageing
  - Change all the front-end!

Timeline

Upgrade TDR

module production

Sensor production

Assembly

installation

	50 ns	LS1	25 ns	LS2	25 ns
Start-up	2010 2011 2012	2013 2014	2015 2016 2017	2017 2018	2019 … 20xx

√s (TeV): 0.9 - 7 - 8 - 13 -14

LHCb Upgrade

$\mathcal{L}$ (cm^{-2}s^{-1}): 10^{32} 3-4x10^{32} 4x10^{32} 20 – 30 x10^{32}

$\int \mathcal{L}dt$ 3 fb^{-1} 8 fb^{-1} > 50 fb^{-1}

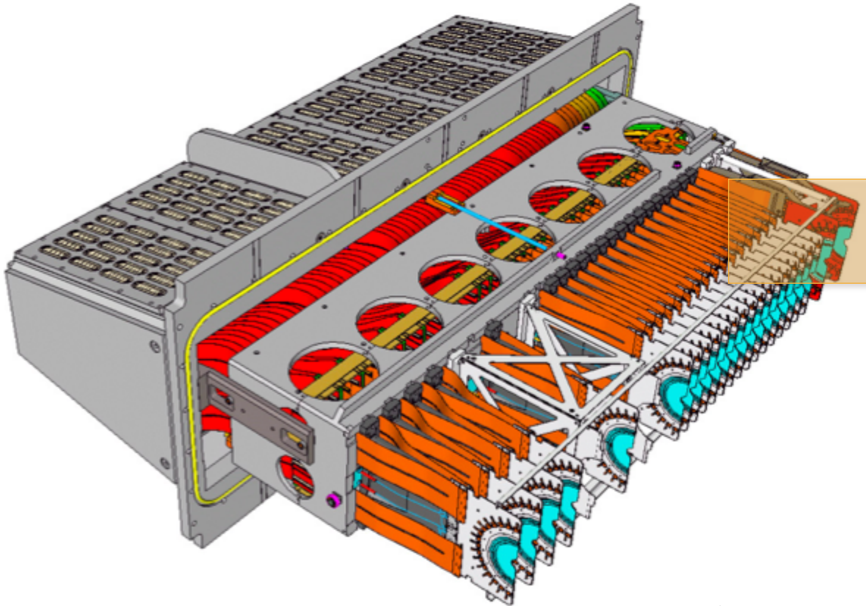
Current upgrade plan still compatible with post LS3 …

Main challenges for the Velo Upgrade

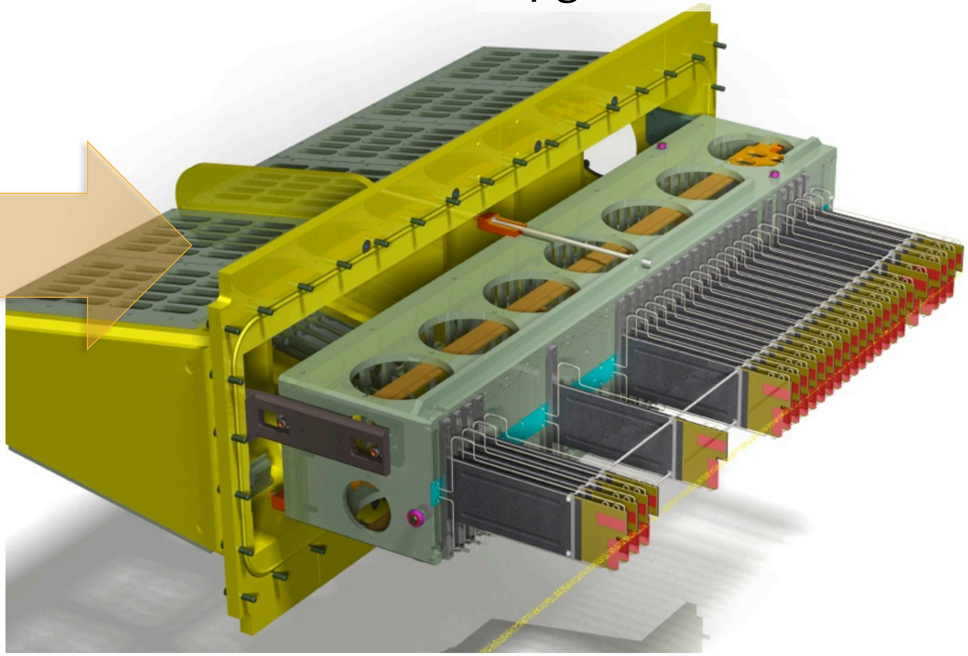
Non uniform Radiation exposure	8×10^{15} n_{eq}/cm^2 @ tip, 0.2×10^{15} n_{eq}/cm^2 @ outer edge
HV tolerance	1000V after 50 fb^{-1}
Readout data rate	~33tracks/Event/module. (LHC: 40 MHz)
Temperature operation	-20 @ tip close to the beam
ASIC power consumption	3W/ASIC; up to 36 W/module;
Material budget	Good IP and tracking resolution currently: • Proper time resolution ~ 50 fs • IP resolution ~ 40 μm (p_T=1GeV)

Upgrade Plan

Current detector Half



Upgrade detector Half



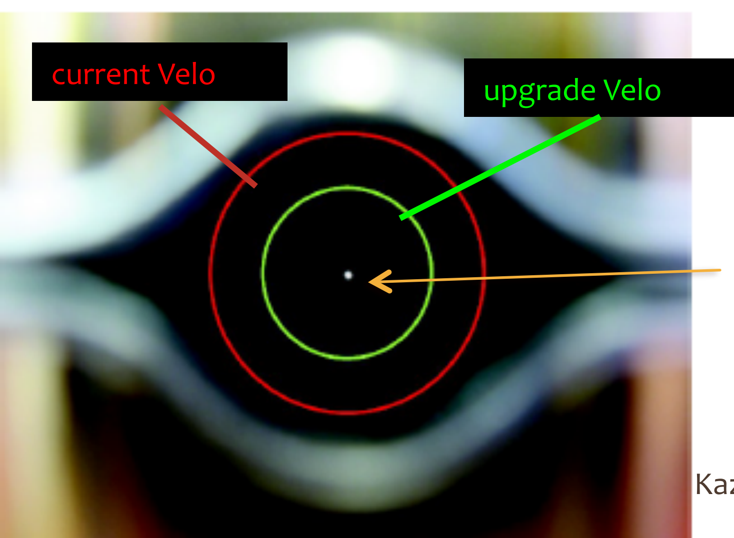
44 C shaped double sided modules (R/ϕ)
88 sensors.

52 L shaped pixel modules
208 sensors.

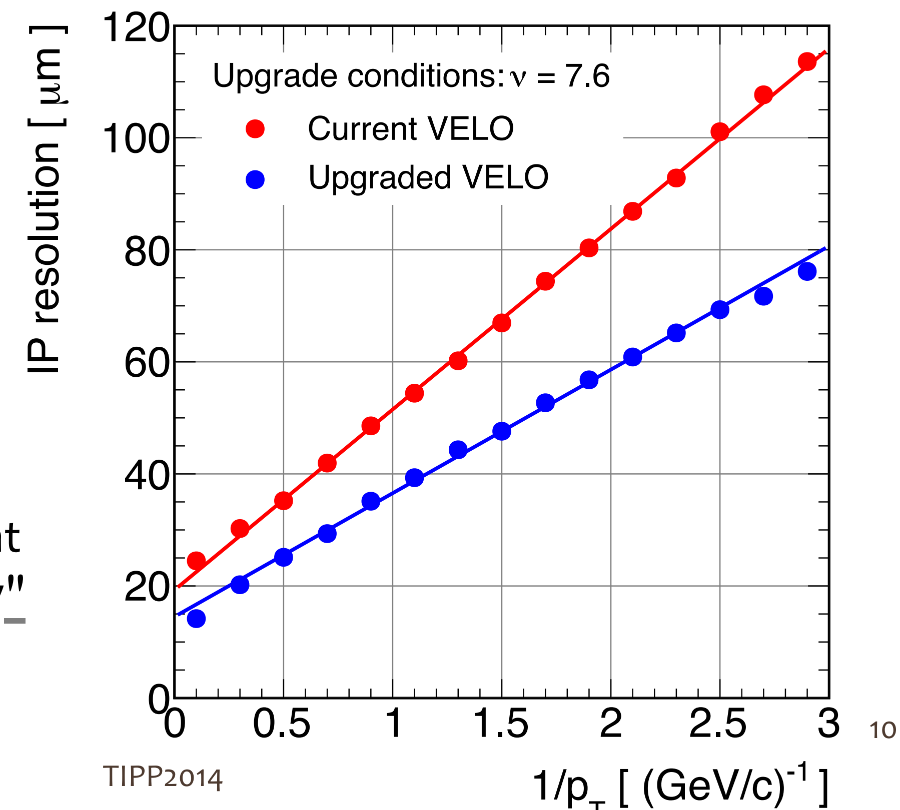
Keep vacuum and motion features.

Changes to improve

- From strips to pixels: Planar Sensors 55x55 μm^2 pixel.
  - Fast and robust pattern recognition.
- Cooling interface needs to come closer to the tip.
  - Plan to use μ-channels etched in a silicon substrate.
    (see P. Rodriguez talk https://indico.cern.ch/event/192695/session/6/contribution/113)
- First active element at 5.1 mm from beam (was 8.2 mm)
- New RF-box required.

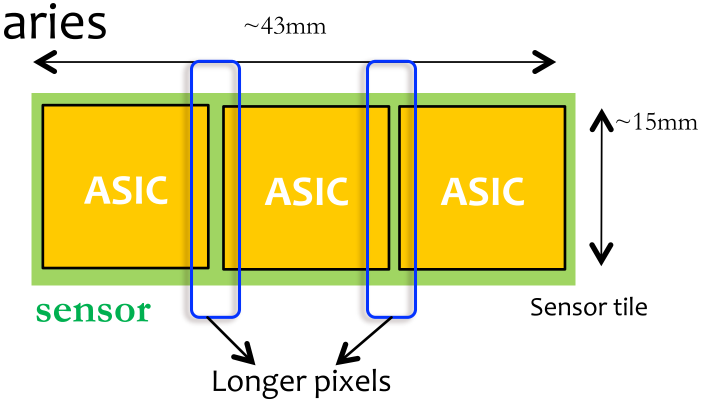


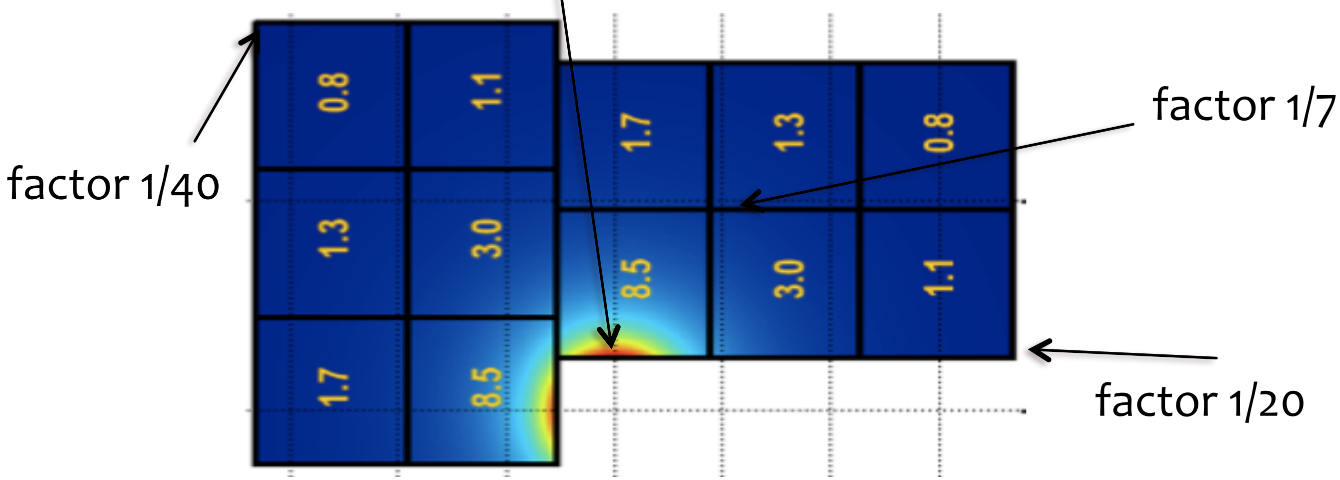
Collision point
“proton view"



Silicon sensors

- Planar silicon, n-in-n or n-in-p under consideration
- Tile for 3 ASIC chips: ~ 43 x 14 mm, 200 μm thick
- 55x55 μm² pixels, elongated pixels at ASIC boundaries
- Non homogeneous irradiation sets constraints on guard ring design
  - Tip close to beam: 8 x 10^{15} n_{eq}, far corner only at 2 x 10^{14} n_{eq}
  - guard ring width ~450 μm
  - Bias of 1000V after 50 fb^{-1}





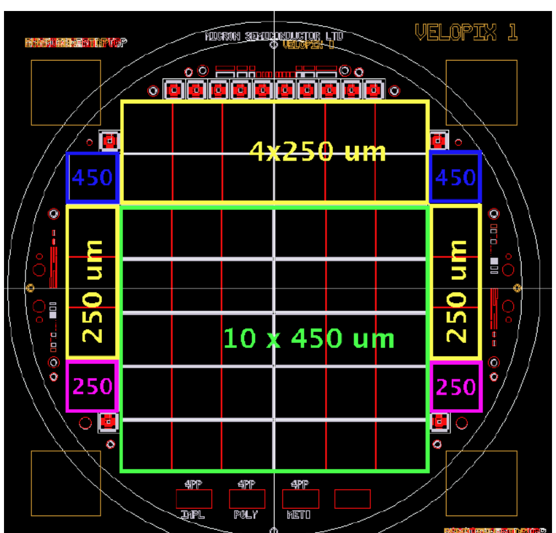
Silicon sensors

- Focus on two vendors with proven track record in radiation hard and HV tolerant sensor designs:

HPK

- n-in-p, 200 um thick
- 450 um guard ring
- 3x1 and single-ASIC sensors

Micron



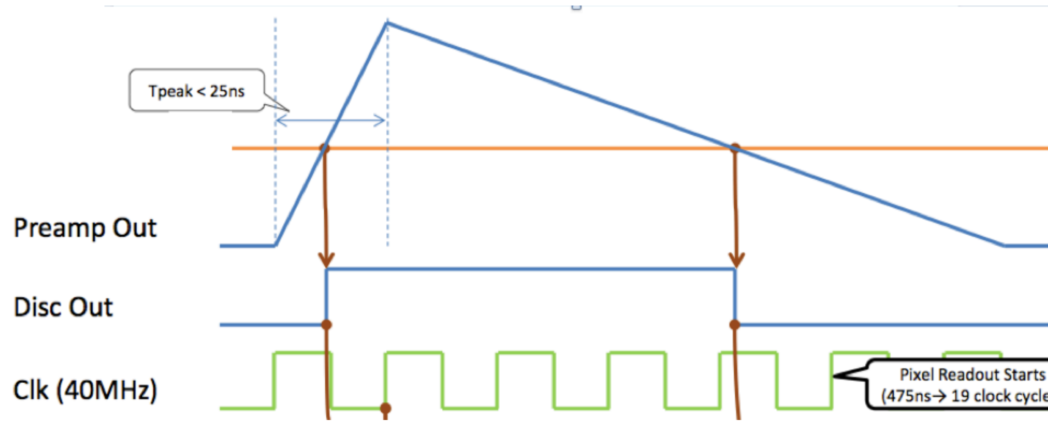
- n-in-n or n-in-p, 150/200 um
- Baseline of 450 um guard ring
- Possibility of reduced width guard rings (250um) and overlapping guard rings on backside in n-in-n case

  - Irradiation and test beam program to validate Sensor and ASIC tech at high rates.
    --- This year!

VELOPix ASIC

TimePix3 chips

- MediPix →TimePix→Timepix3→VELOPix
  - VeloPix designed by CERN and Nikhef
- Square matrix of 256 x 256.
- Technology resistant to required ~400 MRad.
- Key features
  - Data driven readout:
    Each hit time-stamped,
    sent off chip immediately
  - Fast front-end:
    time walk < 25 ns
  - Bunch crossing time stamping
    9 bit
  - SEU protection



- ***VeloPix output hit-rate = ~10 x TimePix3 rate***
- Binary readout – but optional ADC (slow) for calibration
- **Chips will be thinned to 200 μm: minimize material**

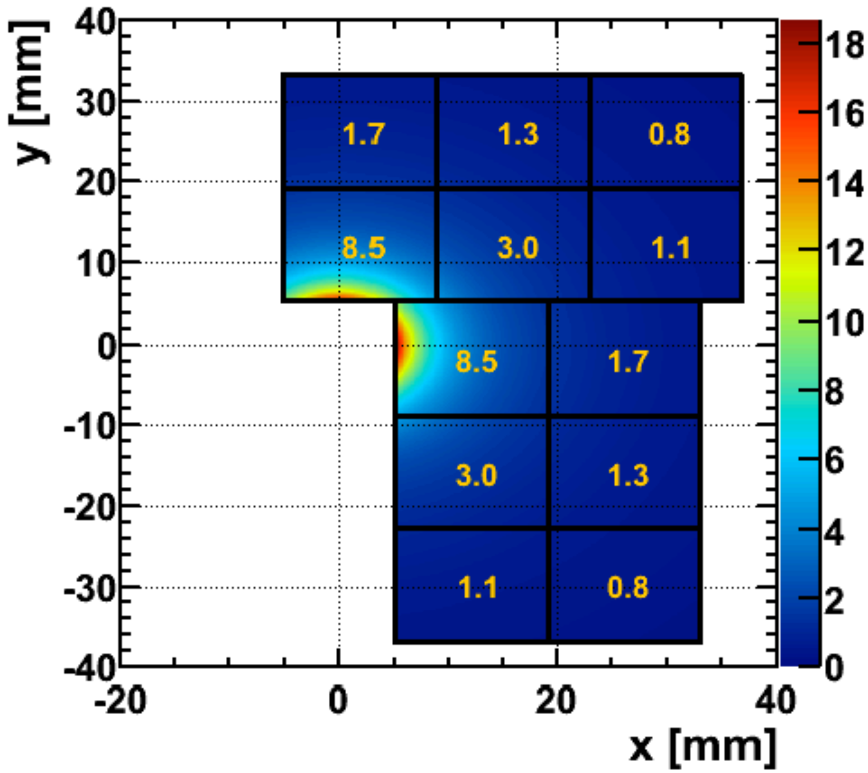
VeloPix challenges

- Average # particles / chip / event
  - average (peak) rate: multiply by 26.8 (40) MHz
- Hottest chip →230 (320) Mtracks/s ~ 600 (900) Mhits/s per chip
  - grouping of pixel hits
    2x4 super pixels→30 % data reduction
  - increase output bandwidth
  - optimize buffering

- Output bandwidth of (hottest) VeloPix:
  - Average: 13 Gbit/s ; peak: 20 Gbit/s
  - 4 links at ~ 5 Gbit/s

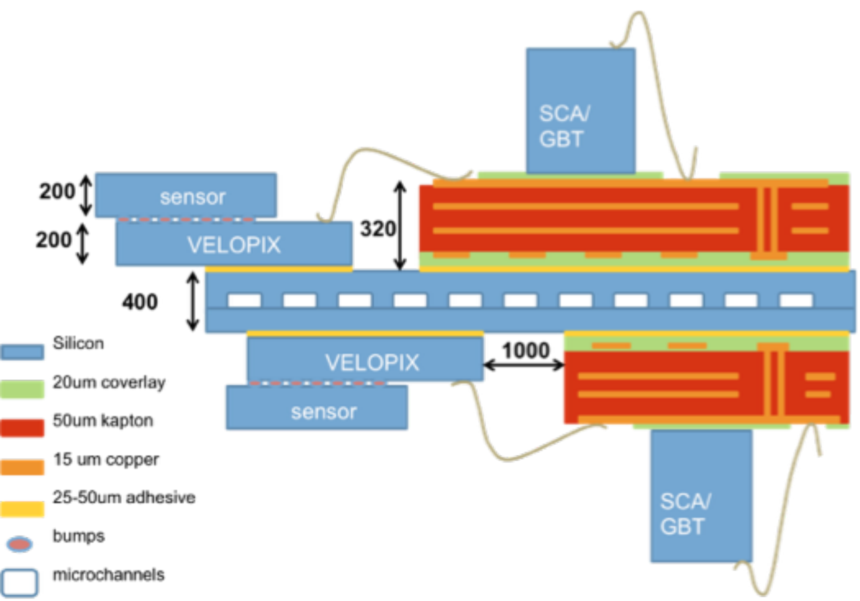
- for first submission summer 2014
- Production quantity chips end 2015

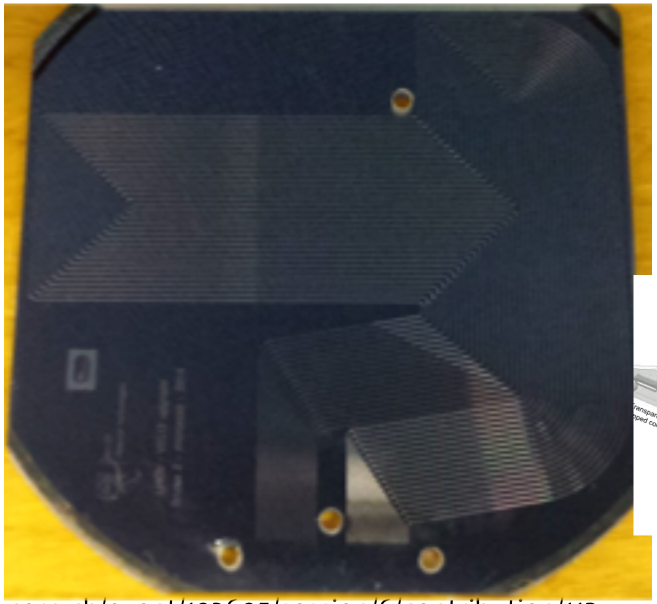
L = 2x10[33] and R_{min} = 5.1 mm, ν = 7.6

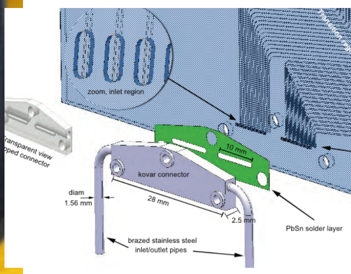


Cooling: micro channel substrate

- Power consumption can go up to ~45 W/module.
- Keep the sensors at < -20 ºC to minimize the effects of radiation damage, and to avoid thermal runaway
- Novel method: evaporate CO_2 via micro-channels etched in Si substrate ➔ Same Thermal Expansion Coefficient (CTE)







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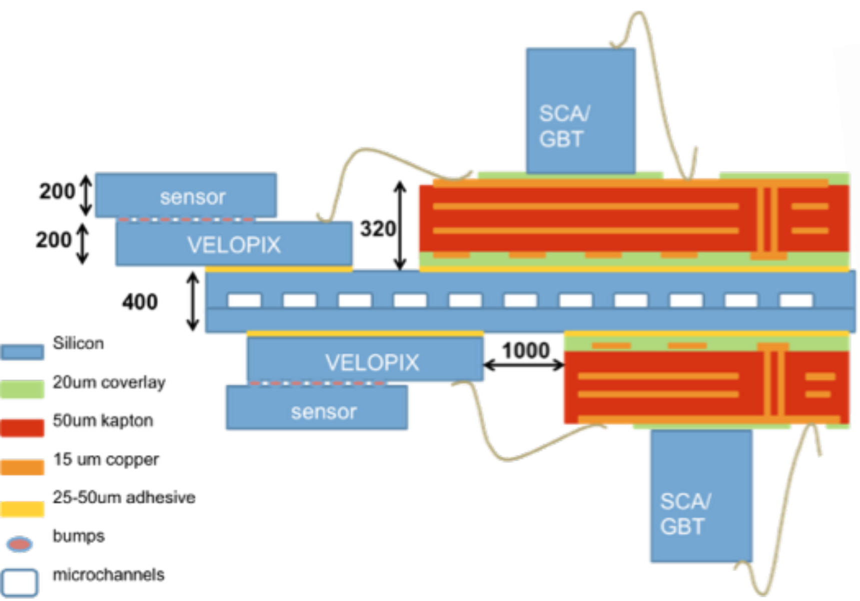

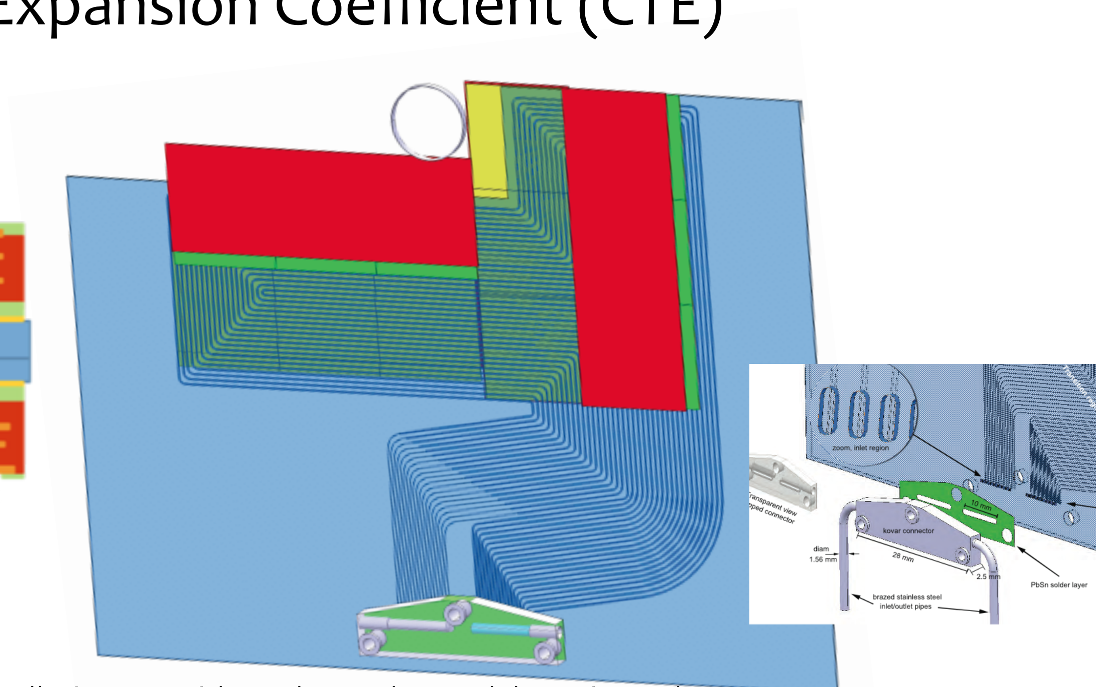

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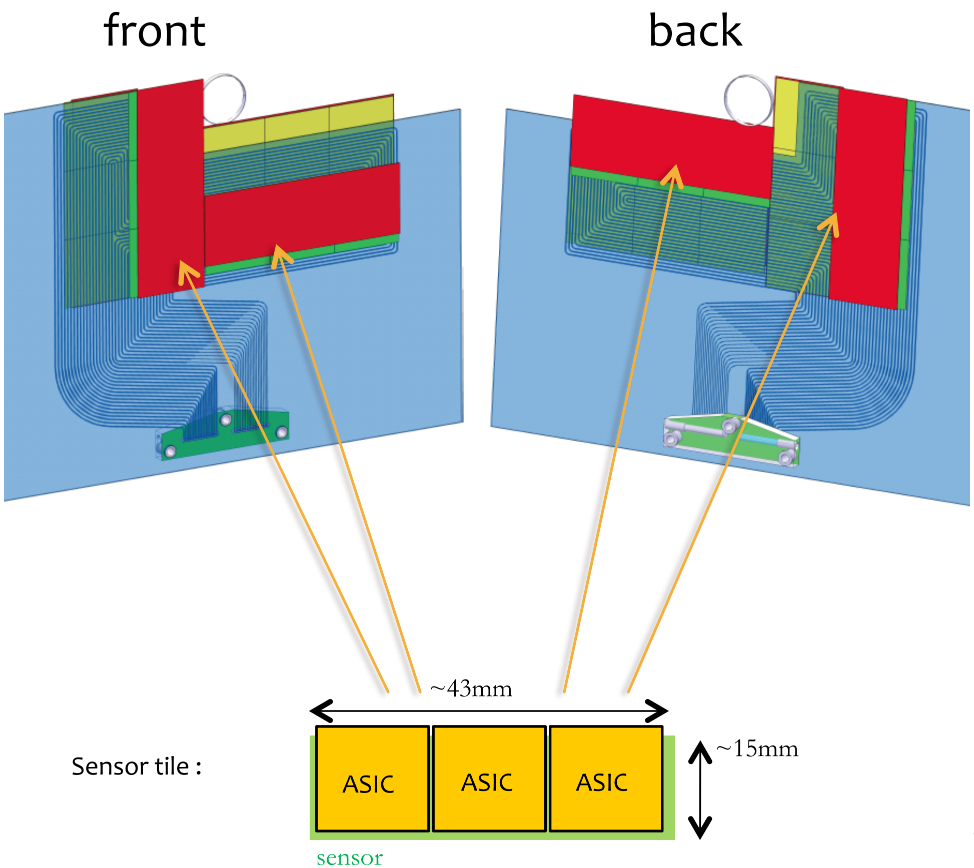
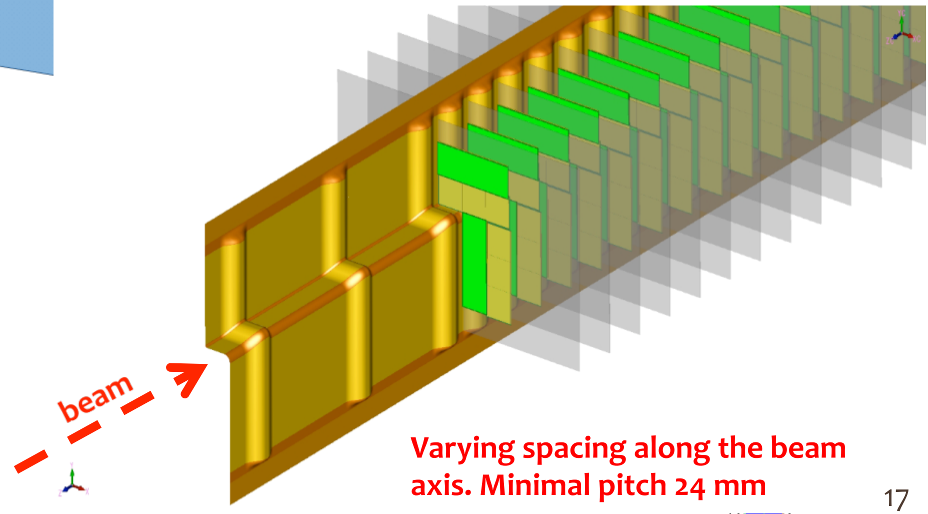
L-shape Pixel Modules



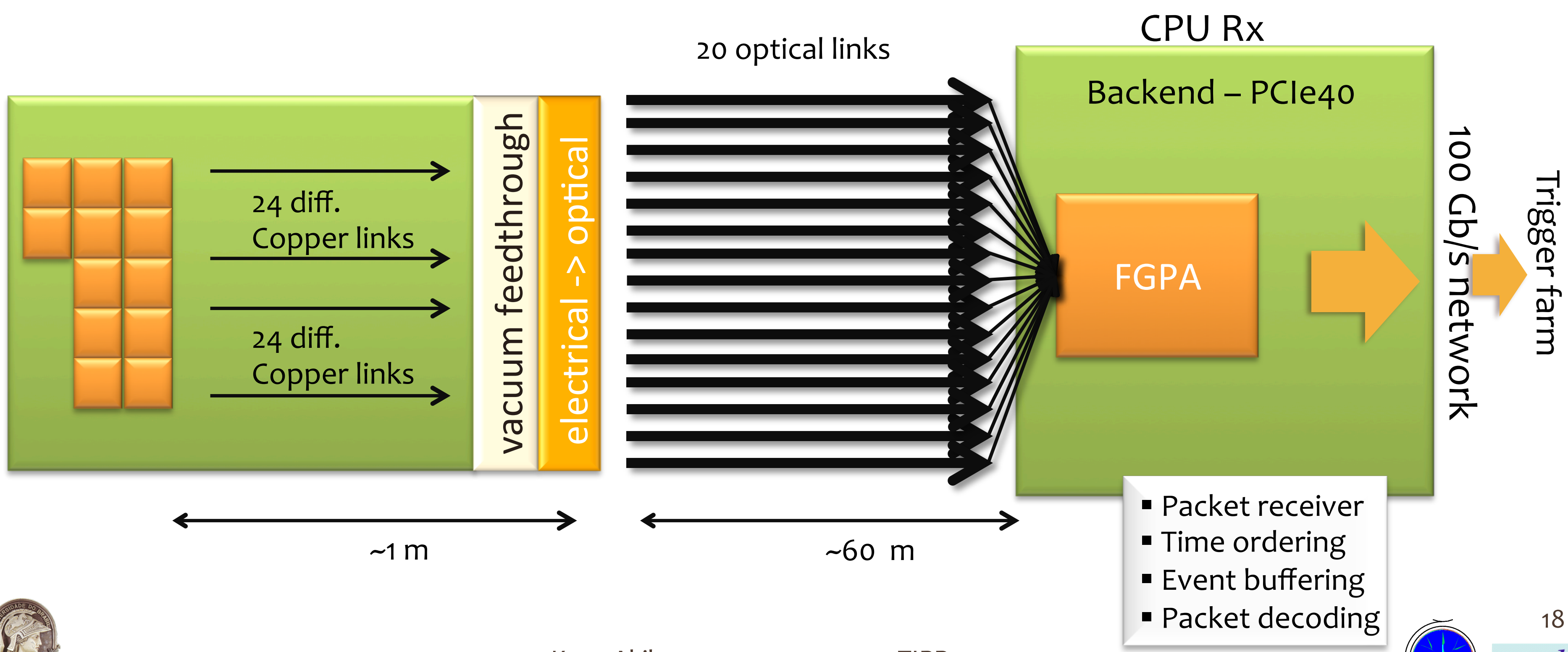
- A 'module' is made of 4 sensor tiles.
  - active area ~100% (except small gaps)
  - Closest pixel is at 5.1 mm from the beam center



Varying spacing along the beam axis. Minimal pitch 24 mm

Data acquisition overview

- LHCb common DAQ boards (PCIE40)
- 48 copper links from chips.
  - Hotter chips demand higher speeds
- Electrical to optical conversion outside of vacuum tank
  - 20 Optical links ~5 Gbit/s each
- 1 FPGA to time order events of 1 module



Upgrade RF Foil

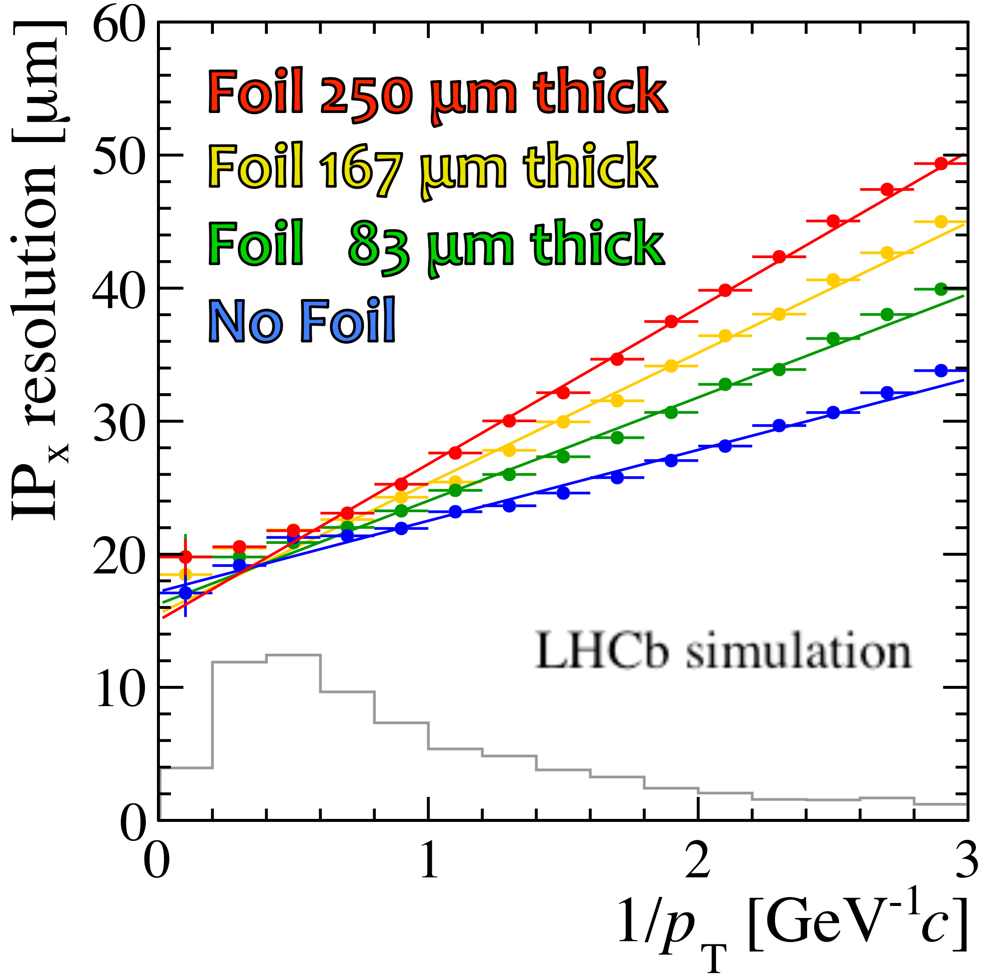
- Requirements
  - Vacuum tight (< 10^{-9} mbar l/s)
  - Radiation hard
  - Low Mass
  - Good electrical conductivity
  - Thermally stable and conductive

•Material and fabrication:

•Aluminium (AlMgMn): 200-350 μm thickness:

•By 5-axis milling of a single homogeneous block

•Chemical etching



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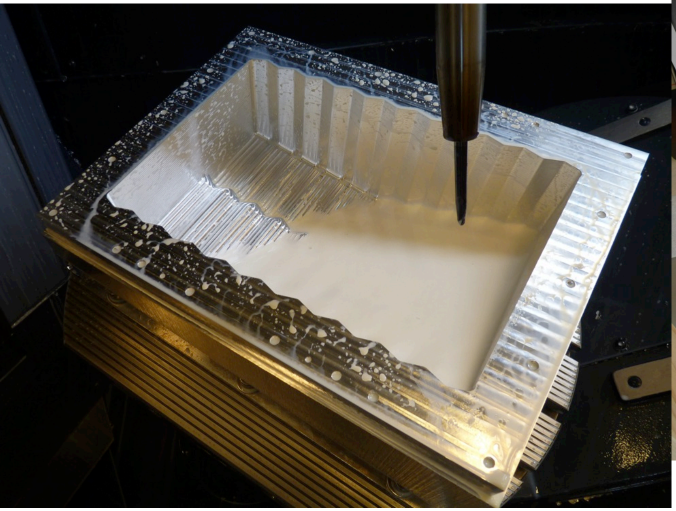
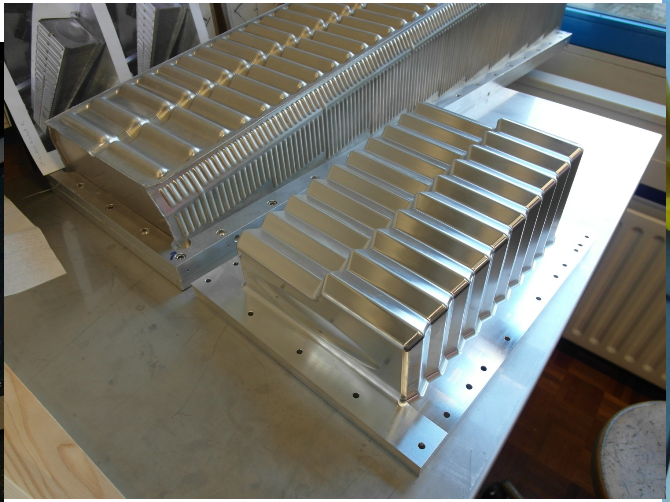
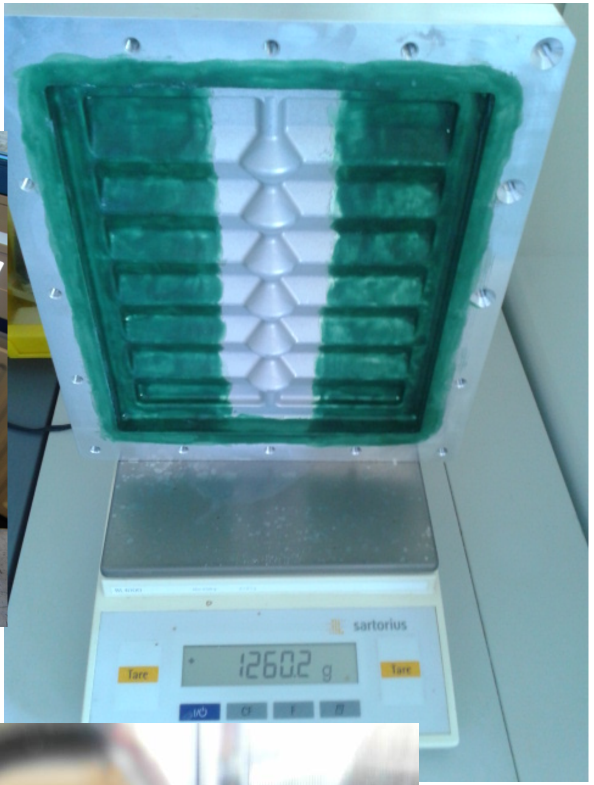
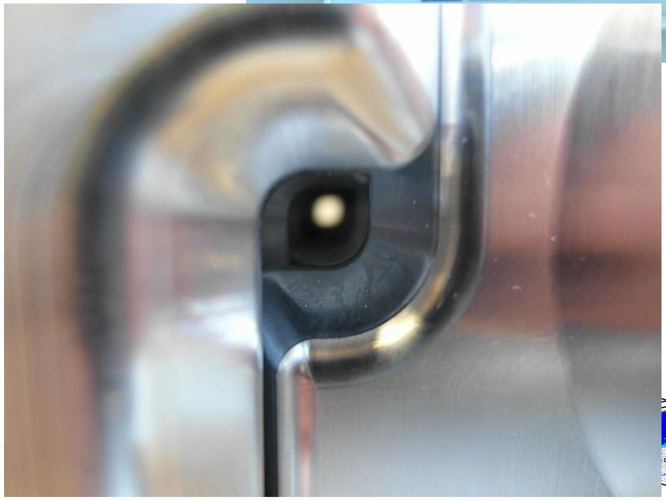








Summary

- We plan to install a fully upgraded detector in the LS2/2018
- With a 40 MHz "triggerless" readout
- Run @ $L = 2 \times 10^{33}\ cm^{-2}\ s^{-1}$ (5x now), but front-end 40 times higher rate.

- Velo subdetector will consist planar silicon pixel sensors with $55 \times 55\ \mu m^2$ pitch
  - Get closer to the collision point
  - Minimize the material

- New ASIC VELOPix with 20 Gbit/s output bandwidth

- Evaporative CO_2 cooling in Silicon with a micro-channel substrate as interface

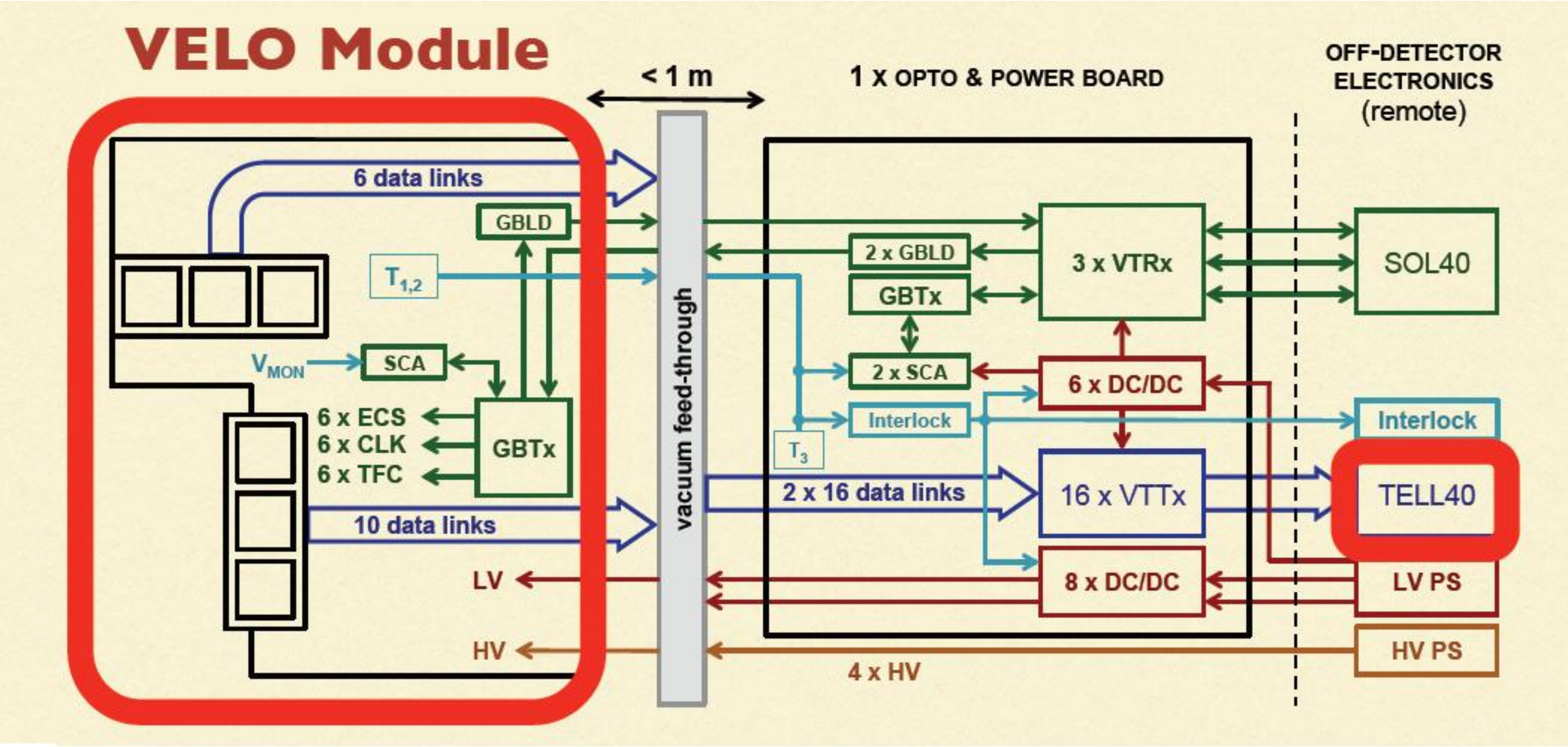
- 300 μm thick RF-box milled from solid block of Aluminum

- Developments for the upgrade going well and on schedule

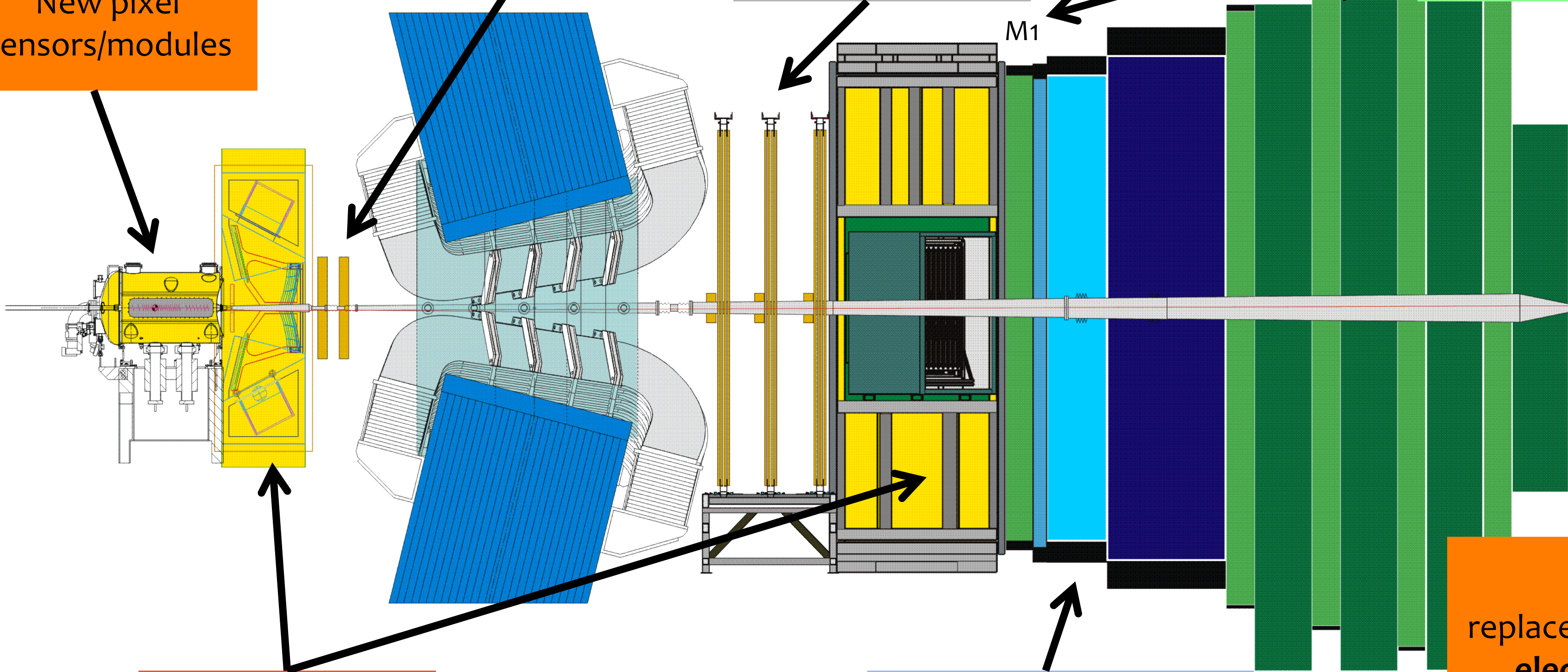
The LHCb VELO upgrade is a very challenging project with many new techniques

Back up

Electronics overview



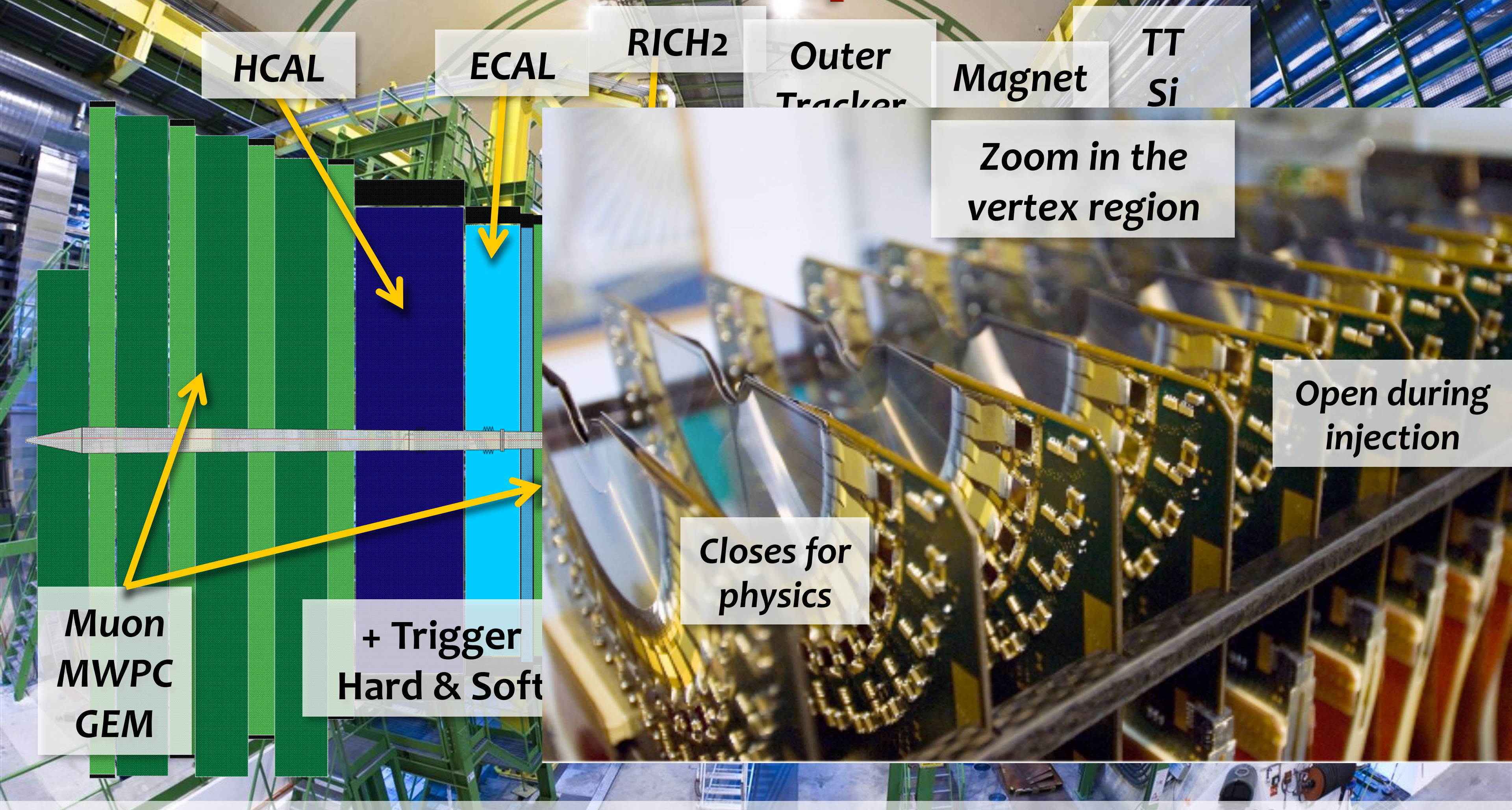
LHCb Upgrade Overview



VeloPix ASIC

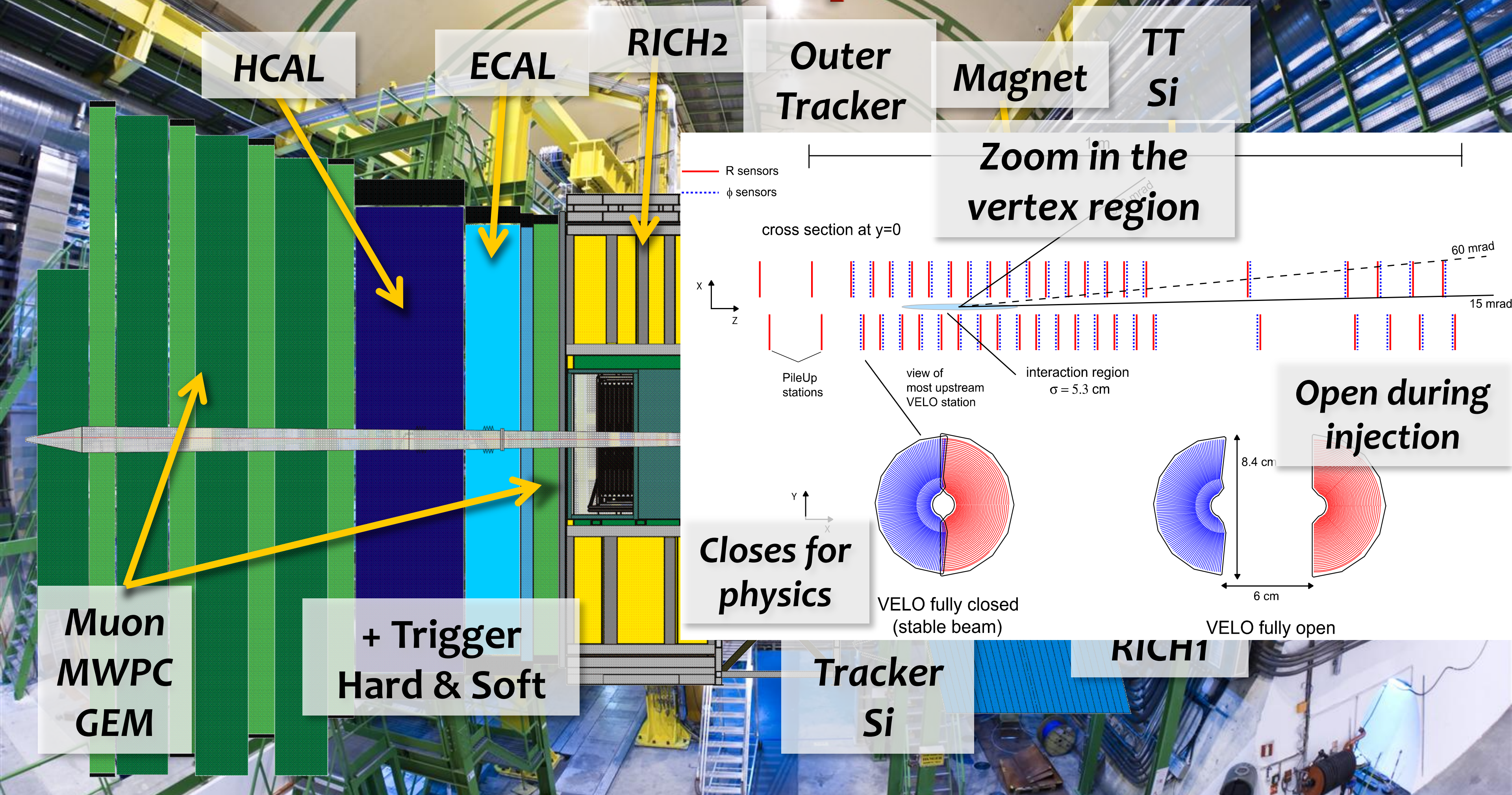
Specification	Timepix3	VeloPix
pixel dimension	55x55 μm^2	55x55 μm^2
matrix size	256x256	256x256
timewalk	< 25 ns	< 25 ns
Time over Threshold range	10 bit	4 bit
leakage current compensation (per pixel)	> 20 nA	> 20 nA
Time stamp resolution	1.6 ns	25 ns
Time stamp range	18 bit	12 bit
sustainable hit rate	40 MHits/s	> 600 MHits/s
output bandwidth	2.5 Gbit/s	> 13.6 Gbit/s
power consumption per chip	< 2 Watts	< 3 Watts
radiation hardness	no spec.	> 400 MRad
single event upset robust	no	yes

The LHCb Experiment



Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

The LHCb Experiment



Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

Main challenges for the Velo Upgrade

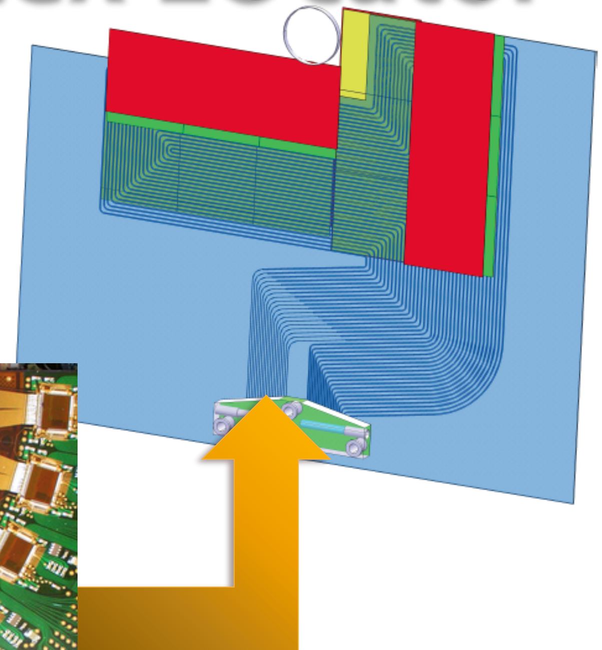
- Completely new front-end electronics and sensor
  - Fast analogue pulse, Ultra fast read out – readout every bunch crossing.
  - High radiation hardness of ~ 400 MRad 8 x 10^{15} n_{eq}/cm^2
- Very high data rate
  - Major changes to front-end back-end electronics and data transport
- Improve the cooling performance
  - Thermal Runaway risk at inner most region
  - New cooling interface design.
- Improve the physics performance… currently:
  - Proper time resolution ~ 50 fs
  - IP resolution ~ 13 + 25/pT μm

The LHCb Experiment

Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

Upgrade of the LHCb VErtex LOcator

- QUICK Current detector overview
- Upgrade motivation
- VELO Upgrade plan
- Upgrade R&D
  - Sensors
  - ASIC
  - Cooling
  - Infrastructure
- Summary



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