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Radiation-hard Active Pixel Sensors for HL-LHC Detector Upgrades based on HV/HR-CMOS Technology

We explore the concept of using deep-submicron HV-CMOS and imaging processes to produce a drop-in replacement for traditional radiation-hard silicon sensors. Unlike fully integrated monolithic active pixel sensors (MAPS), such active sensors contain simple circuits, e.g. amplifiers and discriminators, but still require a readout chip - which can be a traditional strip or pixel readout chip or a tailor-made one without any analogue circuits. This approach yields most of the advantages of MAPS (improved resolution, reduced cost and material budget, etc.), without the complication of full integration on a single chip; in particular, high-speed clocked circuits necessary for trigger handling and efficient communication can be kept separated from the crosstalk-susceptible pre-amplifiers.

The design of test ASICs produced in different processes, characterization results before and after irradiation and experience obtained with pixel and strip readout will be shown. Finally, plans for further submissions with higher-resistivity substrates will be outlined and an outlook will be given on application options for HL-LHC detector upgrades.

Summary

Luminosity upgrades are discussed for the LHC which would make upgrades to the LHC detectors necessary, in particular new, even more radiation-hard and granular sensors for the inner detector region.

Deep-submicron HV-CMOS processes feature moderate bulk resistivity and HV capability and are therefore good candidates for drift-based radiation-hard monolithic active pixel sensors (MAPS). It is possible to apply up to $\sim 100V$ of bias voltage leading to a depletion depth of $\sim 10-20 \mu m$. Thanks to the high electric field, charge collection is fast and nearly insensitive to radiation-induced trapping. Due to the still rather high dopant concentration, almost no radiation effect is expected to the depletion voltage. Imaging processes using high-resistivity substrates could provide significantly more signal charge thanks to larger depletion depths and are therefore also studied.

We explore the concept of using such HV/HR-CMOS processes to produce a drop-in replacement for traditional radiation hard silicon sensors. Such active sensors contain only simple circuits to amplify and either discriminate or condition the basic pulses created by charged particles. A traditional readout chip is still needed to receive and organize the data from the active sensor and handle high-level functionality such as trigger management. The devices are tested with the ATLAS FE-I4 and Timepix pixel readout chips and the LHCb Beetle and ATLAS ABCN25 strip readout chips. Either strip-like or pixel-like readout can be selected on the same device.

While a readout chip is still needed (unlike the case of an ideal monolithic MAPS device), the active sensor approach offers many advantages: such sensors can be fabricated in a fully commercial CMOS process without need for special substrates or processing and will therefore cost less than traditional diode sensors, they can be thinned to the limit of the collection layer resulting in much lower mass, they require relatively low bias voltage, and they can operate at room temperature or with only moderate cooling after irradiation. In addition, they can contain sub-pixels with smaller pitch than the readout chip and improve the spatial resolution compared to standard sensors by encoding the hit sub-pixels in the signal sent to the readout chip.

From a practical perspective, maintaining the traditional separation between sensing and processing functions lowers development cost and makes use of existing infrastructure. Active sensors can also be seen as a first step towards 3D-integrated electronics in which the analogue tier contains the sensor while the digital tier can contain only purely digital circuits. The number of required DC connections between the two tiers could be small while data transmission could be done using AC coupling hence reducing the complexity and required number of inter-chip connections.

To explore the performance and radiation hardness of active sensors, so-called HV2FEI4 ASICs were produced in the AMS H18 process. Their (sub-)pixels of $33 \times 125 \mu\text{m}$ size are combined to match the respective readout chip: for the pixel readout, three HV-CMOS pixels are multiplexed onto one FE-I4 pixel such that the hit pixels are encoded by the pulse height; the chips are just glued to each other, capacitive data transmission is used. In this way, the position resolution of the HV-CMOS sensor can be significantly better than the granularity of the readout chip suggests. For the strip readout, the pixel cells are combined to form virtual strips. Here, the z-position of the hit is encoded via the discriminator's pulse height and can be evaluated by analogue strip readout electronics like the Beetle chip. Future strip readout concepts foresee a digital encoding of the z position using a modified ATLAS readout chip (ABC').

To explore alternative processes, the chip concept was ported to a GlobalFoundries 130 nm HV-CMOS process and first prototypes have been characterised before and after irradiation. In addition, a submission on higher resistive substrates is currently being prepared.

The presentation will give an overview of the characterization results of the prototype chips and highlight first results with irradiated and unirradiated samples in the laboratory and in beam tests. Finally, future prospects within the LHC upgrade and beyond will be discussed.

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