Contribution ID: **317** Type: **Poster**

An FPGA-based full mesh enabled ATCA general purpose processor board

The Pulsar II is an FPGA-based full mesh enabled ATCA general purpose processor board, its design is motivated by the silicon-based tracking trigger needs for LHC experiments. Some of the main challenges of silicon-based tracking trigger are the complex data dispatching and the pattern recognition and track fitting. Data dispatching is where the hits from many thousands silicon modules must be organized and delivered to the appropriate eta-phi trigger towers. Since the efficient data dispatching for time and regional multiplexing requires high bandwidth, low latency, and flexible real time communication among processing nodes, a full mesh backplane based hardware platform is a natural fit. An FPGA-based full mesh enabled ATCA board called Pulsar II has been designed at Fermilab with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth board-to-board communication channels. In addition, user-defined mezzanine cards can be designed for Pulsar II, and can be used either for data communication or as pattern recognition engine. In this talk we describe the relevant silicon based tracking trigger needs, our Pulsar 2 design and test methodology, prototype performance results and experience gained in the process.

Summary

For more information, please visit Pulsar II web page:

http://www-ppd.fnal.gov/EEDOffice-w/Projects/ATCA/

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Track Classification: Data-processing: 3b) Trigger and Data Acquisition Systems