TIPP '14 International Conference on Technology and Instrumentation in Particle Physics
2 – 6 June 2014 / Amsterdam, The Netherlands
"Instrumentation as enabler of Science"

Microfabrication Activities in the Engineering Office of the PH-DT Group at CERN

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CERN | PH-DT Detector Technologies

BE Beams
EN Engineering
FP Finance and Procurement
GS General Services
HR Human Resources
IT Information Technology
PH Physics
TE Technology

AGS : Administration and General Services
ALICE : A Large Ion Collider Experiment
ATLAS : A Toroidal LHC ApparatuS
CMS : the Compact Muon Solenoid experiment
DT : Detector Technologies
EDU: Educational group
ESE : Electronics System for Experiments group
LCD : Linear Collider Detector
LHCb : The Large Hadron Collider Beauty experiment
SFT : SoFTware design for experiments group
SME : Small and Medium Experiments team
TOTEM : TOTal cross section, Elastic scattering and diffraction dissociation Measurement at the LHC
TH : THeoretical physics unit

DI: Detecior Infrastructure
DD: Detector Development
EO: Engineering Office
EM1: Engineering & Mechanics 1
EM2: Engineering & Mechanics 2
TP: Technology & Physics

microEngineering

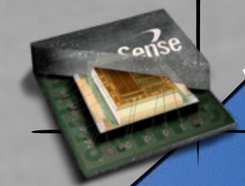
- microScint
  - development of a microfluidic scintillation detector
- microCool
  - implementation of microfabricated on-detector cooling systems
- microHell
  - study of heat transfer of superfluid HeII in microfluidic networks
- microSystems engineering
  - microFabrication
  - integration of microfabricated devices in detectors
  - development of a methodology to estimate the mechanical performance of (silicon) μ-devices

Microsystems are investigated since 2010 in the CERN Physics Department (PH) by the Detector Technologies Group (PH-DT) in close collaboration with the EPFL Microsystems Laboratory (LMIS4).

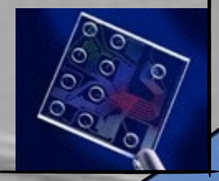
The fabrication of the microsystems is performed by CERN in the class 100 MEMS cleanroom of the Center of MicroNanoTechnology of EPFL in Lausanne, Switzerland

lab-on-a-chip

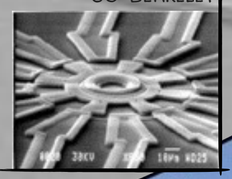
2013
Nine-Axis MEMS
Gyro + Accelerometer + Compass



1999
DNA microarray
ex. Affymetrix

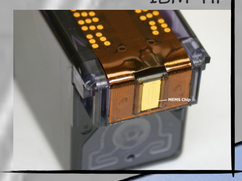


1988
Electrostatic Motor
UC-Berkeley



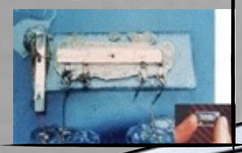
microfluidics

1977
Inkjet nozzle
IBM-HP

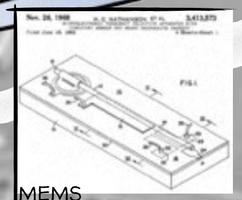


microelectronics

1958
Integrated Circuit
Texas Instrument



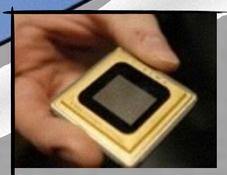
Transistor
Bell
1947



MEMS
H. Nathanson
1967

MEMS
MicroElectroMechanical Systems

LIGA
W. Ehrfeld
1982



Digital Mirrors Display
Texas Instruments
1996

Optical Switch
Lucent
2002

MOEMS
MicroOptoElectroMechanical Systems

microfabrication techniques

Bulk micromachining

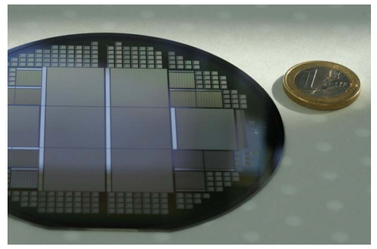
mechanical structures are etched in the substrate

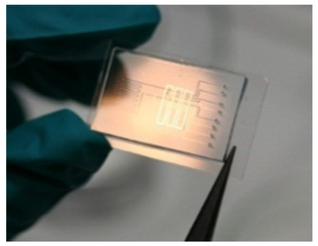
Surface micromachining

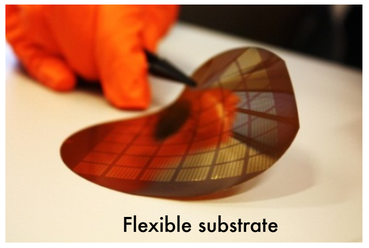
layers of material are deposited on the substrate, patterned and selectively removed

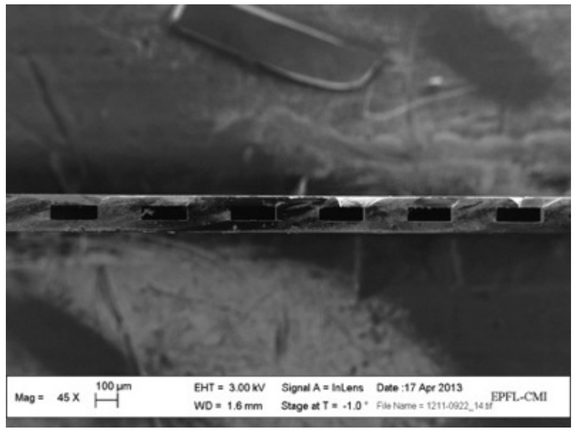
Substrates

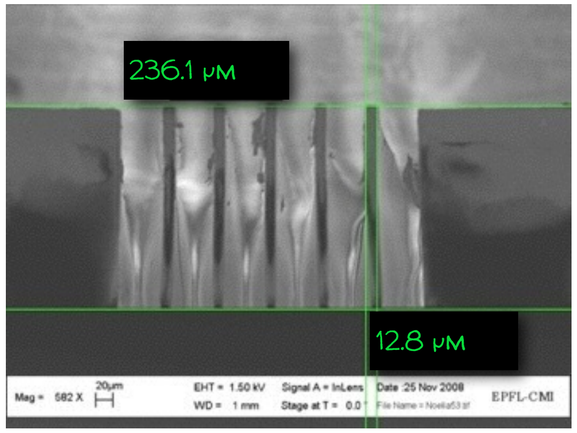
round wafers 3", 4", 6", 8", 12"...
Silicon, SOI, glass, GaAs, SiC, Ge, polymers...

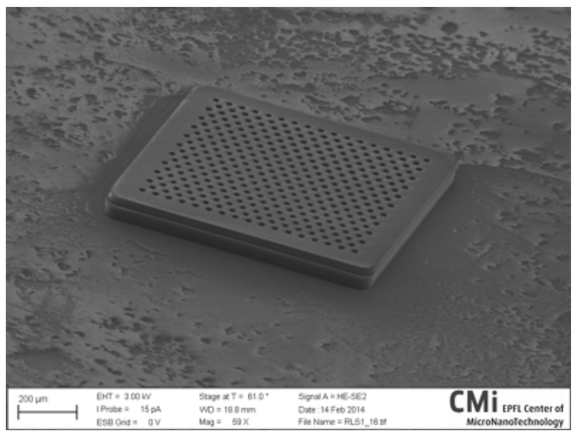


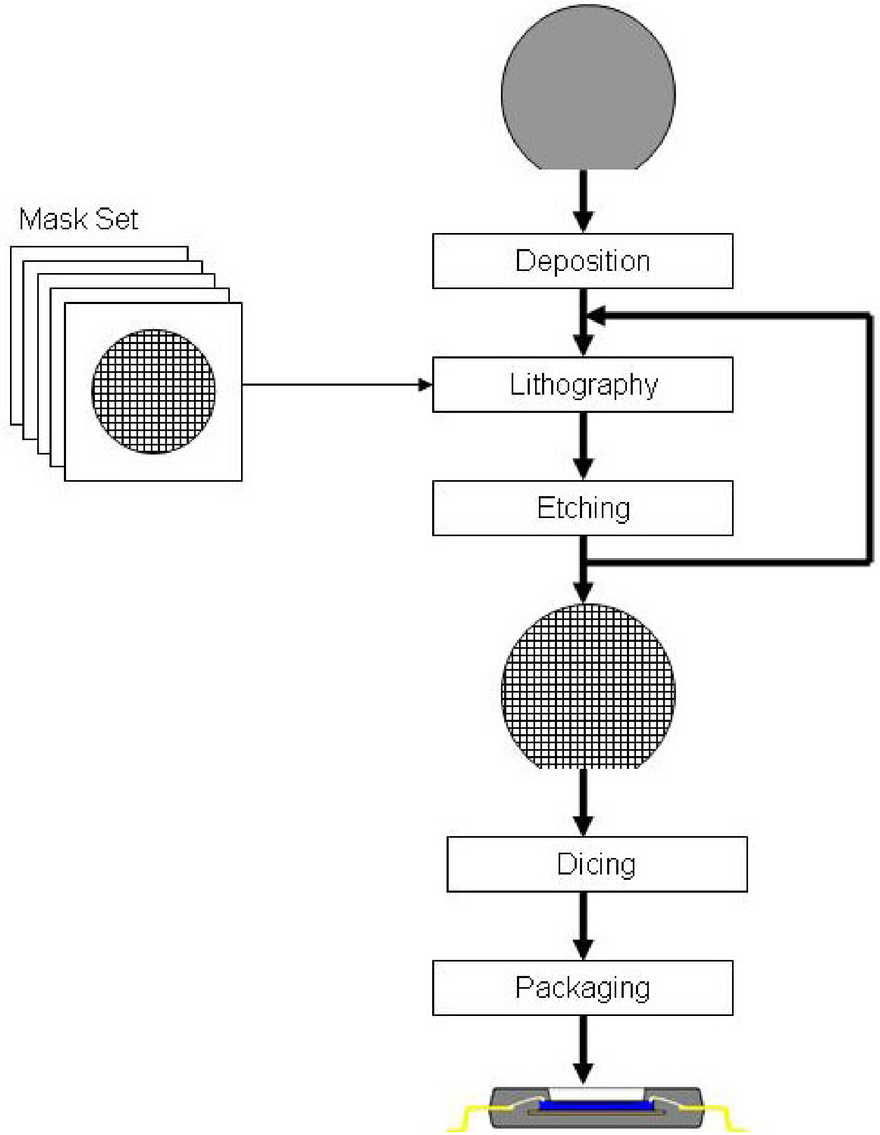






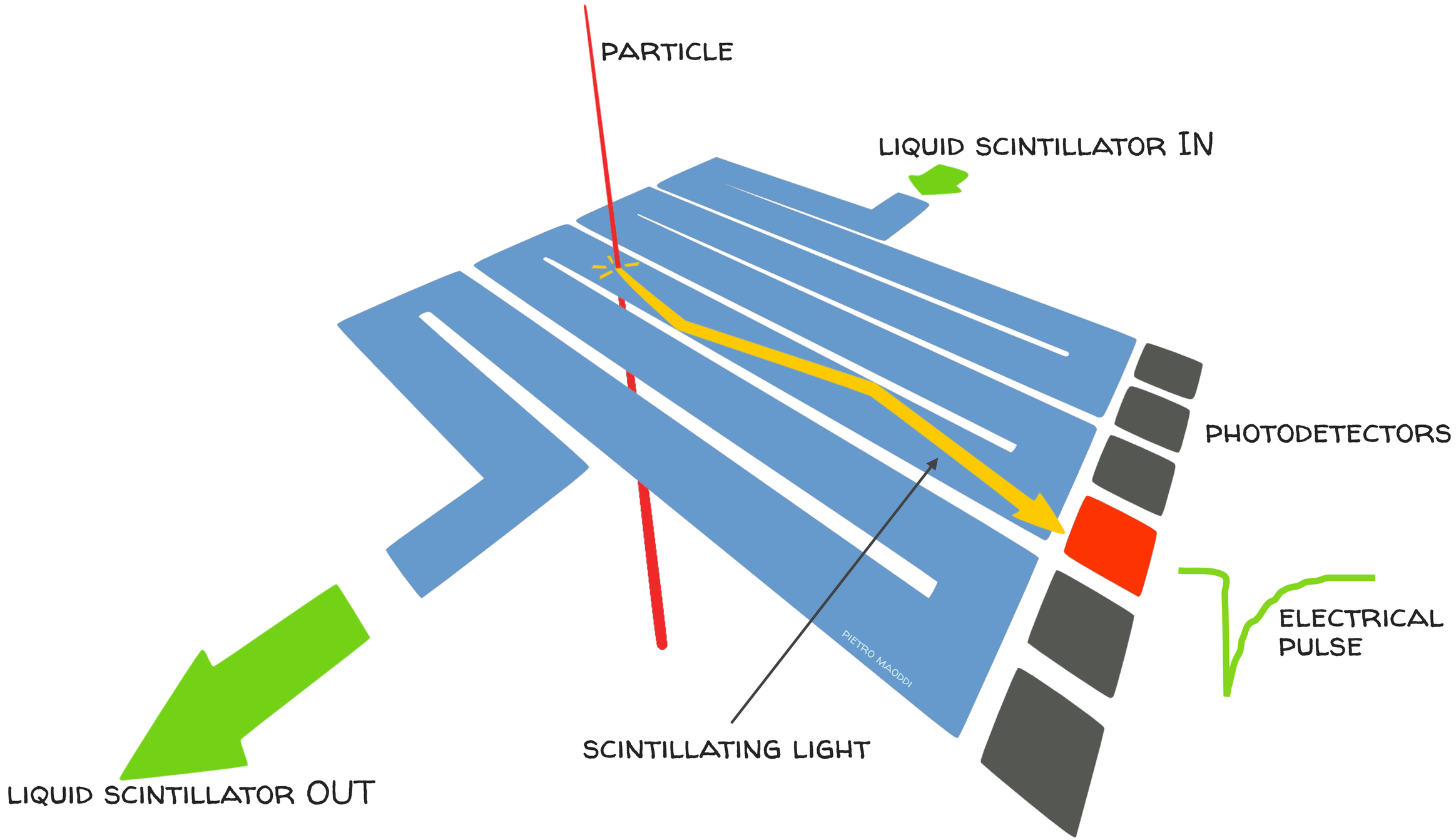






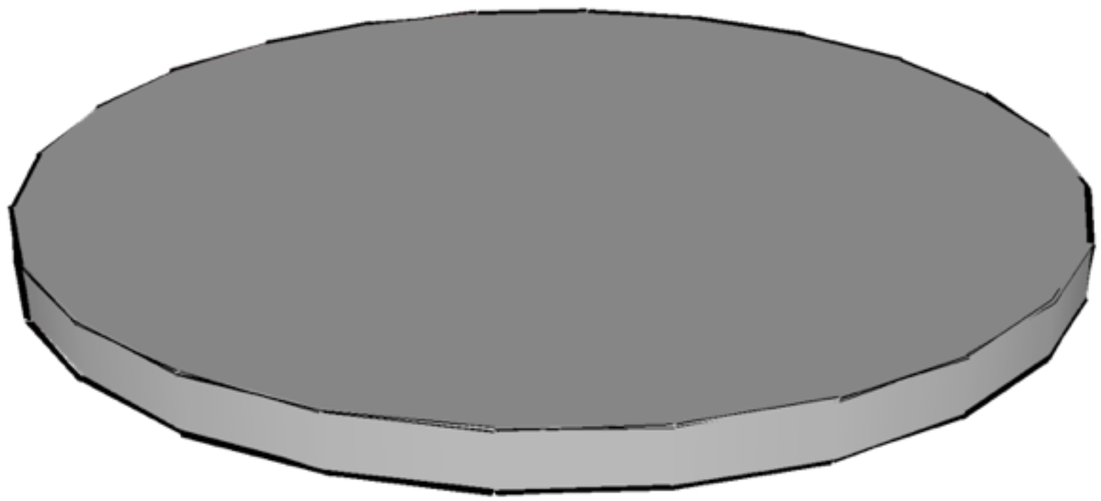
http://www.electronicproductsktn.org.uk, 2007

microScint


PARTICLE
LIQUID SCINTILLATOR IN
PHOTODETECTORS
ELECTRICAL PULSE
PIETRO MAODDI
SCINTILLATING LIGHT
LIQUID SCINTILLATOR OUT

1st microScint protos made of SU-8 photoresist

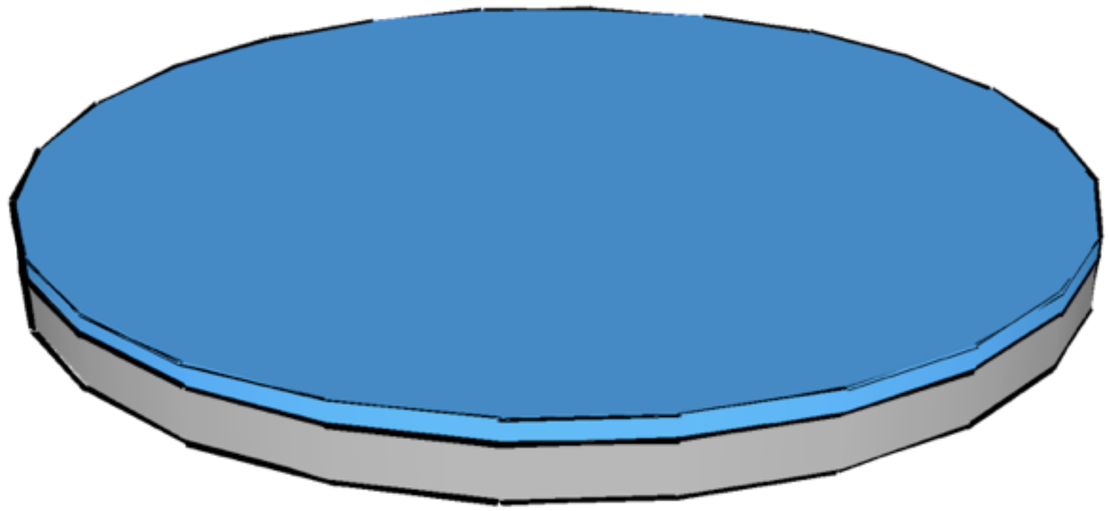
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



SILICON SUBSTRATE

1st microScint protos made of SU-8 photoresist

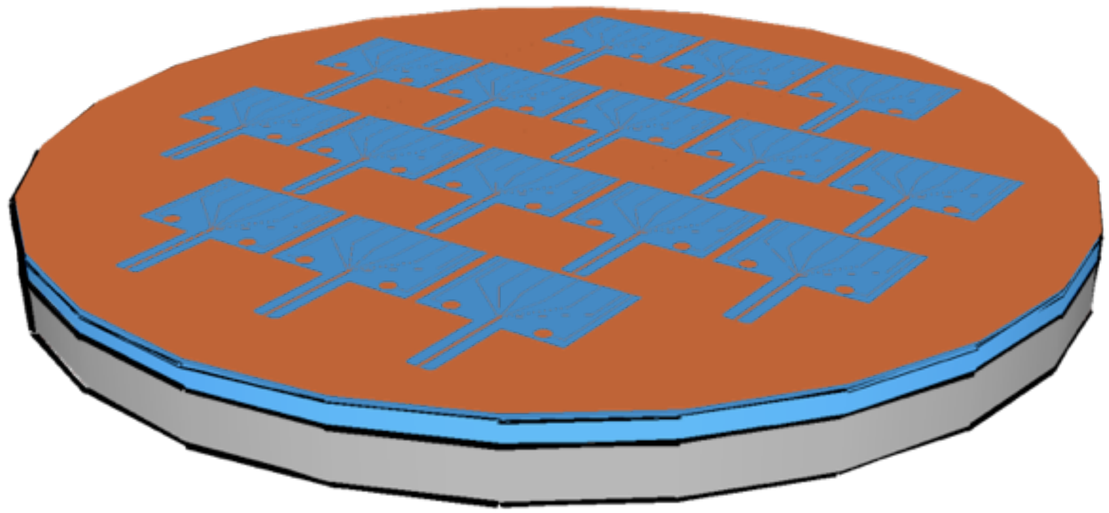
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



PHOTORESIST SPIN COATING

1st microScint protos made of SU-8 photoresist

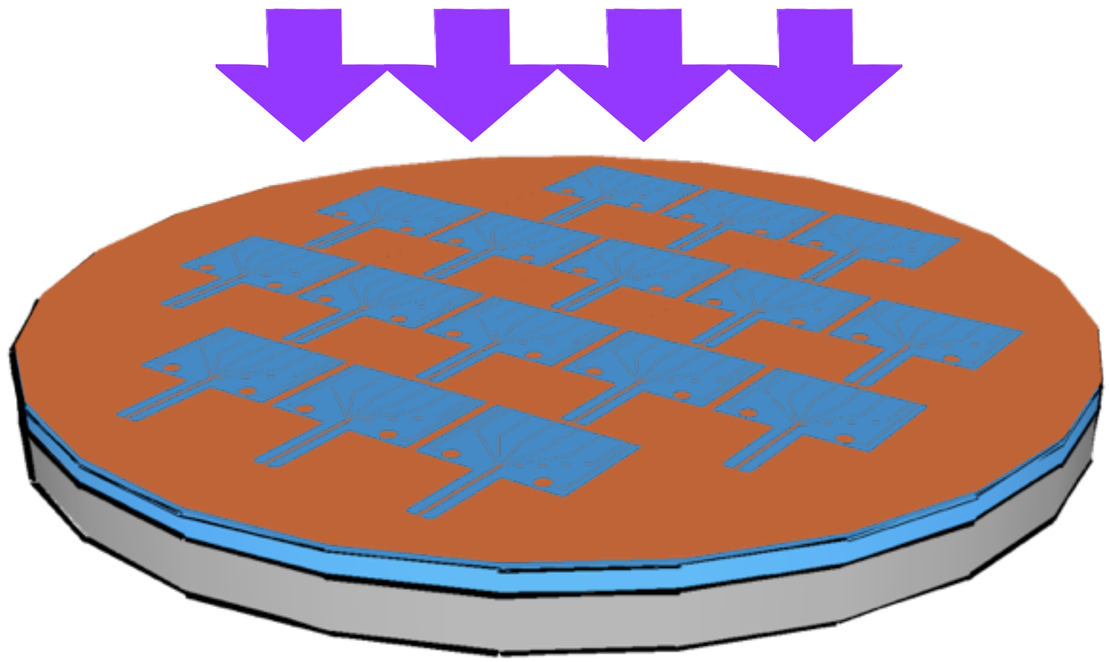
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



MASK ALIGNMENT

1st microScint protos made of SU-8 photoresist

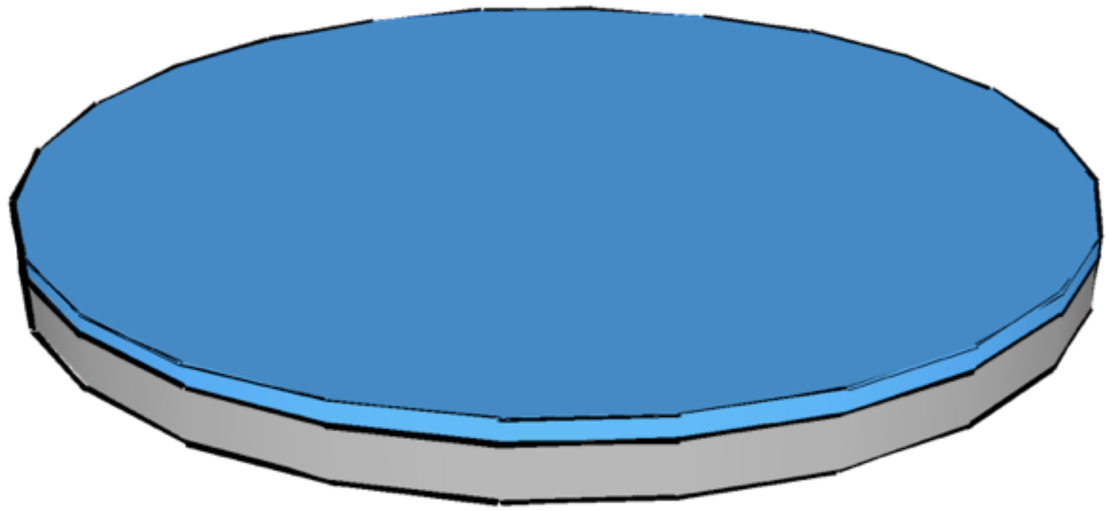
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



UV EXPOSURE

1st microScint protos made of SU-8 photoresist

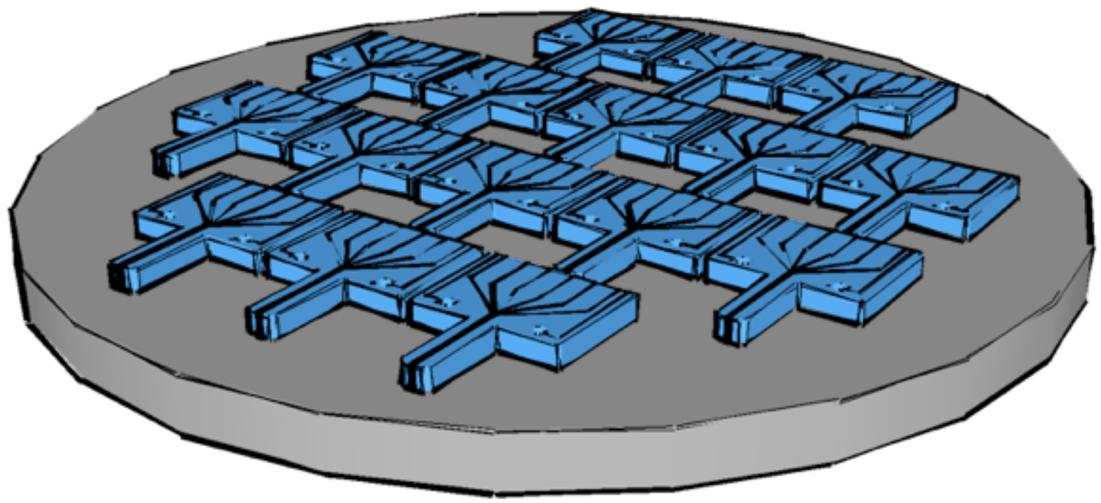
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



UV EXPOSURE

1st microScint protos made of SU-8 photoresist

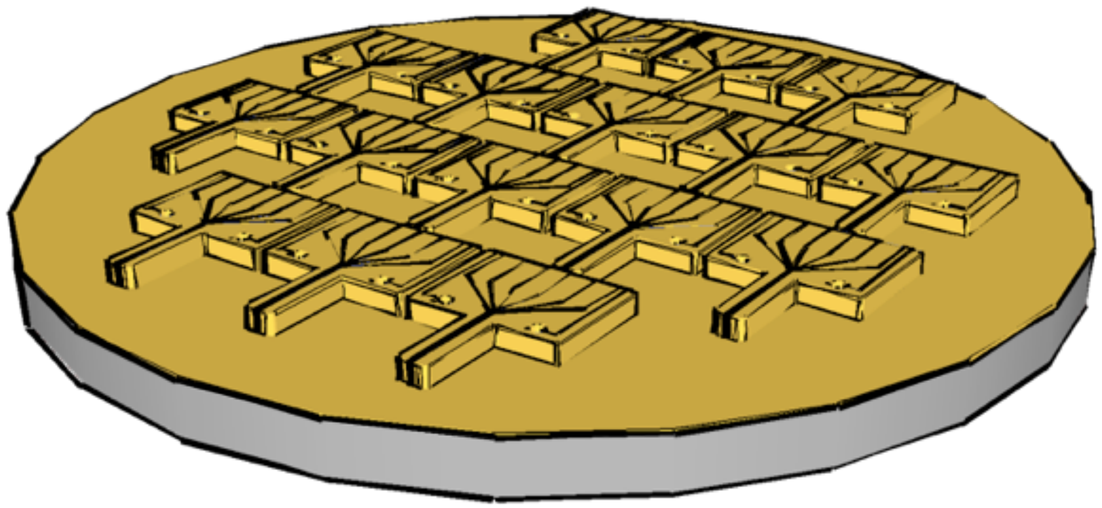
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



DEVELOPMENT

1st microScint protos made of SU-8 photoresist

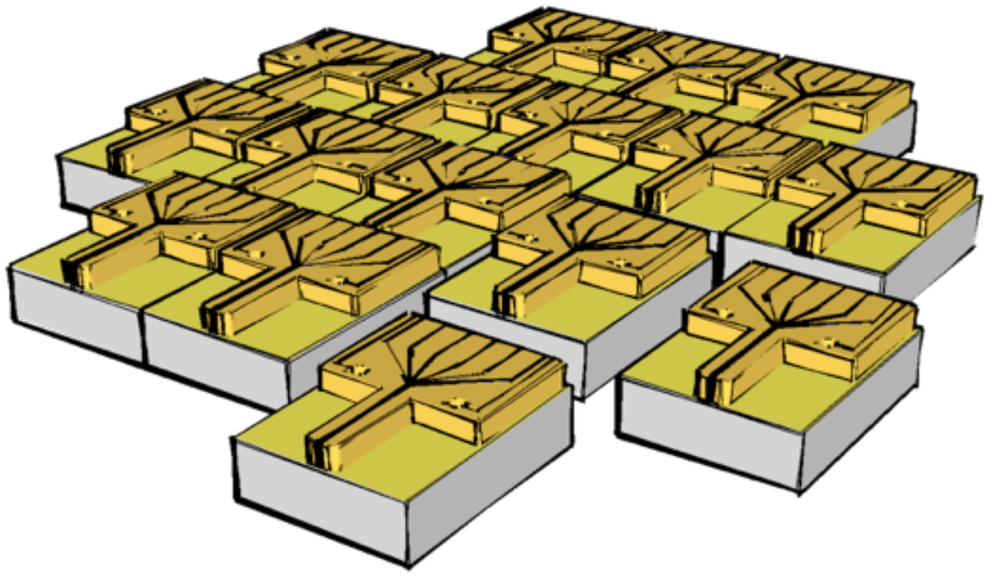
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



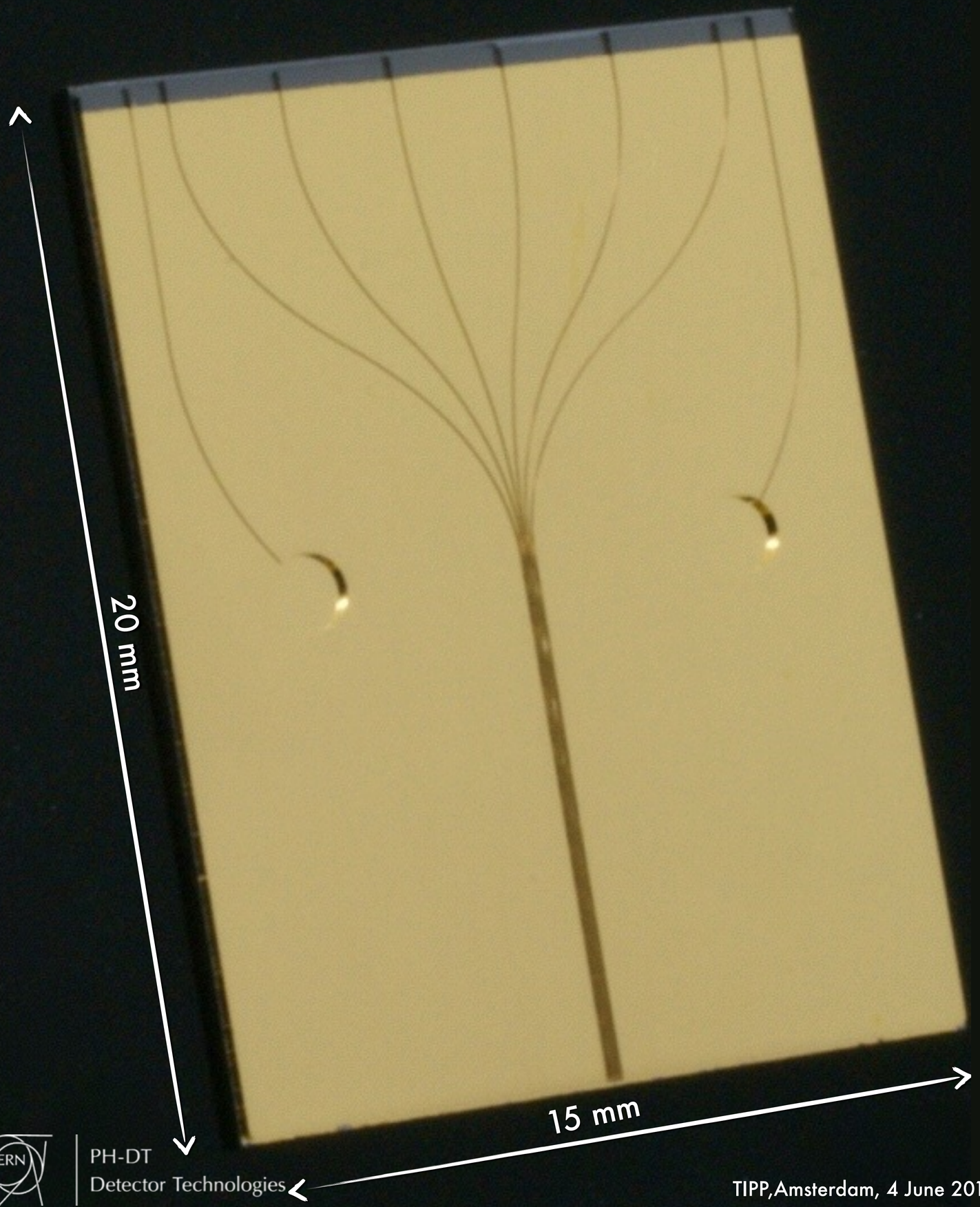
METALLIZATION

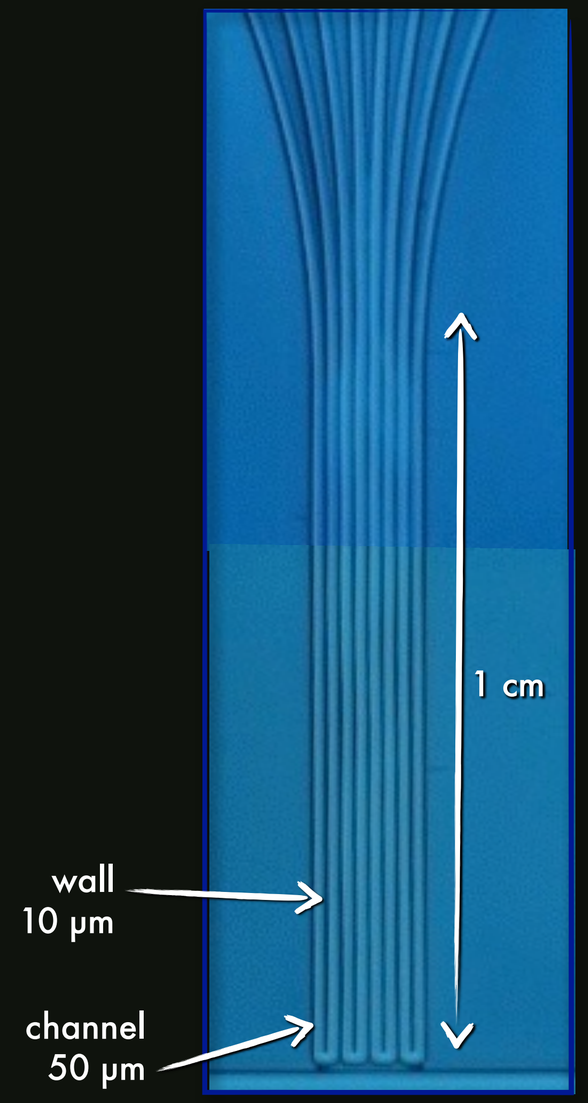
1st microScint protos made of SU-8 photoresist

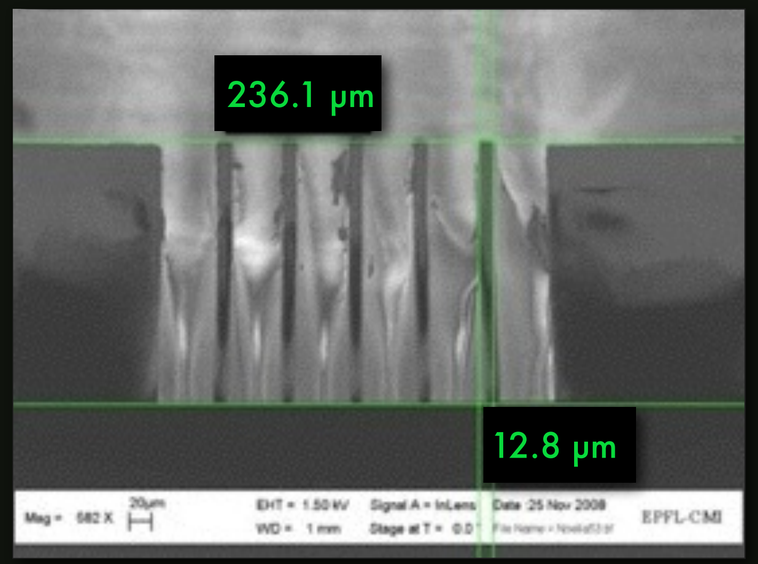
SINGLE PHOTOLITHOGRAPHY STEP TO DEFINE THE CHANNELS
(SURFACE MICROMACHINING)



DICING

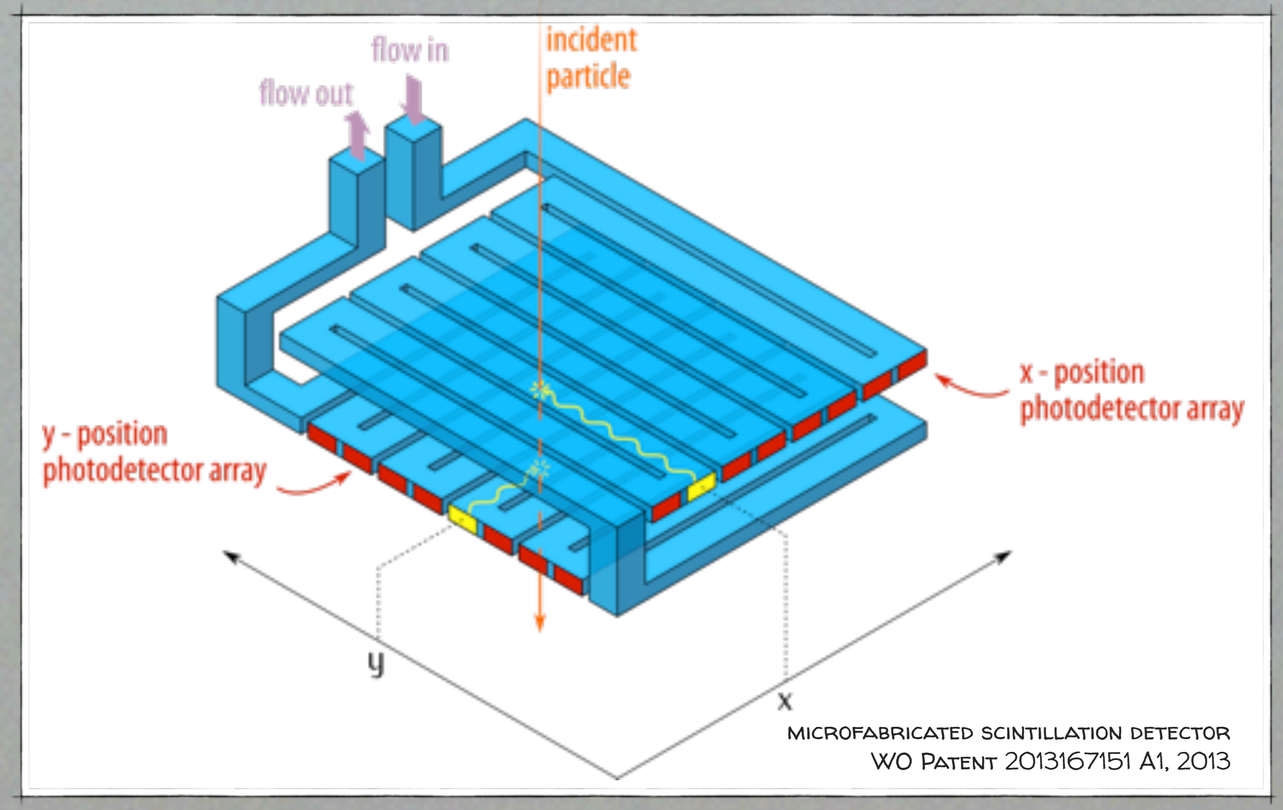

20 mm
15 mm


1 cm
wall
10 µm
channel
50 µm


236.1 µm
12.8 µm
Mag = 582 X
20µm
EHT = 1.50 kV
WD = 1 mm
Signal A = InLens
Stage at T = 0.0
Date :25 Nov 2008
EPFL-CMI

	plastics	microScint SU-8 Au-coat	microScint Silicon Al-coat
scintillator	0.5 mm	0.2 mm	0.18 mm
light yield	4.4 pe 9 pe/mm	1.6 pe 8 pe/mm	1.4 pe 7.8 pe/mm

Y layer 150 μm
0.9 pe
6 pe/mm



X layer 150 μm
1.0 pe
6.7 pe/mm

coming up with microScint

- Double layer (XY) microfluidic device
  - EPFL Microsystems Laboratory (lmis4.epfl.ch)

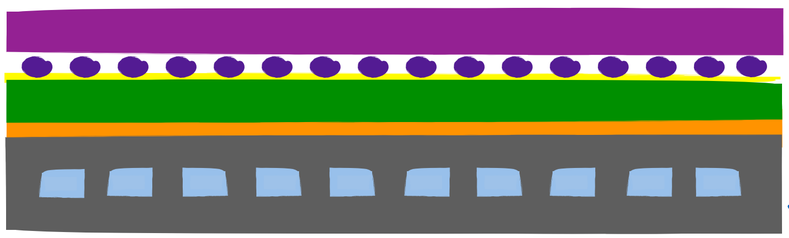
- SiPM readout
  - INFN, Roma

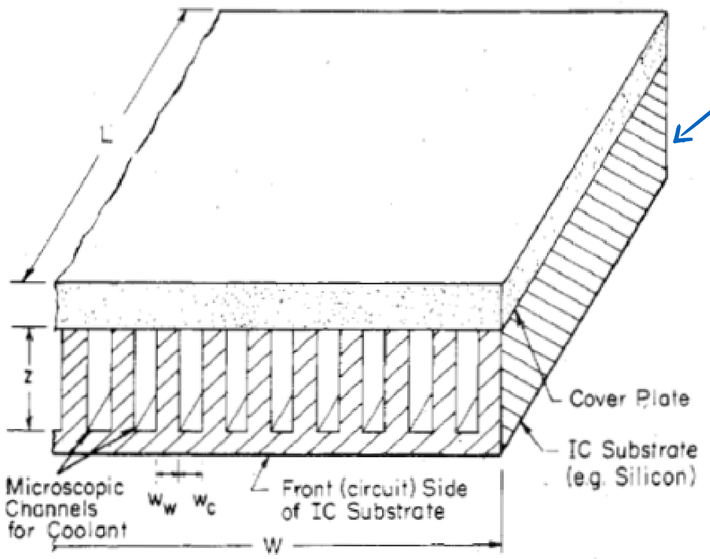
- Integrating aSi:H photodiodes in the microfluidic channels
  - EPFL PVLAB (pvlab.epfl.ch)

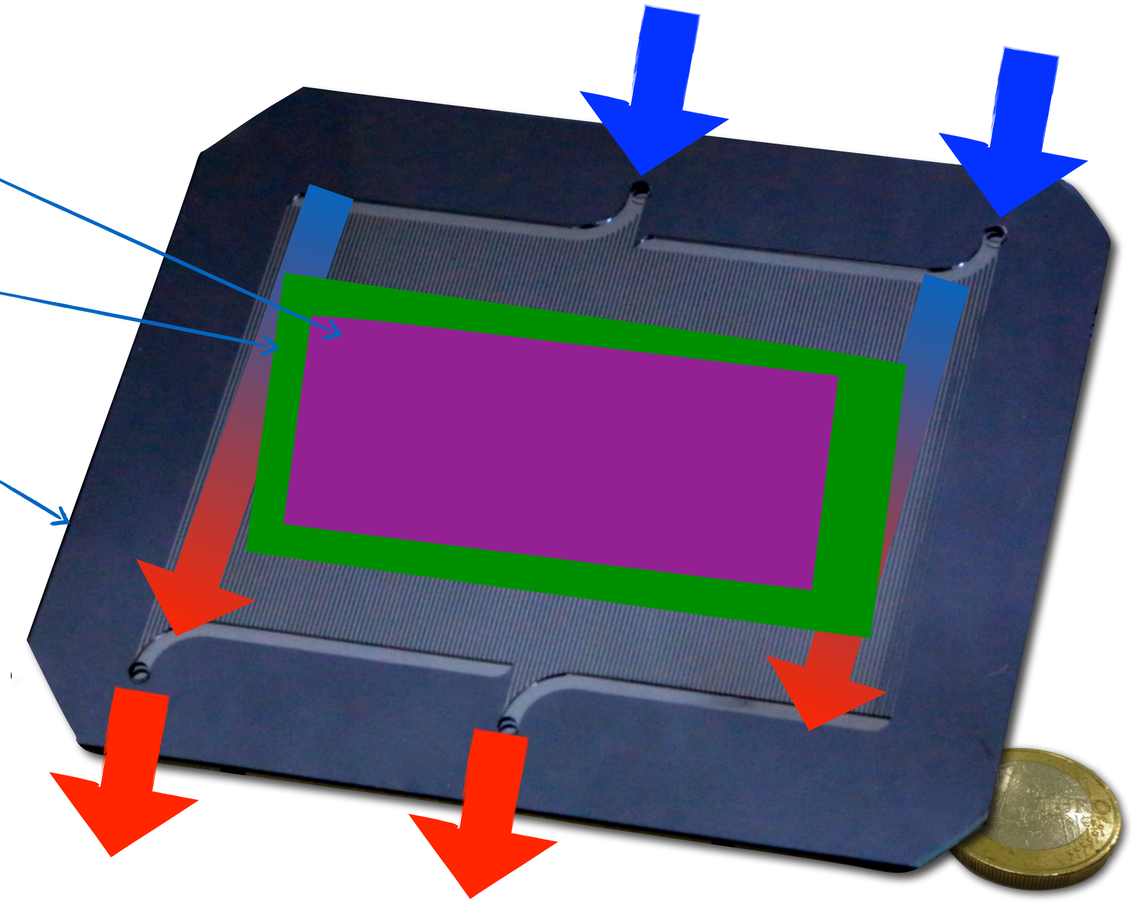
silicon microchannel cooling

- No CTE mismatch
- Low material budget
- Active/distributed cooling
- Integration potential

Great effort required for microfluidic connections in HEP!!



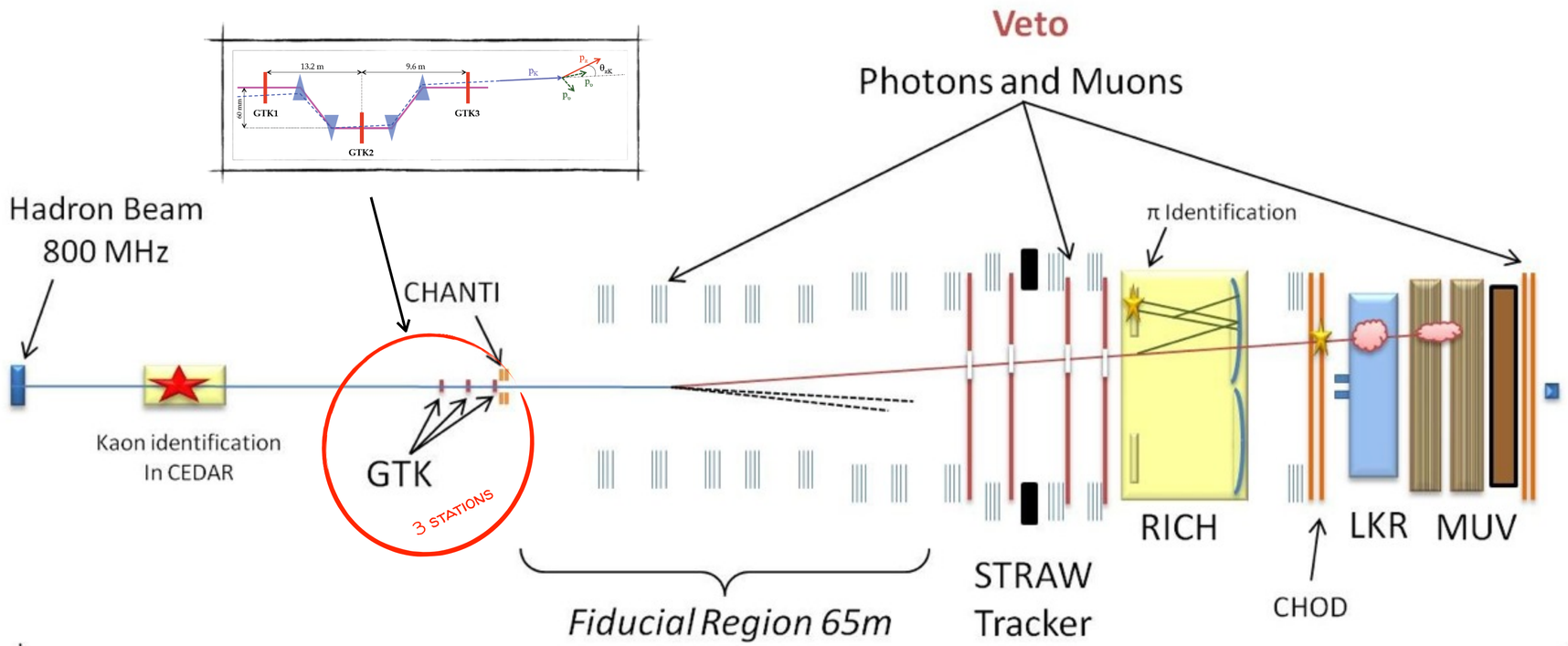




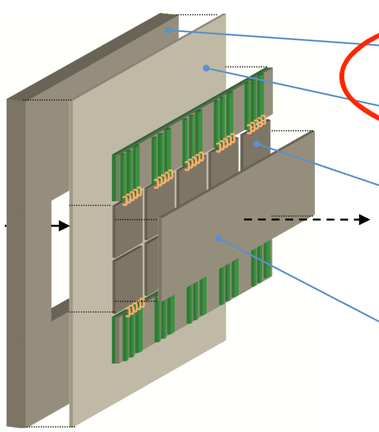
D.B. Tuckerman and R.F.W. Pease, IEEE Elec. Dev. Letters, Vol. 2, 5, 1981

NA62-GTK.. the 1st microCool

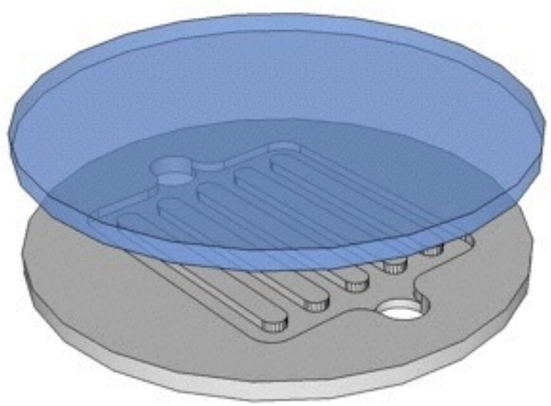
- In October 2014, the Gigatracker pixel detectors will be the first detectors to be cooled with silicon microchannels.
- Liquid C_6F_{14} will circulate at -20°C in a 130 µm thick silicon plate with microchannels (200 µm x 70 µm).



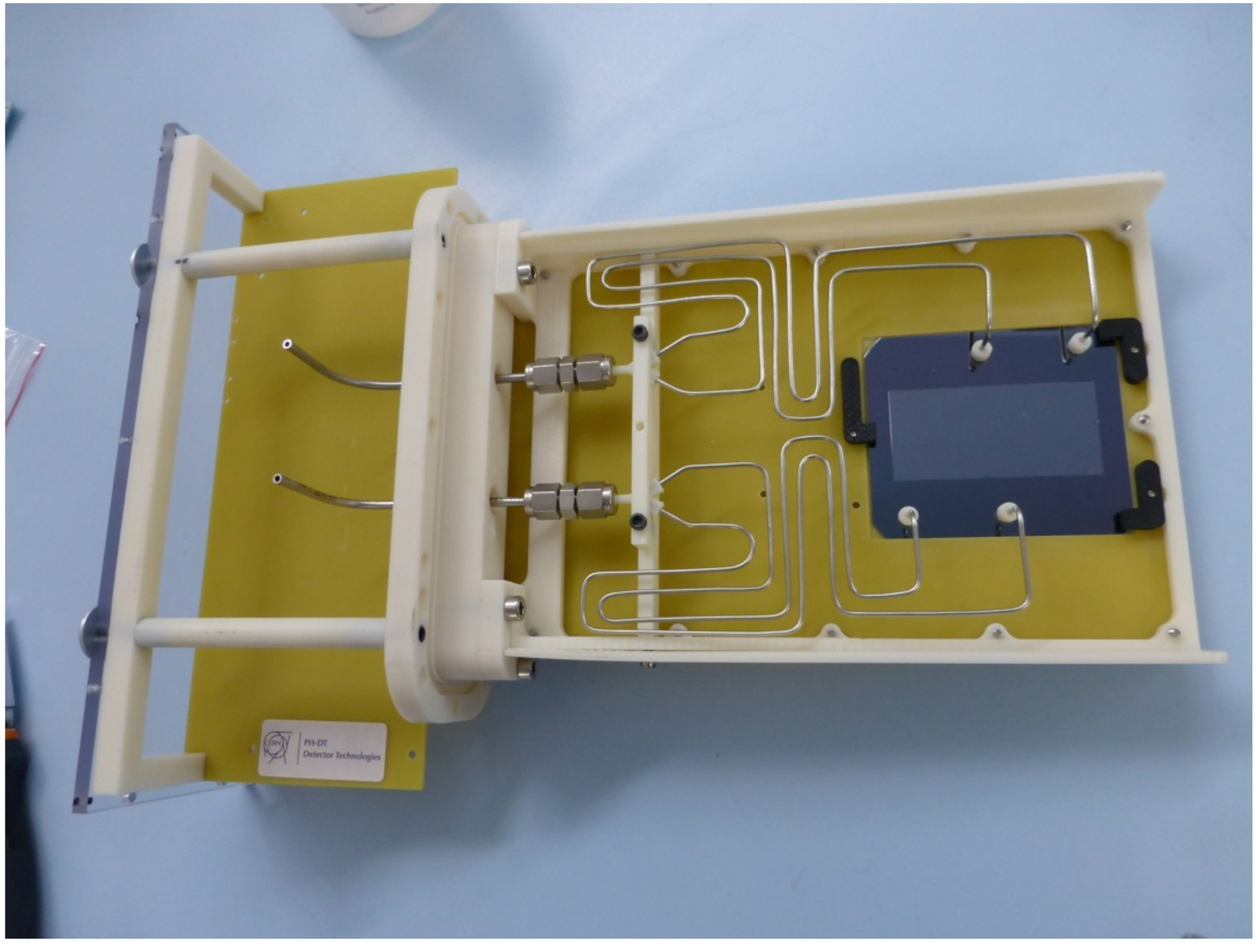
single GTK station

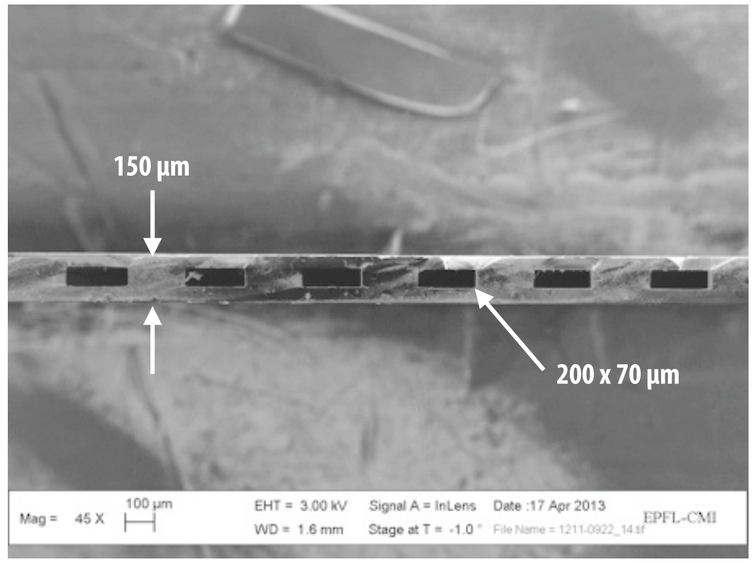


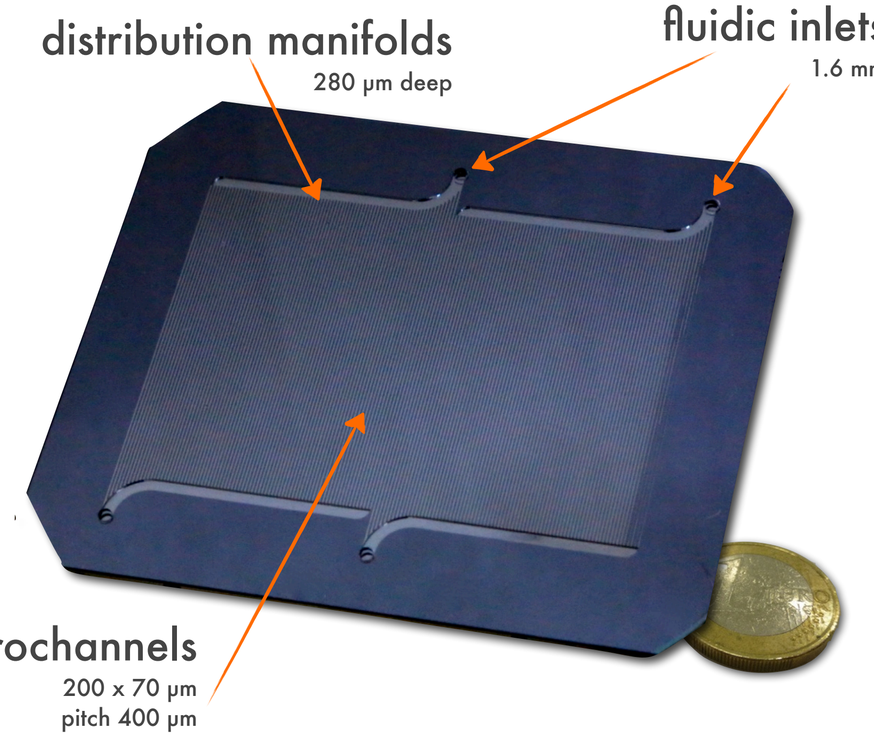
130 µm thick Silicon substrate with microchannels



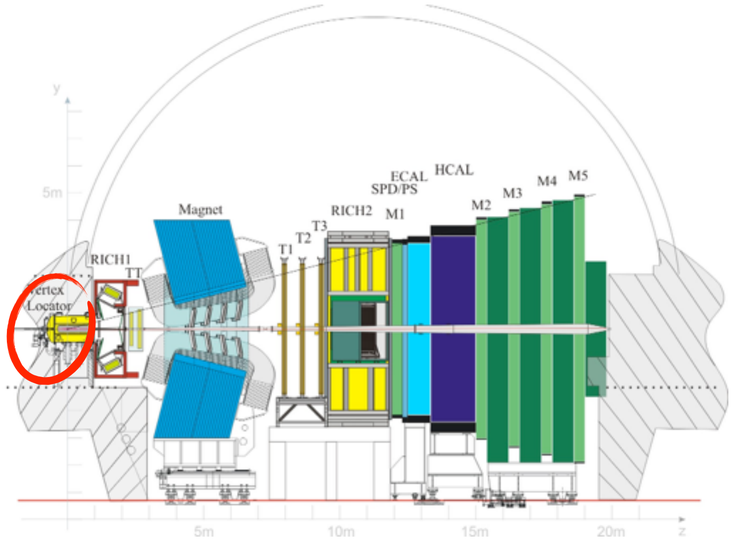
NA62-GTK.. the 1st microCool

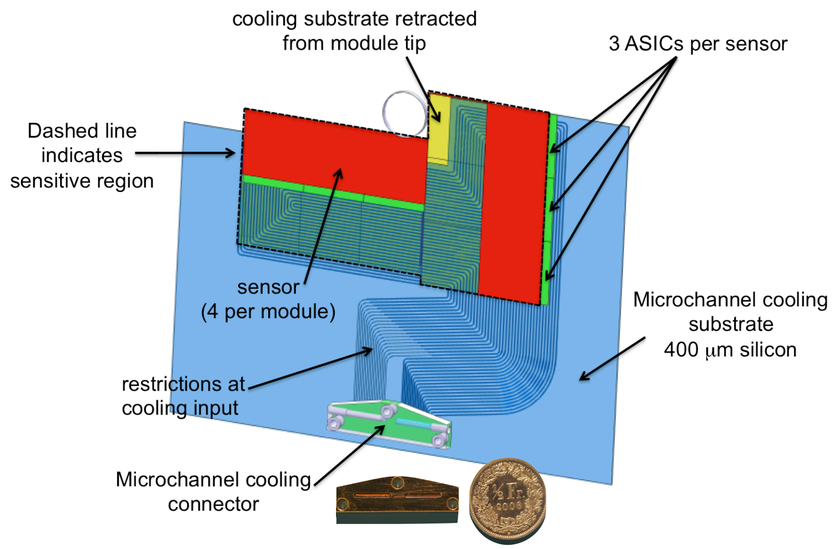


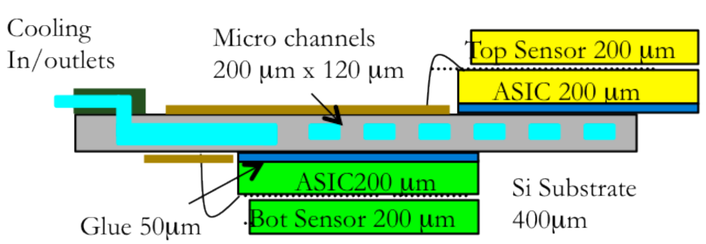


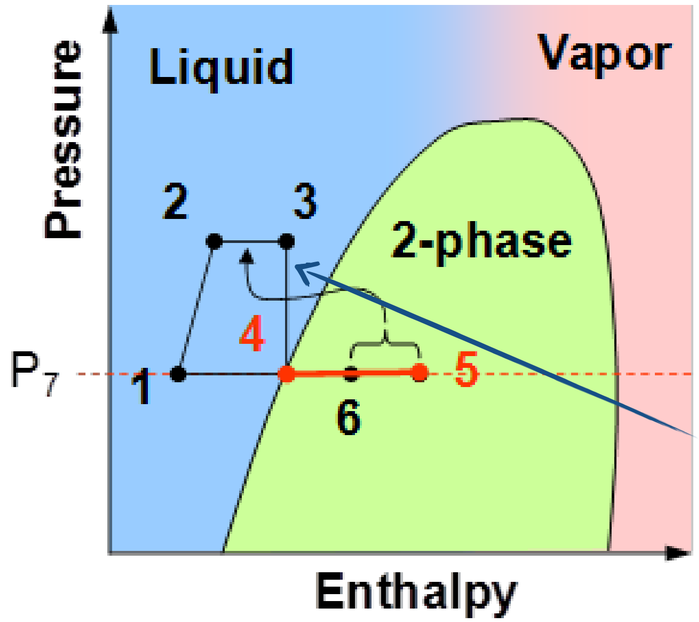


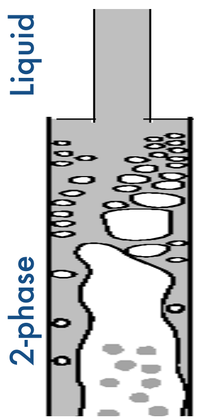
LHCb VeLo Upgrade.. CO_2 in microchannels

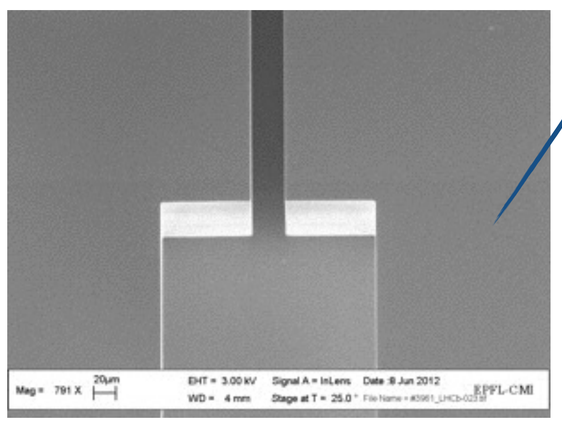






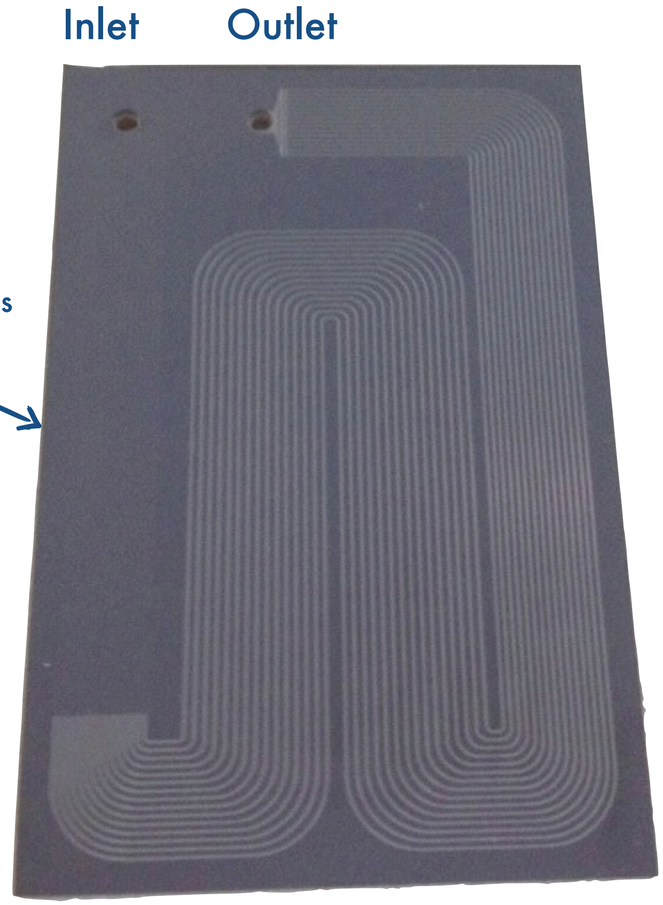






Transition from inlet restrictions to evaporative microchannels

Inlet restrictions 30 x 60 μm

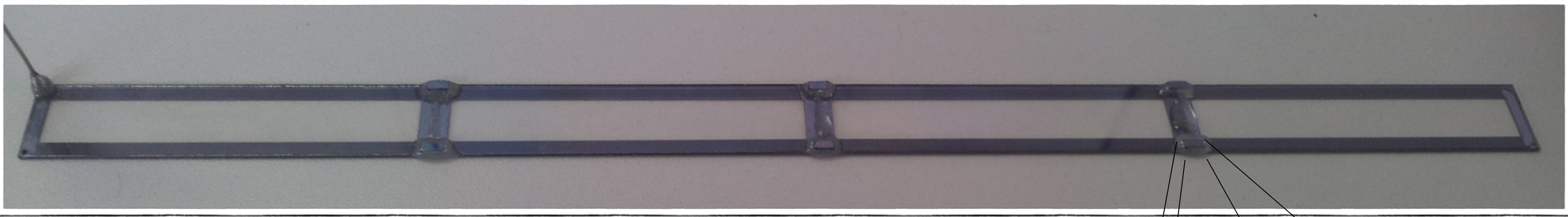


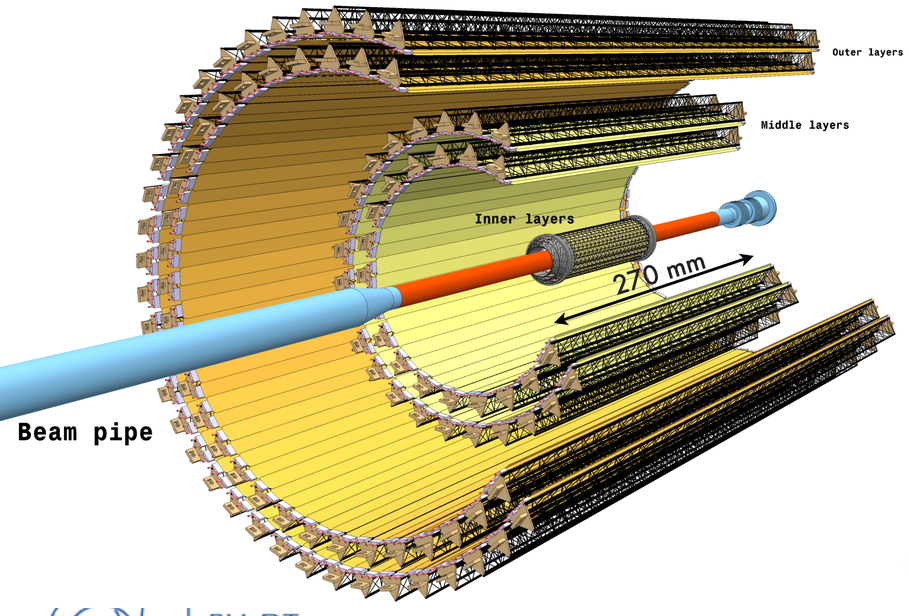
Microchannels 200 x 60 μm

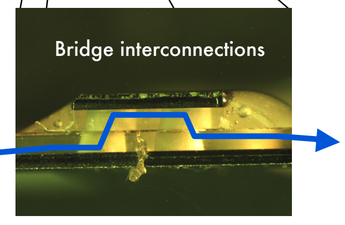
ALICE ITS… towards a microfluidic stave

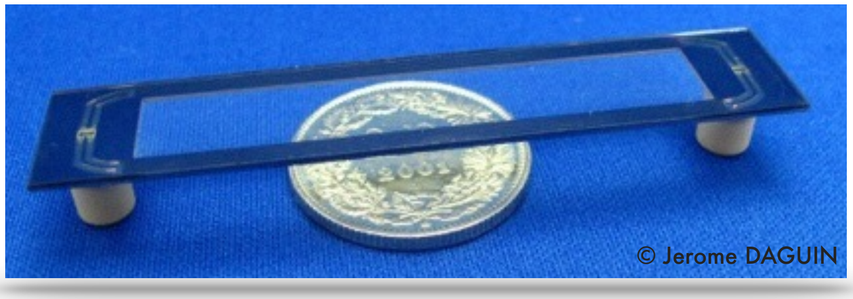
Baseline solution for mechanics and cooling developed by Corrado GARGIULLO *et al.*

270 mm



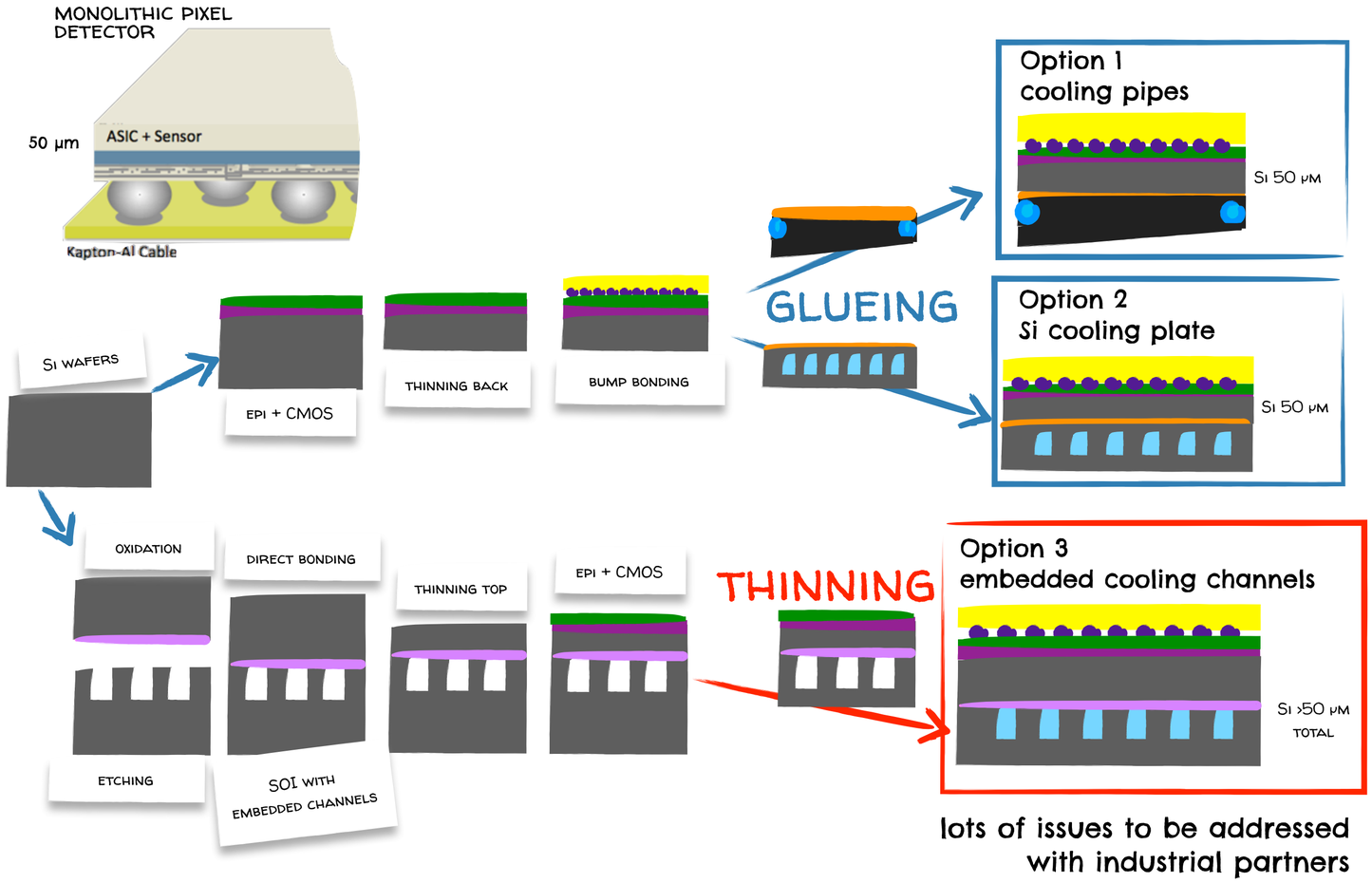






x4 = 270mm

towards integrated microcooling



lots of issues to be addressed with industrial partners

A. Mapelli, L. Musa, P. Petagna, P. Riedler, 2011

How SOI wafers are made

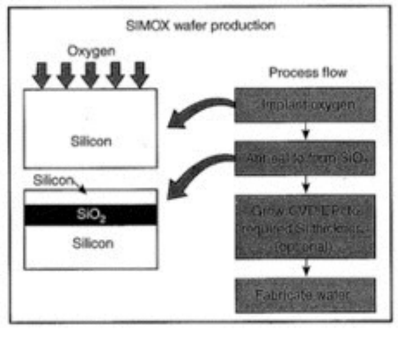
[From P. N. Dunn, *Solid State Technol.*, October, 32–35 (1993). Copyright 1993 PennWell Publishing Company, with permission.]

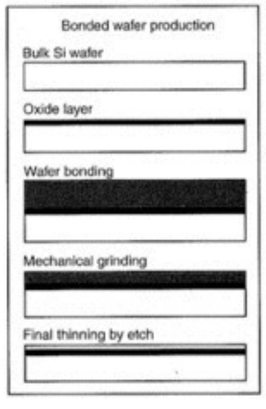
Many different silicon-on-insulator materials have been developed over the years, but two are currently being used for IC production: SIMOX (Separated by IMplanted OXygen) and bonded wafers.

In the SIMOX process, a standard silicon wafer is implanted with oxygen ions and then annealed at high temperatures; the oxygen and silicon combine to form a silicon oxide layer beneath the wafer surface. To minimize wafer damage, the oxygen is sometimes implanted in two or more passes, each followed by an anneal. The oxide layer's thickness and depth are controlled by varying the energy and dose of the implant and the anneal temperature. In some cases, a CVD process is used to deposit additional silicon on the top layer.

The bonded wafer process starts with an oxide layer of the desired thickness (typically 0.25 to 2 microns) being grown on a standard silicon wafer. That wafer is then bonded at high temperatures to another wafer, with the oxide sandwiches between. One of the wafers is then ground to a thickness of a few microns using a mechanical tool.

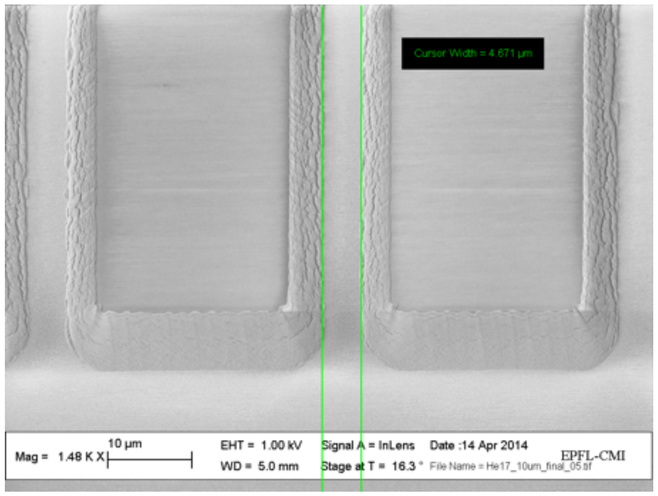
Because advanced devices require an even thinner layer, more silicon must be removed. The wafer may be etched with a confined plasma, between 3 and 30 mm wide, which is stepped across the wafer surface. A film thickness map is made for each wafer and used to compute the dwell time for the plasma etcher at each stop. The process can be repeated for additional precision. Silicon thicknesses of a little as 1000 to 3000 Å, with total thickness variation of 200 Å have been achieved. IBM has also developed an etch-back process for bonded wafers.

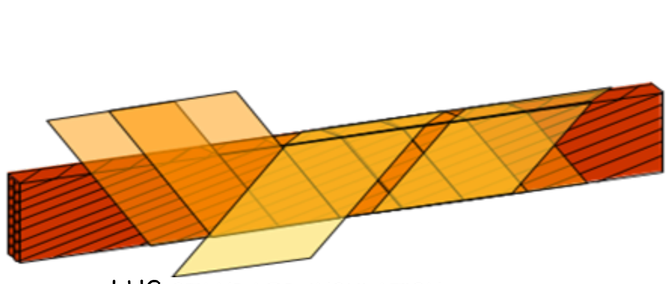




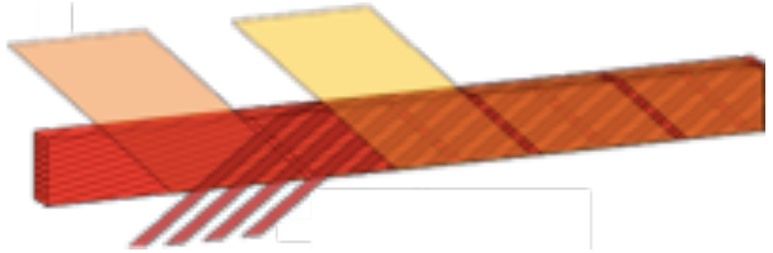
microHeII.. superfluid helium

- study the heat transfer of superfluid Helium-II in glass microchannels
- thermally-enhanced insulation of LHC magnets for future upgrades



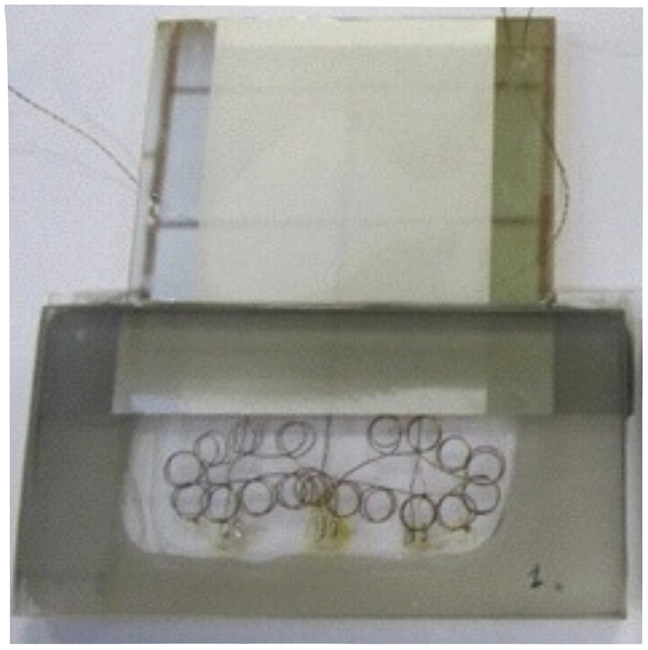


LHC standard insulation



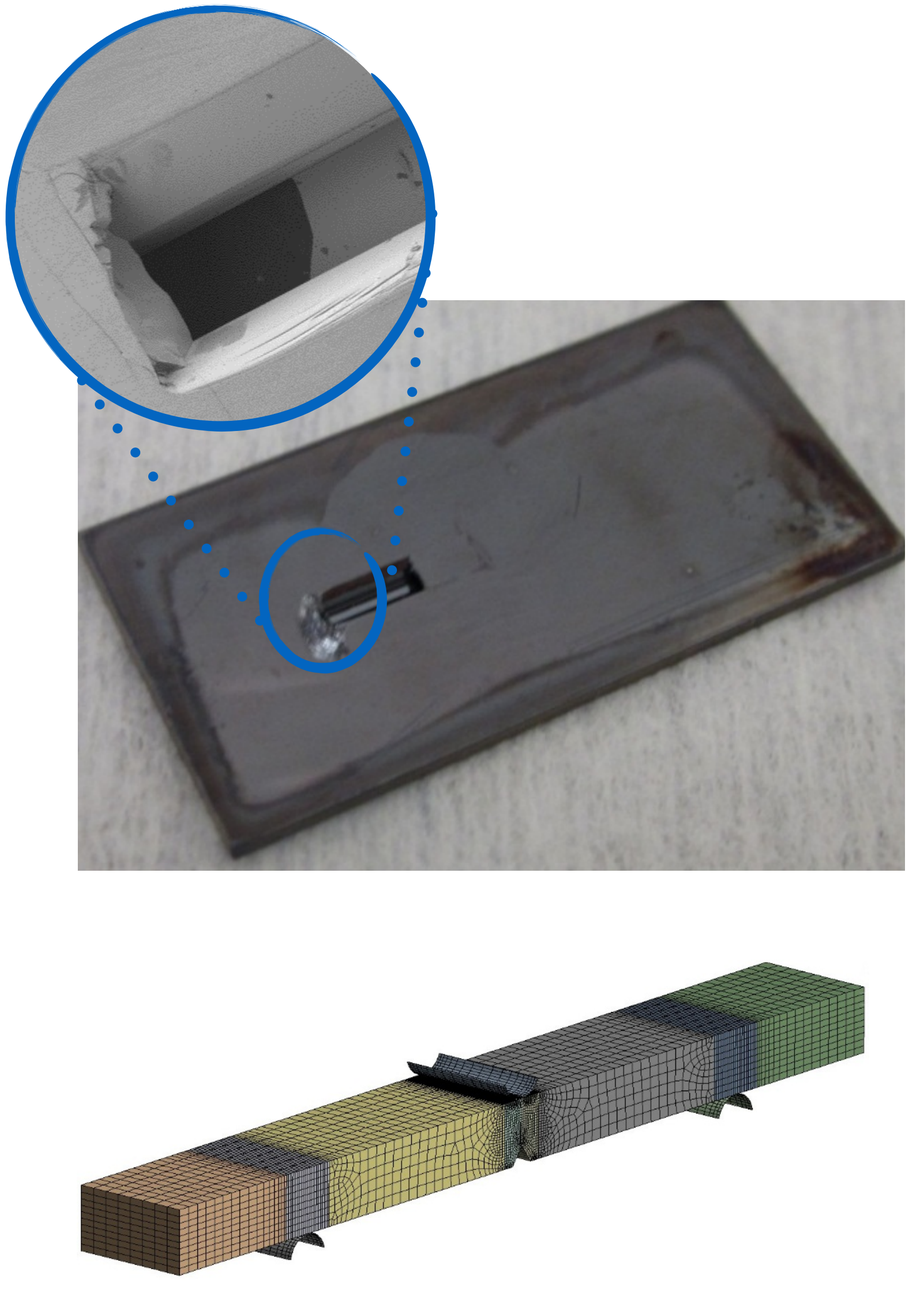
Enhanced insulation for LHC upgrade

Sample	MEMS technique	Number of channels	Characteristic dimensions (µm)	Total Channels Area (mm^2)	Length (mm)
1	Sandblasting	158	$\Phi_{equivalent}$ = 100.4	1.25	55
2	HF etching	172	17.15 x 75.1	0.22	55
3	DRIE etching	1000	~15.8 x 24	0.38	55

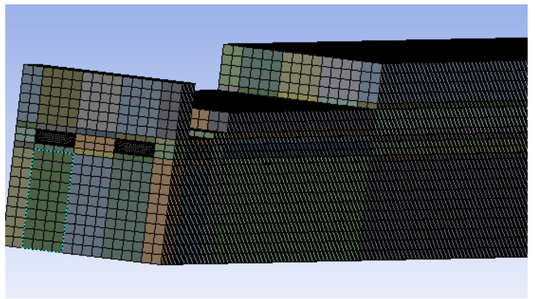


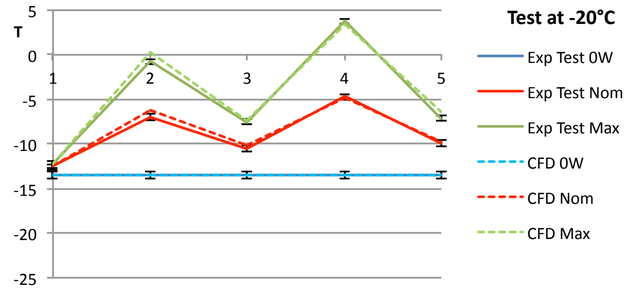
simulations vs experiments

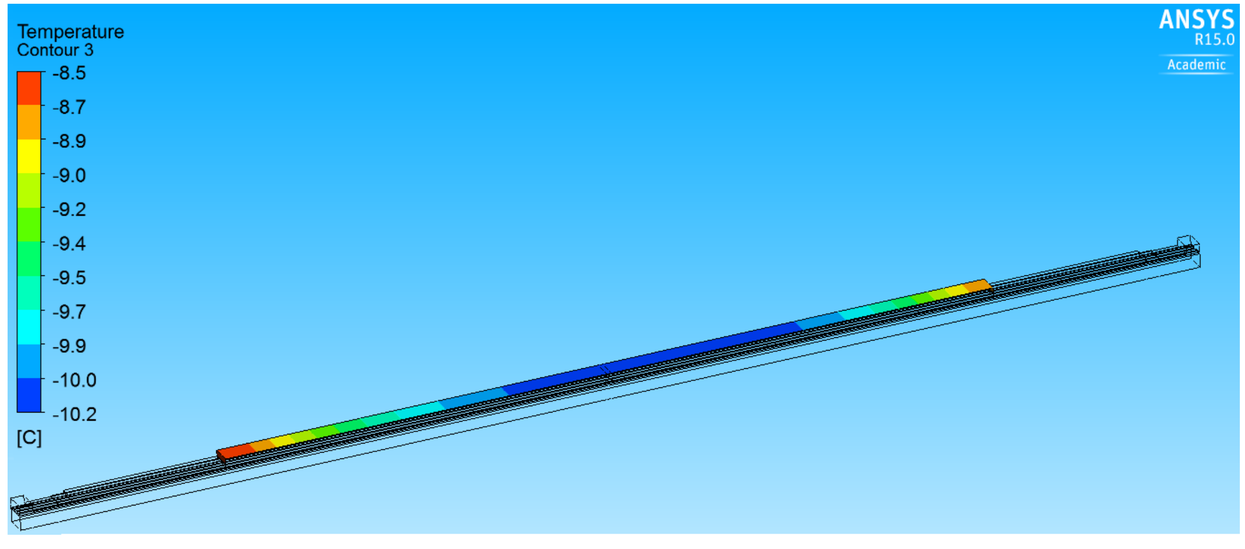
Structural resistance



Thermal Behaviour





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- MEELWORMEN VOOR MEER DAN 50% UIT PROTEINE BESTAAN?
- ONZE LOEMPIA HEEL LEKKER IS
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