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High-speed photon counting readout ASIC for spectral computed tomography detectors

This study is concerned with the simulation and design of a high-speed photon counting readout circuit for spectral computed tomography detectors. We propose a novel front-end architecture aimed at reducing dead time by introducing multi signal paths in each pixel. A prototype chip using 0.18um six-metal standard CMOS process is consisting of 16 x 16 pixels and periphery circuits. Each pixel has 200um pixel pitch and contains two signal paths. Two preamplifiers, eight comparators, three 15-bit counters, switching circuits, and a 30um x 30um input pad are included in a pixel. Each preamplifier has a feedback capacitor and a feedback resistor. We use a transistor as a feedback resistor to control its resistivity. When the preamplifier integrate charge, the gate voltage of the transistor is lower than threshold voltage to have high resistivity. After readout the input current pulse, the transistor is turned on for fast reset. The two preamplifiers are connected to the input pad via the switching circuit respectively. The switching circuit allows only one preamplifier to connect the input pad at a time. After current pulse coming to one amplifier, the switching circuit changes its connection to reduce dead time of a pixel. Each output of the two preamplifiers feed four comparators with different thresholds respectively. These four comparators perform quantization of the preamplifier output amplitude to distinguish incident X-ray photon energy. The chip will be fabricated in June 2014 and post layout simulation results will be presented in TIPP 2014.

Summary

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