AGIPD, The Electronics for a High Speed X-ray Imager at the Eu-XFEL

European XFEL

AGIPD

Peter Göttlicher

DESY HELMHOLTZ ASSOCIATION

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for the AGIPD consortium:

A. Allagholi, J. Becker, L. Bianco, A.Delfs, R. Dinapoli, E. Fretwurst, P. Göttlicher, H. Graafsma, D. Greiffenberg, M. Gronewald, B. Henrich, H. Hirsemann, S. Jack, R. Klanner, A. Klyuev, H. Krüger, A. Marras, D. Mezza, A. Mozzanica, I. Sheviakov, B. Schmitt, J. Schwandt, X. Shi, U. Trunk, Q. Xia, J. Zhang, M. Zimmer

universitätbonn DESY PAUL SCHERRER INSTITUT PSI UHH

Outline

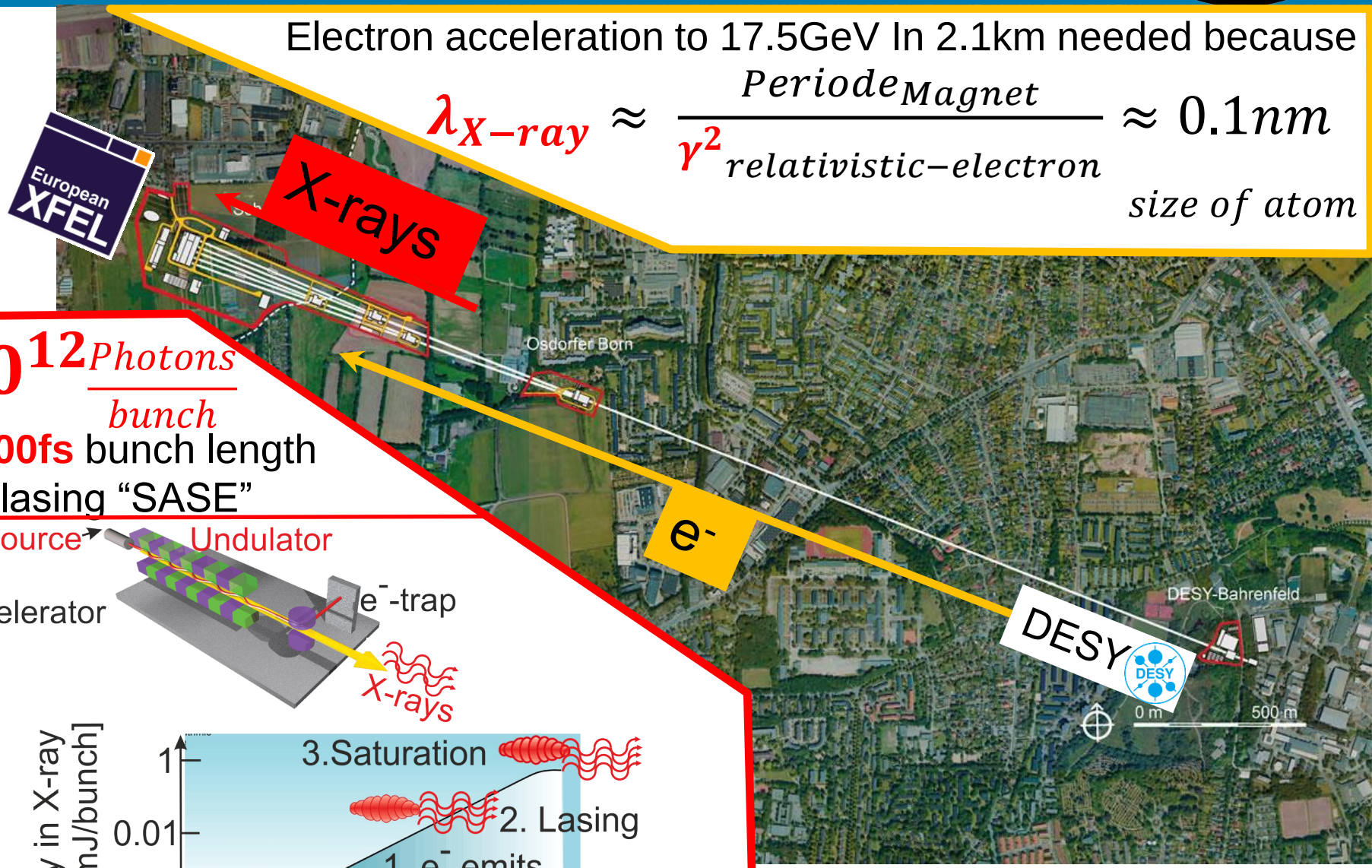
- Introduction: Free Electron Laser and its experiments
- Concepts for AGIPD
- **Functional block of the electronics**
- **System aspects and logic realization**
- Off-Detector-Head data handling
- First Measurements
- Summary and Outlook

Introduction: Free Electron Lasers (Eu-XFEL)

Electron acceleration to 17.5GeV In 2.1km needed because

$$\lambda_{X-ray} \approx \frac{Periode_{Magnet}}{\gamma^2_{relativistic-electron}} \approx 0.1nm$$

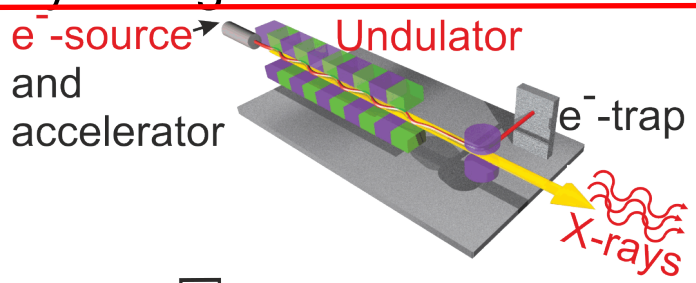
size of atom

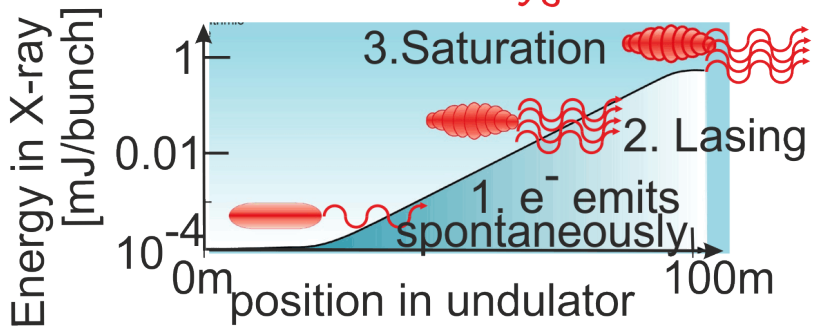


$10^{12} \frac{Photons}{bunch}$

<100fs bunch length

by lasing "SASE"

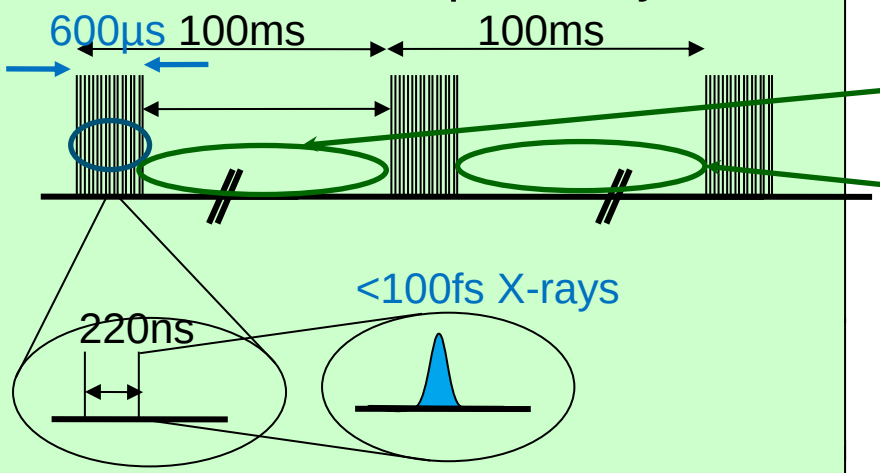




Introduction: Experiments at Eu-XFEL

Accelerator X-rays as trains

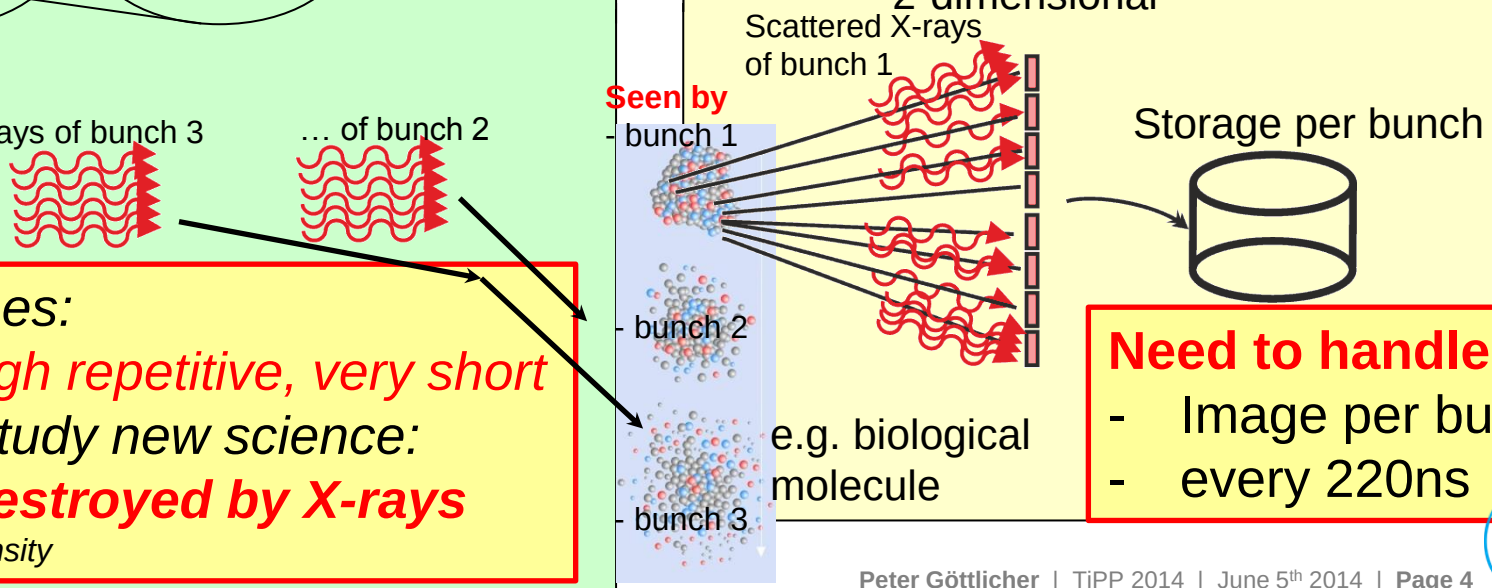
- 27000 bunches/sec
- 2700 bunches spaced by 220ns



Experiment:

- 222ns time to catch each image
- 600µs with 2700 scatterings
- 99.4ms time to process signals
- 99.4ms time to transfer data out of detector – and pipelined process the signals of next train

Imaging detector:
- 2-dimensional



X-ray flashes:
Intense, high repetitive, very short
allows to study new science:
Objects destroyed by X-rays
– even small intensity

Need to handle

- Image per bunch
- every 220ns

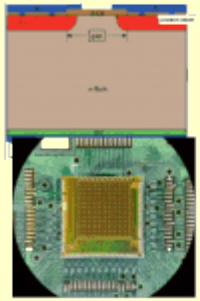
Concept: Signal Chain for a 2-dimensional Camera

AGIPD aims for recording images with:

- 1 Mega Pixel: 1024 ×1024
- 12.4 keV X-ray with efficiency>90%
- 200 µm pixel-size (square)
- Active detector area: 20×20 cm^2
- Identifying individual photons
- Dynamic up to 15 000 with resolution better than Poisson statistics $\sigma < \sqrt{n_{Photons}}$
- Radiation hard: 1GGy at sensor surface
- Catch 352 Images from the 2700 bunches
- Select best images

System has to deal with no data compression

- Nearly all pixels have signal in each image
- Information in different details for different science and usage
- Stored signal-rate 3.7 Giga-Signals/second
- Data-rate at output: 60 Gbit/second



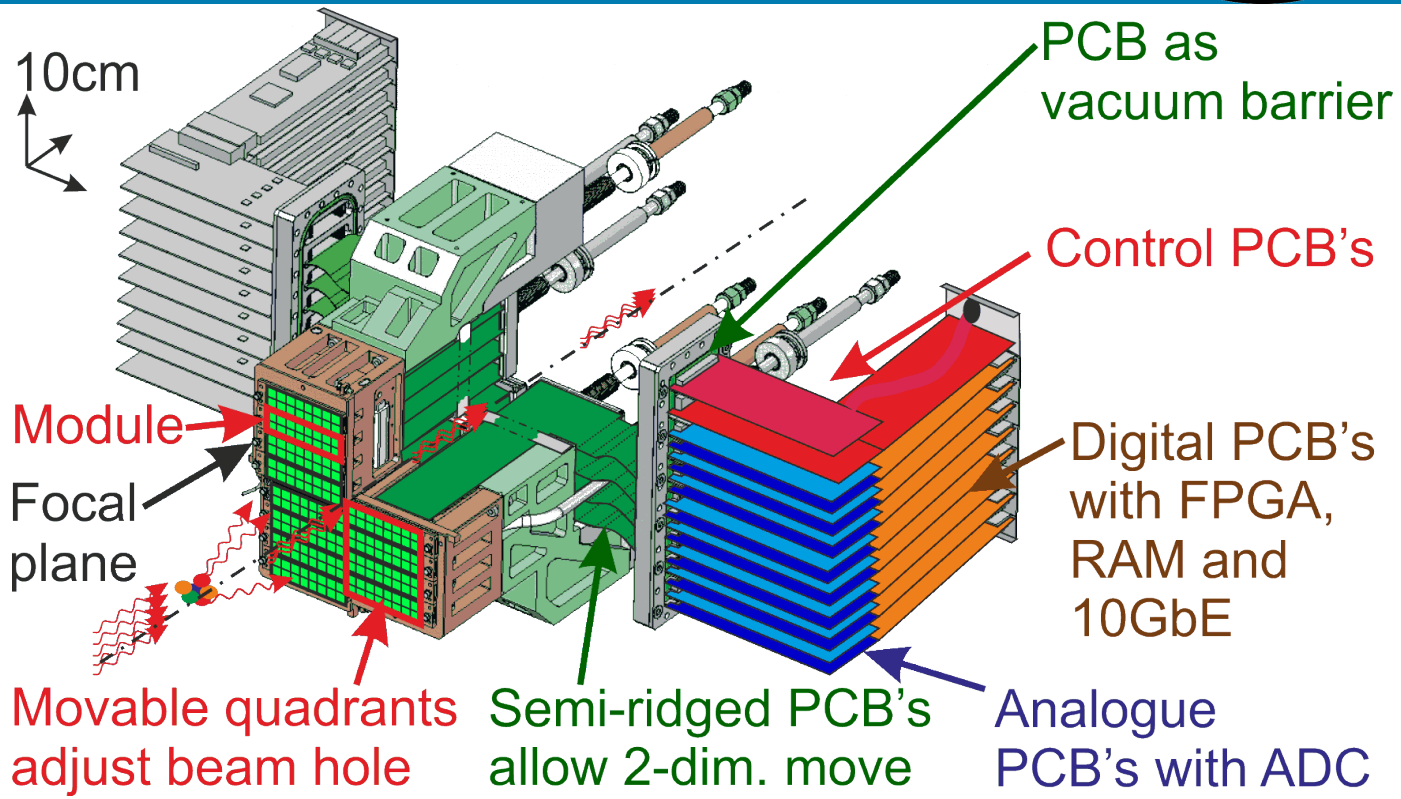
- Silicon sensor
- ASIC for signal preparation, storage and multiplexing

- Analogue PCB for digitizing

- Digital PCB for digital preprocessing, storage and multiplexing to 10GbE

- Off-detector data processing and storage

Concept: Mechanical for a 2-dimensional Camera

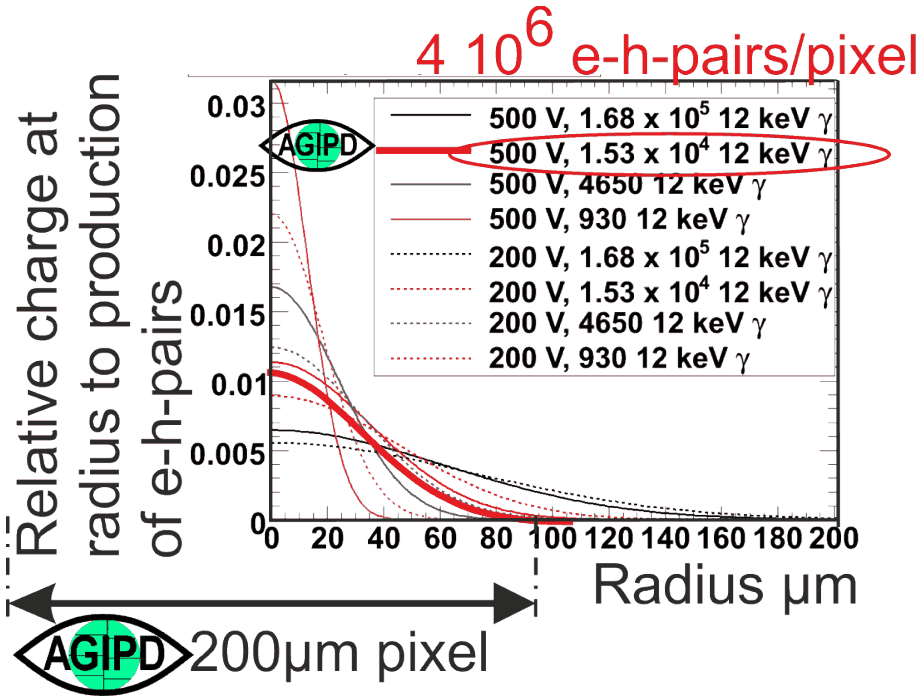


- Focal plane in probe-vacuum cooled to ~ -15-20^{0}C
- Focal plane sticking close to probe through flange

- Electronics as wings to the side allows down-stream small angle detectors
- PCB electronics: Closed-loop air cooled outside vacuum
- Thick Multilayer-PCB as vacuum barrier with plugged and micro-vias
- Interfaces always limited by number of contacts in connectors

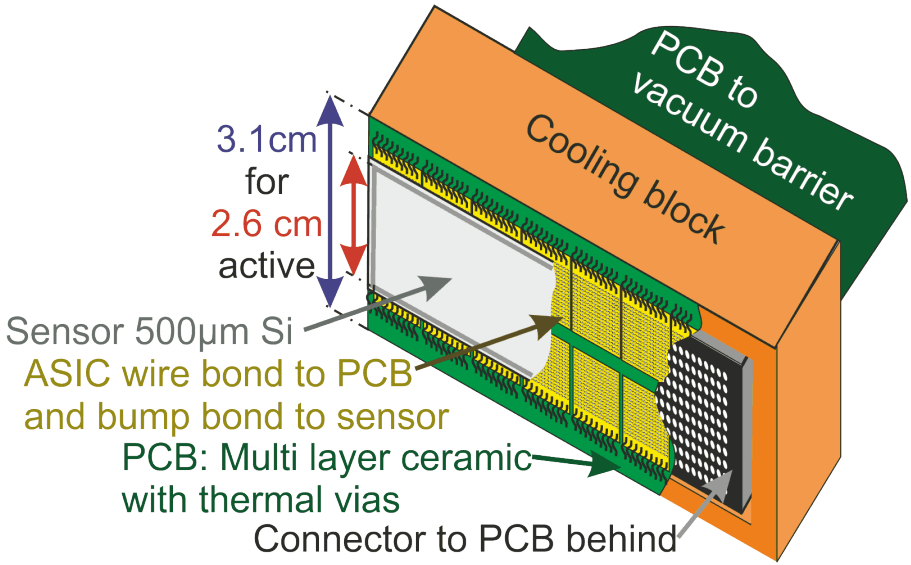
Sensor design and operation point

- Keep the charge within pixel, even for intense pulses
- Modularity: 512×128 pixel and 16 modules to get 1Mega-Pixel

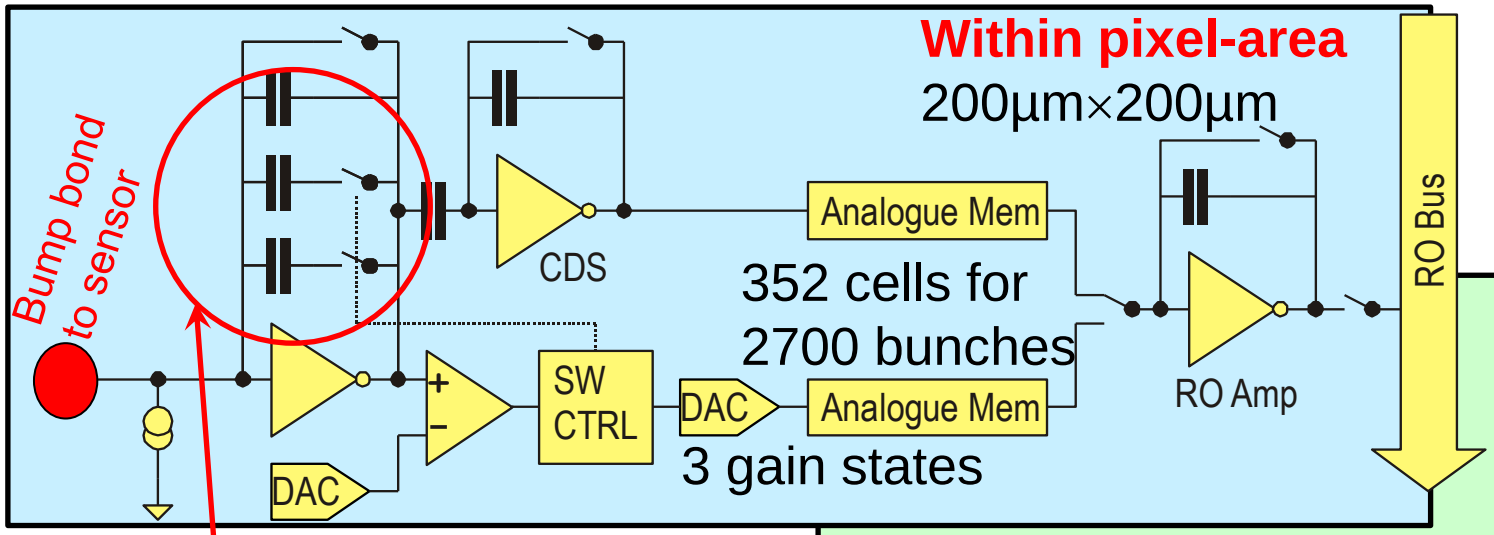


Focal Plane:

- **8×2 ASIC's** for each sensor
- **Pixel electronics** behind each pixel within 200µm ×200µm and than multiplexed to fit with
- **Dense connector** 500 pins share space with
- **Cooling interface**



Functional Block: Functionality of the ASIC



Common for ASIC:
64 x 64 pixels
4.5M-bunches/s

Dynamic switching of the gain per image at threshold in the integrating input amplifier

Dynamics: X-rays/pixel/image
Single X-ray identifying up to 15000

Command Interface with 16 bit/bunch
- 3 LVDS (clock, data, strobe=bunch-start)
- Random write/read access to analogue memory
- Control of settings and readout

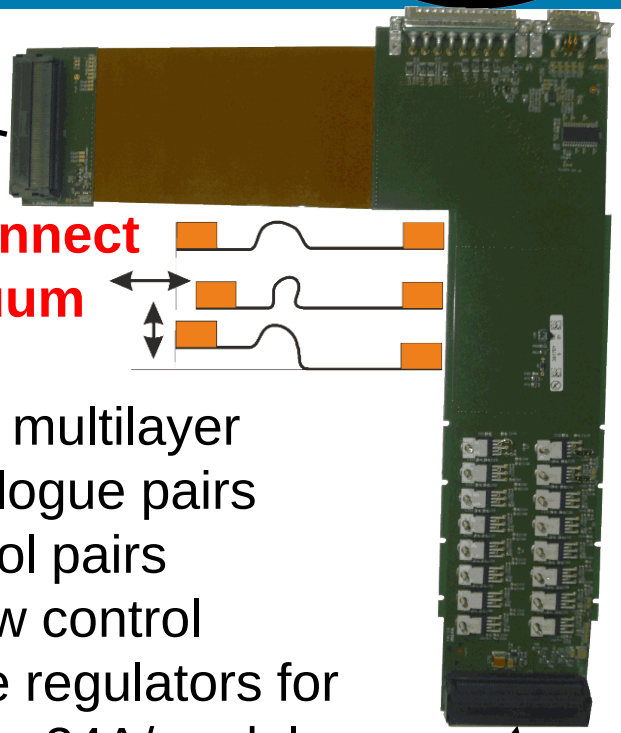
Output driver: 4 differential analogue
- into 100Ω-lines with 33MS/s
- Common usage for analogue + gain
- Each for 64x16 pixels

Adaptive Gain Integrating Pixel Detector

Functional Block: Interconnecting PCB's

3. Backplane for ½ Mega Pixel as vacuum barrier

- 512 analogue feed trough's
- 48 digital controls for time synchronic operation
- Slow control I^2C branched network
- Vacuum tide: Multilayer with copper-GND and plugged/micro-vias



2. Interconnect to vacuum barrier

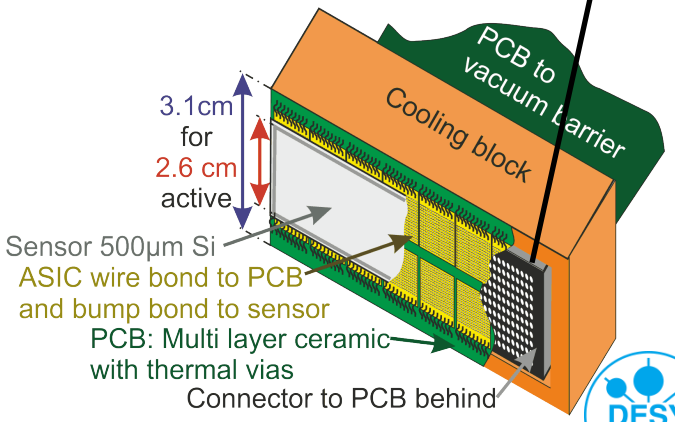
Semi rigid multilayer

- 64 analogue pairs
- 3 control pairs
- I^2C slow control
- Voltage regulators for ASICs: ~24A/module

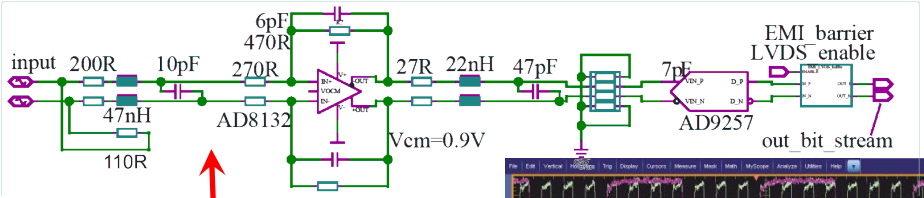
1. Dense interconnect

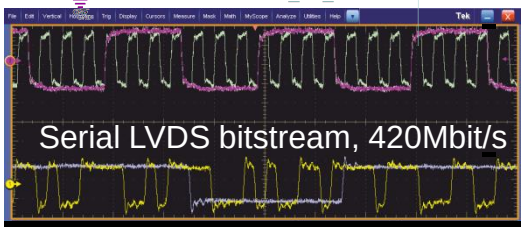
from wire bonded ASICs to 500 pin connector:

- PCB out of ceramic (LTCC)
- Multilayer
- Thermal and micro-vias
- Ceramic capacitors for power/bias

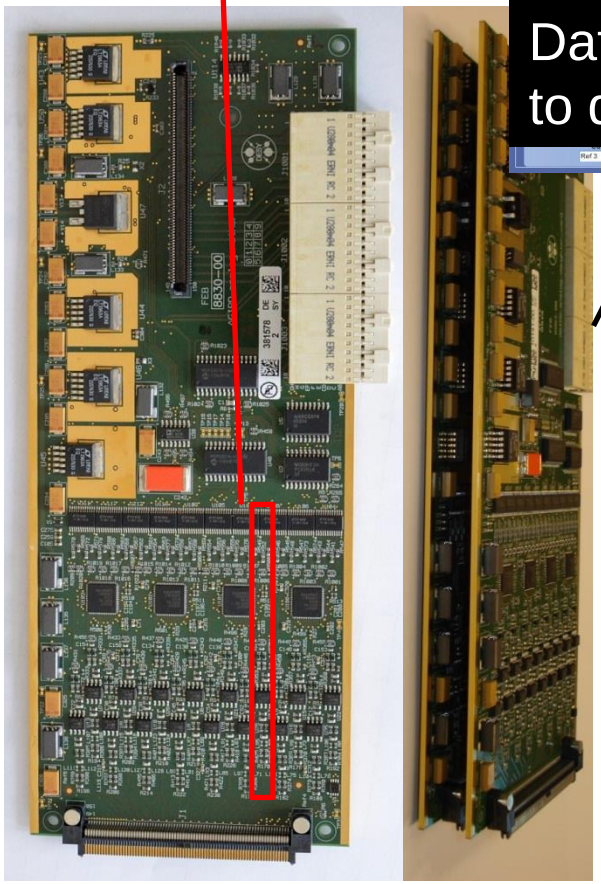


Functional Block: Analogue Signal Chain



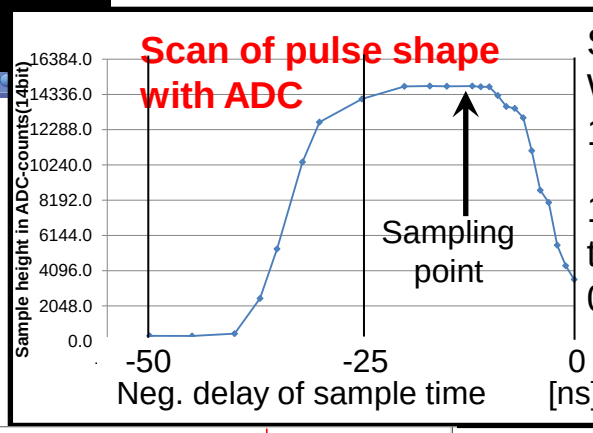


Data transfer to digital board



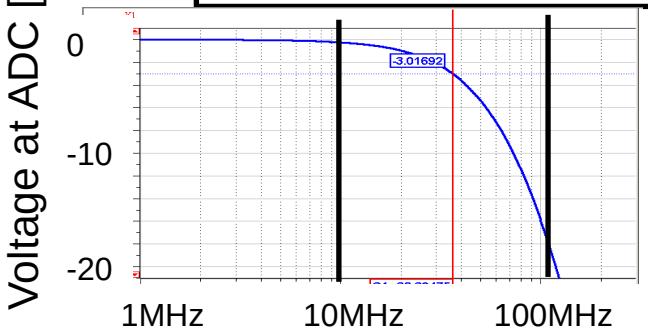
64 channel as 2 PCB's each 2 sides:
Minimal components/channel:

- Differential noise filter to sample rate within 8mm of PCB-side
- Multichannel 14-bit ADC's with serial output stream: 33MS/s
- 64 x 465Mbit/s to digital part



Settling to 11 bits
While full scale is just 128 X-rays full scale

14-bit ADC allows to calibrate 0,1,2 X-rays as peaks



Frequency response of the filter (simulated)

-3dB @ 36MHz

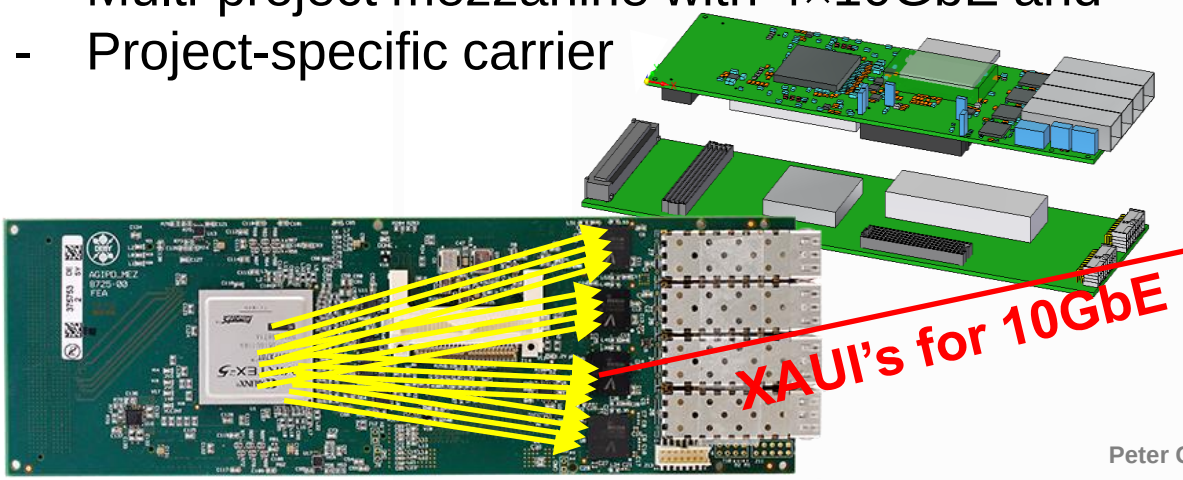
Functional Block: Digital Processing

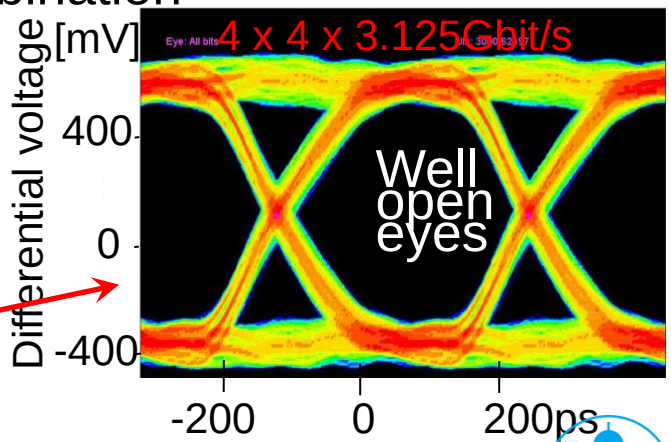
Need is 64 ADC inputs with design goal per **one of 16 modules**

- 50MS/s with 14bit or 700Mbit/s/channel In: 45Gbit/s
- Gain sampling: Reducing 14bit to 2 bits for 3 states
  Forth 2 bit code allow to transfer debug information for uncertain decoding
- Output word for pixel and image: 16 BIT: 14bit for analog + 2 for gain
- Sorting data to small geometrical pattern needs write/read to memory:
  SODIMM 128 I/O's, >250MHz-DDR Memory: 55Gbit/s
- Formatting to 10GbE
- Data stream to Off-detector through whole following train Out: 3.7Gbit/s
  for 1×10GbE optical Link with UDP as protocol

Realized around Virtex-5 as central FPGA as combination

- Multi-project mezzanine with 4×10GbE and
- Project-specific carrier

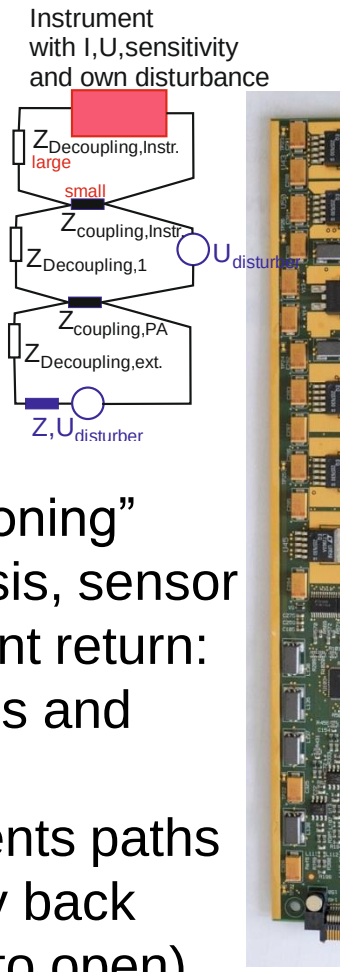


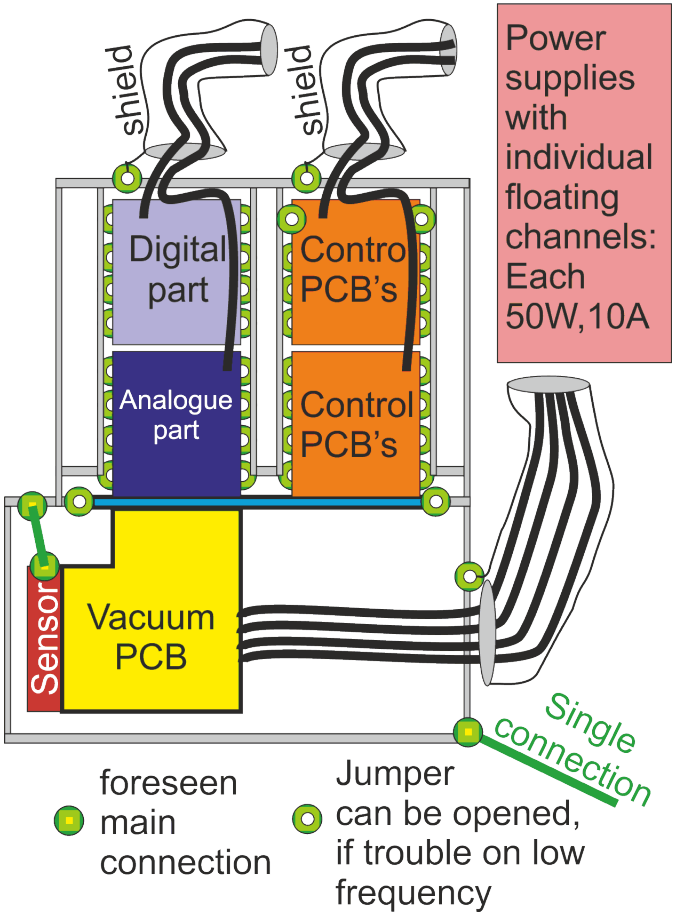


System: Grounding/EMI for a high Current Camera

AGIPD deals with

- 600A current consumption
- 14 bit ADC's
- Signal transfers on geometrical scale of PCB's
- Frequency is open: DC-33MHz





Techniques for handling

- Single point GND to external "zoning"
- Internal: Most sensitive to chassis, sensor
- Minimal usage of GND as current return:
  Floating, low ripple supplies and connection at usage
- Ferrite to block unflavored currents paths
- Guiding induced currents locally back to chassis (default, option to open)

- Differential signals from ASIC to FPGA
- I^2C, single ended, but slow: minimal allowed edge: >20ns
  SPI with LVDS or quite while data taking

System: Numbering and Selecting best Scatterings

Accelerator defines unique numbers for bunch

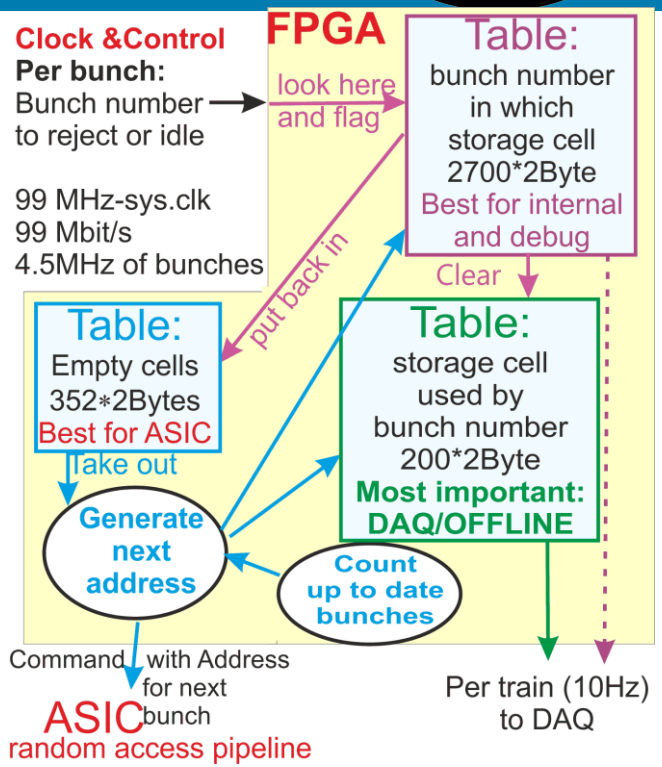
Is scattering expected to be good?

Experiments and accelerator get fast sensors like

- Scattering generates fluorescence light
- currents, monitor losses, intensities, ….

The beam hutch infrastructure sends telegrams with 22 bits per bunch to detector head:

- Can contain the number of **any bad old bunch**



AGIPD

- Records every bunch until memory is full
  - 352 memory cells but 2700 bunches
  - Random access analogue memory within ASIC
- With external information the cell is declared free
- Book keeping with three table allow easy
  - Cell definition for ASIC-write from table of free cells,
  - Function bunch-nr(memory-cell) for offline and
  - Function “memory-cell+status”(bunch-number) as full information for interpretation of telegrams and full history for debug

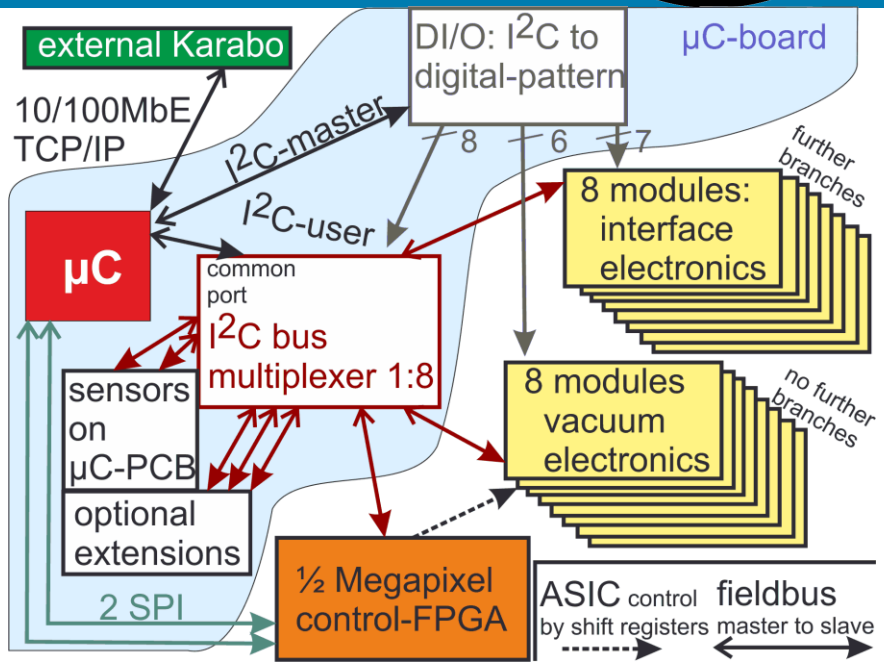
System: Slow Control within Detector-head

Constrains:

- Micro-controller have few I²C-buses
- AGIPD has many identical modules
- Each module has identical devices with no external address-modifier

Method to overcome

- Use two I²C of micro-controller
- Use one as master for control, which sets final branch to address
- Send command to device



That can be repeated on a PCB itself without having there two I²C-buses

"branched I²C network"

Benefits, which appears with it

- Total length to drive is shorter
- Independent developments with full range of addresses
- Multiple usage of same chips easing the programming and purchase, no limit on I/O-channel

Price: Programming effort, few lines through system, slow control

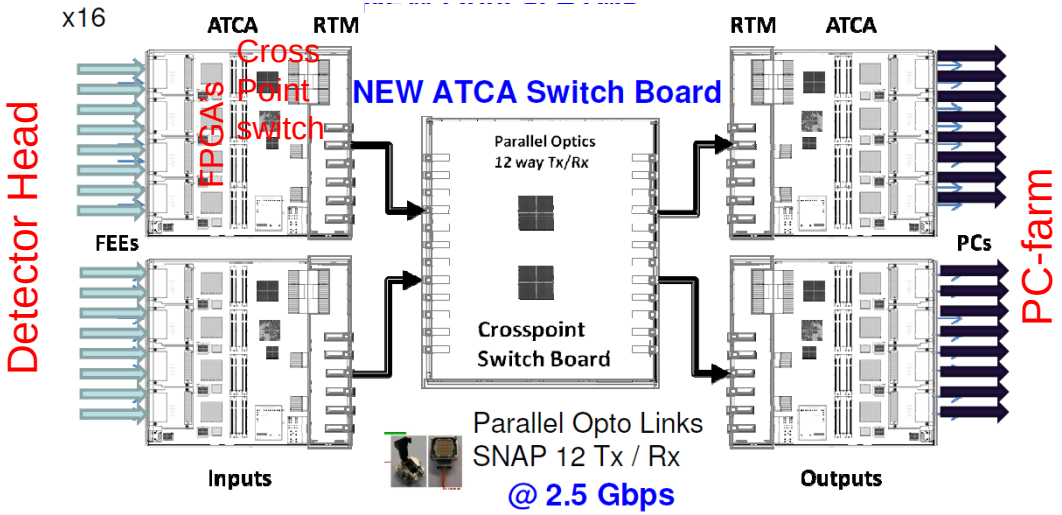
Off-Detector-head Data Handling

DAQ-System is developed for all experiments at Eu-XFEL

1. FPGA housed in ATCA process the data
   "Train builder"
2. Transfer into PC farm with 10GbE, TCP/IP
3. Processing, disk-storage by a PC-farm

Train builder in ATCA

J.Coughlan at TWEPP 2012



Actions:

- Frontend "FEE" delivers on 16 links (10GbE, UPD) fractions of the images
- Train builder sorts from each group of 8 links the data to ½-images and orders pixels according to geometry with FPGA's and cross point switches
- Train builder sorts with next cross point switch to full images and trains
- All data are sent to a PC farm (>80Gbit/s)

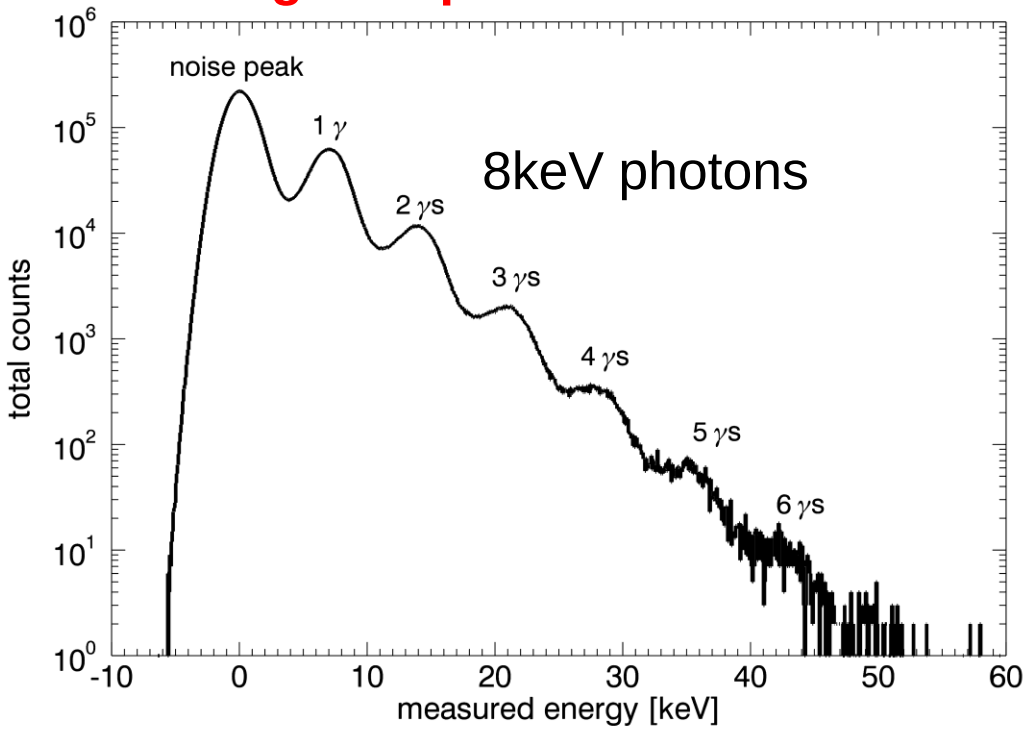
No information loss by compression is allowed

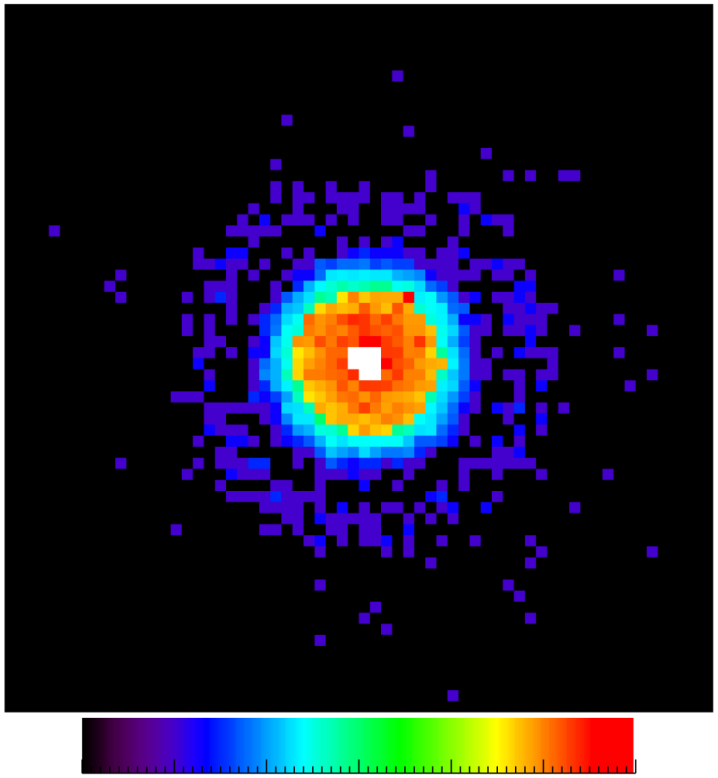
Pure compression has low effect for general science,

may be for given users after experience

First Data

Data to single chip 64 ×64 Pixels in direct beam of PETRA-III @ DESY





First tests at PETRA shows

- Single photons even for 8keV, specifications for 12keV.
- Full dynamic range is recorded

This week: Full module test with electronics-chain at APS (512×128 pixel)

Summary and Outlook

- A **new field of science** opens with intense X-ray sources: FEL's
  e.g. diffraction of X-rays can be used to study objects,
  which gets destroyed by X-rays.
- Need of dedicated detector developments to handle speed and rates
- Technology overlap with other fields of large scale instrumentation

- **AGIPD** will be a camera with 1Mega-Pixel and 4.5MHz image recording
- Electronics for signal-chain fully designed and test in blocks
  Dedicated control boards in progress
- Single full scale chip tests are done
- A module test is just in progress

Next:

- System integration to full 1Mega-Pixel to be done
- Open to integrate test results into electronics for next generation
- Firmware development ready for operation of signal-chain
  Evolving process
- EU-XFEL will deliver first beams in 2016 and first user operation in 2017