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## Development of a Data Acquisition System for the Belle II Silicon Vertex Detector

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The Silicon Vertex Detector (SVD) is one of the main detectors in the Belle II experiment (KEK, Japan) which takes essential roles in the decay-vertex determination, low-energy-track reconstruction, and background rejection. The SVD consists of four layers of Double-sided Silicon Strip Detectors (DSSD) and is being developed toward the start of the Belle II experiment in 2016.

Due to more than 220,000 strips in the whole SVD and the Belle II maximum trigger rate of 30 kHz, the integration of a large number of readout channels and the reduction of data size are challenging issues on the development of the SVD readout electronics. APV25 chips are employed to read the DSSD signals, and Flash-ADC (FADC) boards digitize and decode the outputs of the APV25s. To increase the integration density of the readout channels, one FADC board processes 48 APV25 outputs with one FPGA. The FPGA performs pedestal-subtraction, two-step common-mode correction, and zero-suppression for the sake of the data reduction. The development of the first prototype of the SVD readout system was completed in Dec. 2013, and the per-

formance study of this system was done in an electron beam at DESY in Jan. 2014. In the beam test, the prototype system was implemented into the Belle II DAQ for the first time and the whole data-streaming was successfully operated.

In this presentation, we will introduce features of the SVD readout system, and report on prototype performance results from the beam test, as well as future prospects for the Belle II experiment.

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