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Firmware development and testing of the ATLAS IBL Back-Of-Crate card

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The ATLAS experiment is the the largest of the four LHC experiments. Currently its Pixel-Detector is being upgraded with a new innermost 4th layer, the Insertable b-Layer (IBL). The upgrade will result in better tracking efficiency and compensate radiation damages of the Pixel-Detector. Newly developed front-end electronics (FE-I4) will require a complete re-design of the Off-Detector-Electronics consisting of the Back-Of-Crate card (BOC) and the Read-Out-Driver (ROD).
The main purpose of the BOC card is the distribution of the LHC clock to all Pixel-Detector components as well as interfacing the detector and the higher-level-readout optically. It is equipped with three Xilinx Spartan-6 FPGAs, one BOC Control FPGA (BCF) and two BOC Main FPGAs (BMF). The BMF are responsible for the signal processing of all incoming and outgoing data.
The data-path to the detector is running a 40 MHz bi-phase-mark encoded stream. This stream is delayed by a fine delay block using Spartan-6 IODELAY primitives. The primitives are reconfigured using partial reconfiguration inside the FPGA. The 160 MHz 8b10b-encoded data-path from the detector is phase and word-aligned in the firmware and then forwarded to the ROD after decoding. The ROD it will send out the processed data which is then forwarded to the higher-level readout by the BOC card.
An overview of the firmware, which has been developed, will be presented together with the results from production tests and the system test at CERN. One focus will be the partial reconfiguration and the results of the fine delay measurements.

Summary

For the new innermost layer of the ATLAS Pixel-Detector at CERN new off-detector hardware needs to be developed. The Back-Of-Crate card (BOC) is driving the optical interface to the detector and distributing the LHC clock to all detector components. A brief overview of the firmware and test results from production and system test will be presented.
Abstract

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