Firmware development and testing of the ATLAS IBL Readout Driver card

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on behalf of the ATLAS IBL DAQ group
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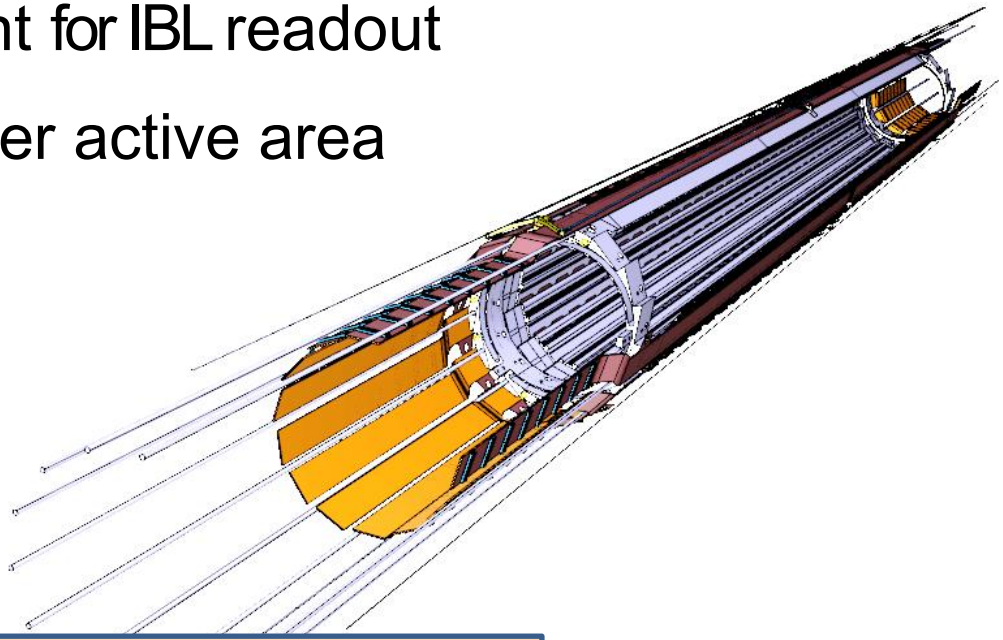
The Insertable-B Layer

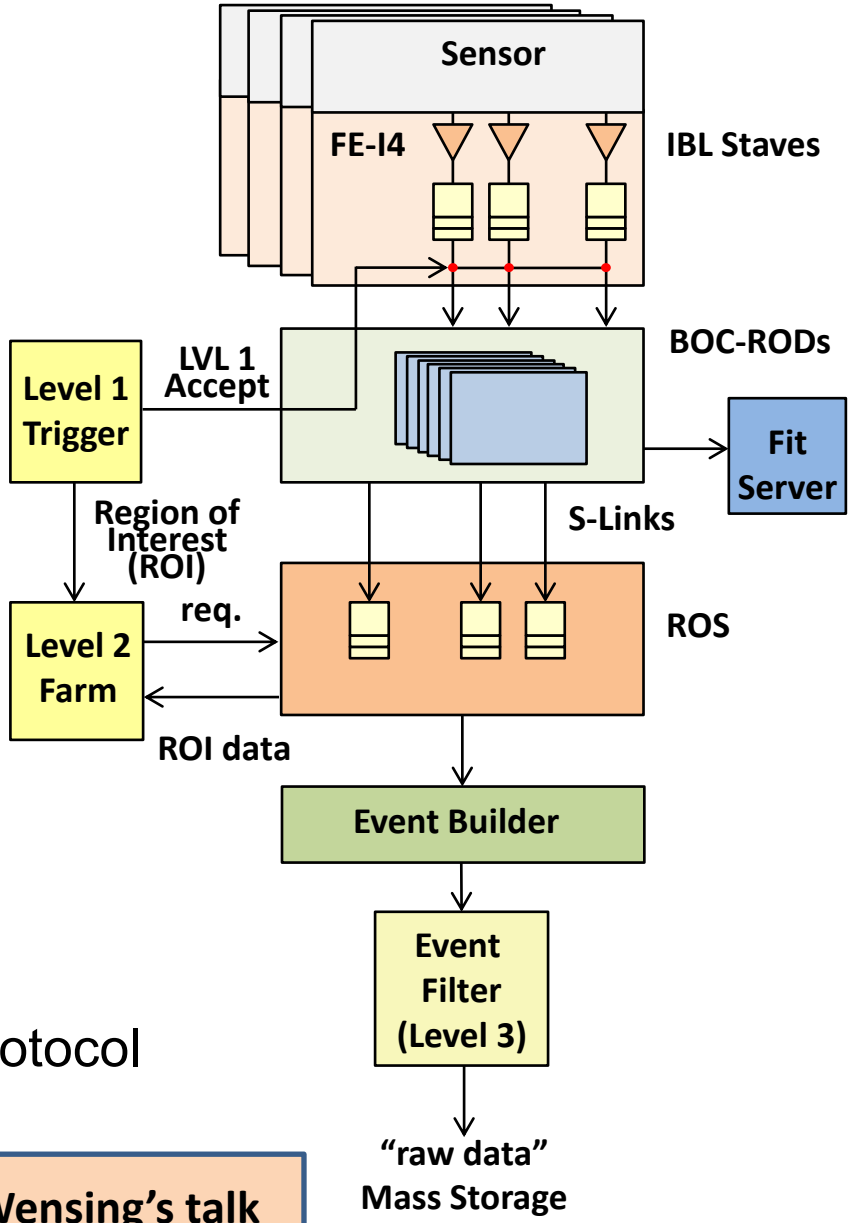
- The successfully installed (May 2014) new inner layer of the ATLAS Pixel detector at the LHC at CERN
- Higher luminosity and closer to interaction point → higher occupancy expected
- Existing Pixel FE inefficient for IBL readout
- New FEs (FE-I4) with larger active area and higher readout speed
- New Readout Drivers and Back of Crate Cards



Details on IBL covered in Cecile Lapoire's talk

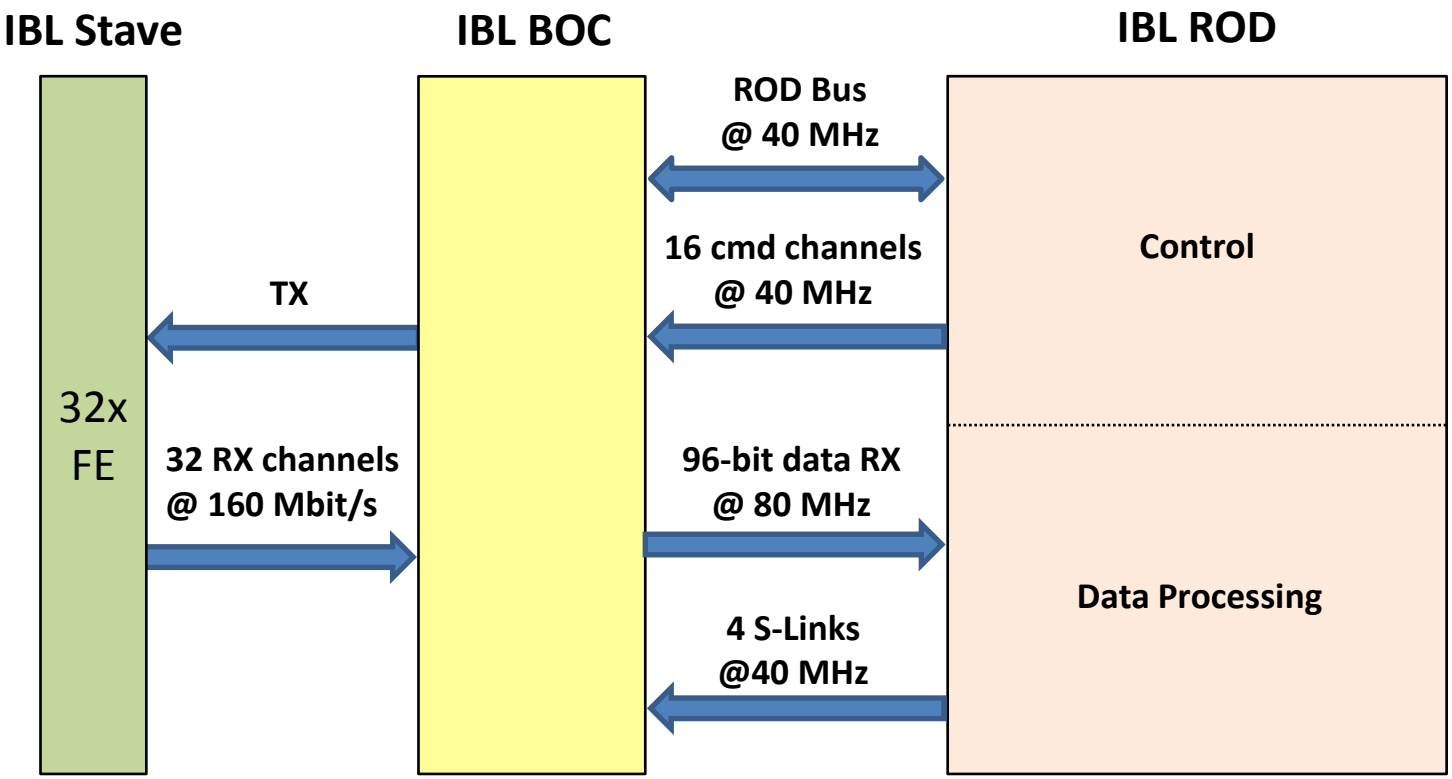
Trigger DAQ

- Based on the VMEx64 Pixel TDAQ
- On-detector (staves)
- Optical communication to off-detector (ROD/BOC)
- TTC Interface Module (TIM)
- VME-crate cards (TIM/ROD /BOC)
- New FitServer (for calibration)
- Readout Subsystem (ROS) with Readout Buffer INput (ROBIN) cards
- S-Link: CERN's data transmission protocol



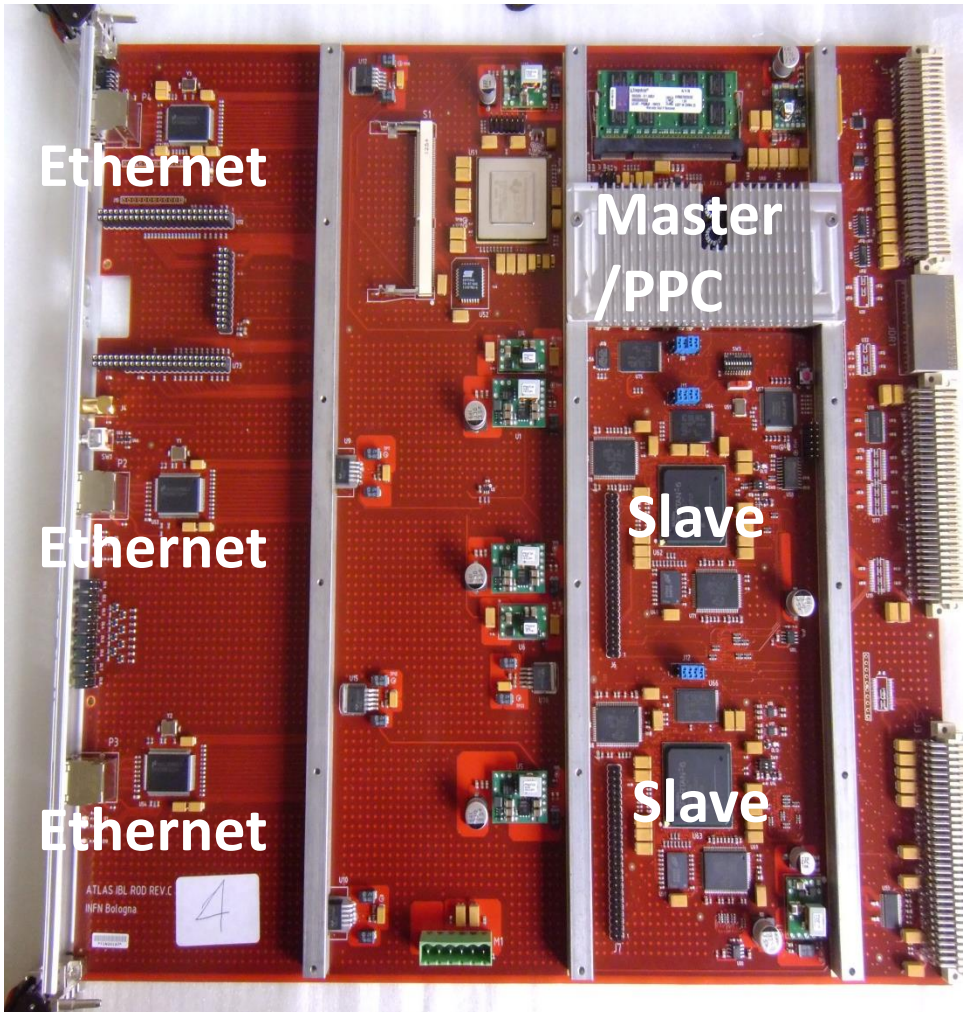
Details on IBL BOC covered in Marius Wensing's talk

ROD-BOC Communication



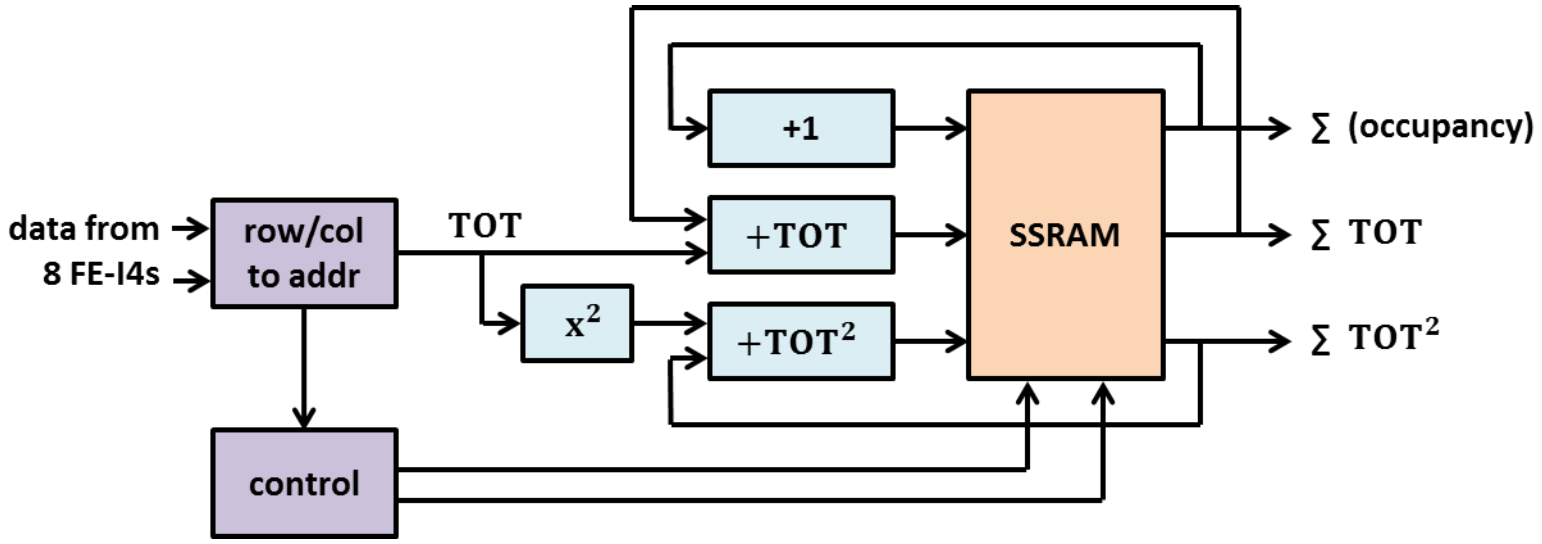
ATLAS IBL ROD Card

- FE control and readout
- Fast histogramming for FEs
- Main Components:
  - 1 Master FPGA
  - 2 Slave FPGA
  - 1 PRM FPGA
- 2 SSRAMs,1 DDR2 per slave
- 32 FE data processing
- PowerPC controller
- Upgrades for Pixel Layer 1 & 2
- 15 productions cards ready (RevC and RevD)



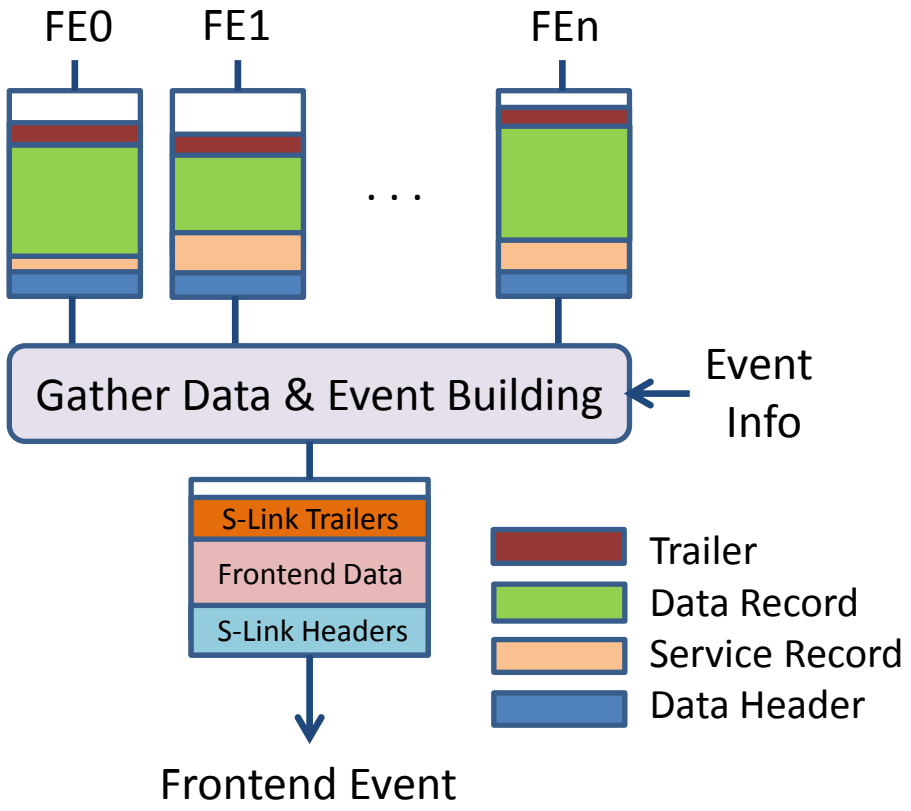
Detector Calibration

- Set uniform readout threshold for all channels
- Find and reject noisy readout cells
- Max. hit rate of 85 MHz by serializing 8 FE-I4s.
- Histograms stored and updated in external SSRAMs @ 50 MHz (speed upgrade in progress)
- Histograms transfer:
  SSRAMs → dual DMA → DDR2 → MicroBlaze TCP/IP transfer → Gbit Ethernet → FitServer

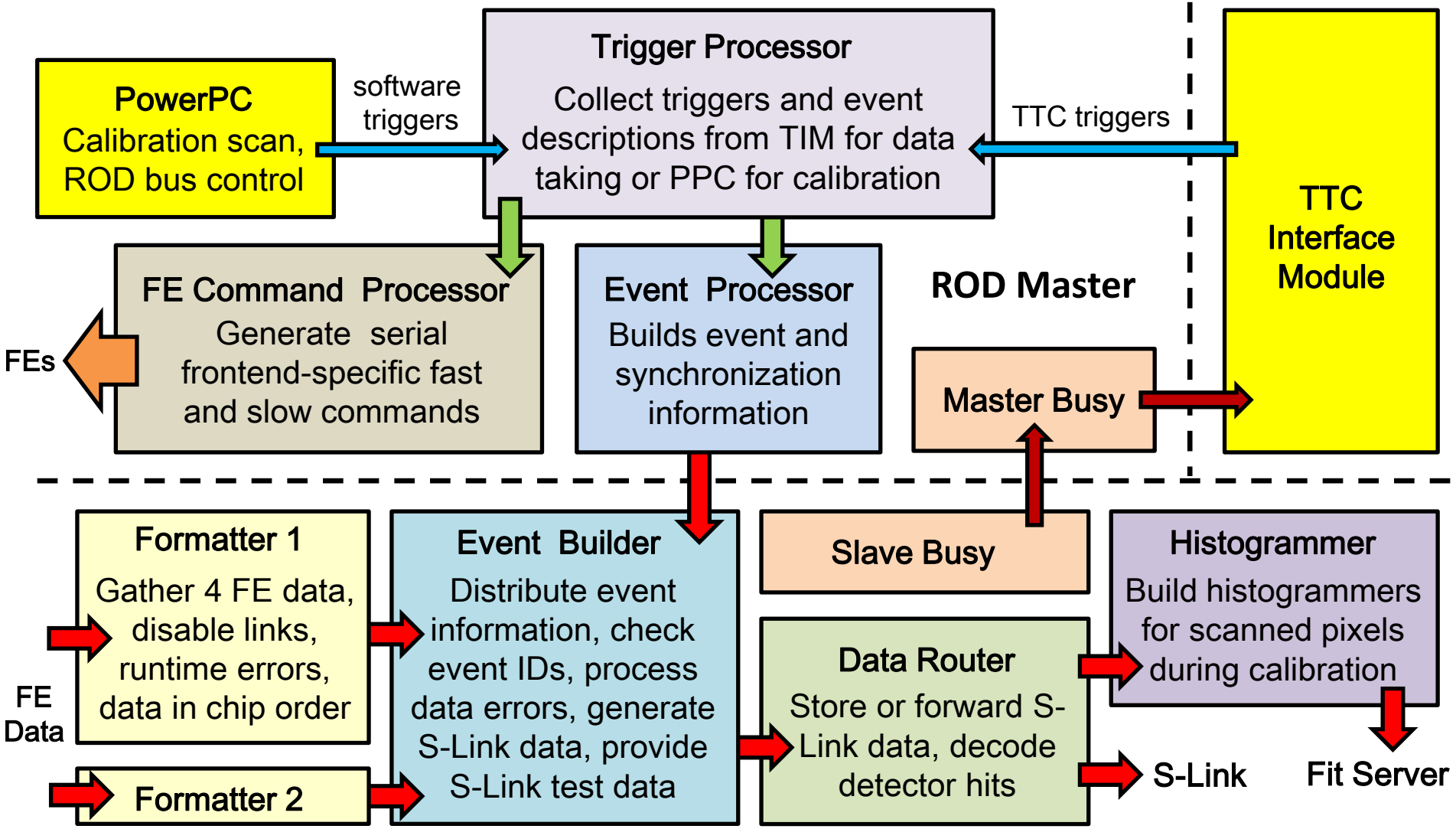


ROD Data Processing

- Modular VHDL Firmware based on Pixel ROD
  - Internalized many discrete FIFOs and memory
- Real-time @ 80 MHz
- De-randomizing FIFOs
- FE service records
- Error checking
- Busy handling
- Generate S-Link data
- Readout link test data

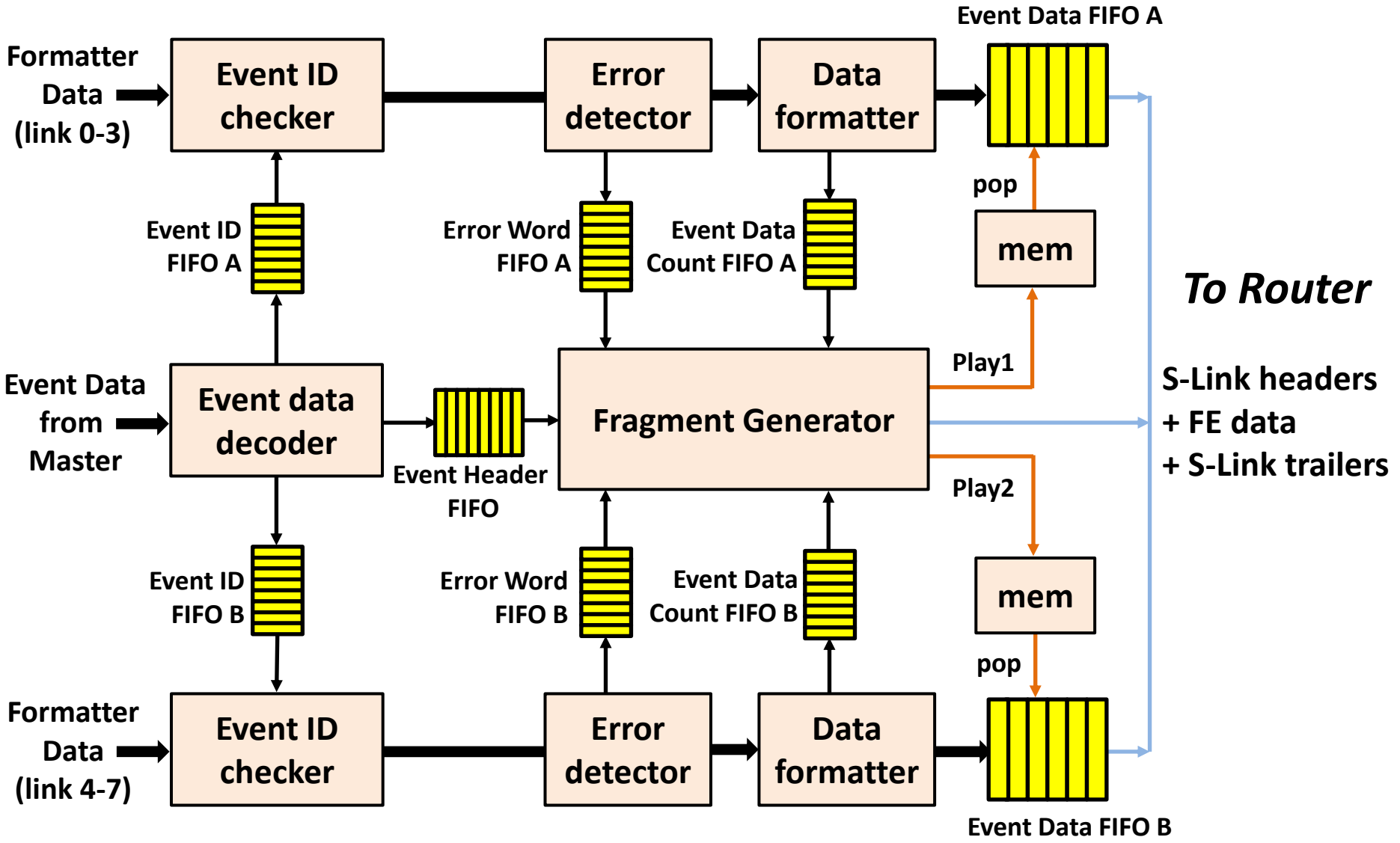


IBL ROD Control & Data Flow

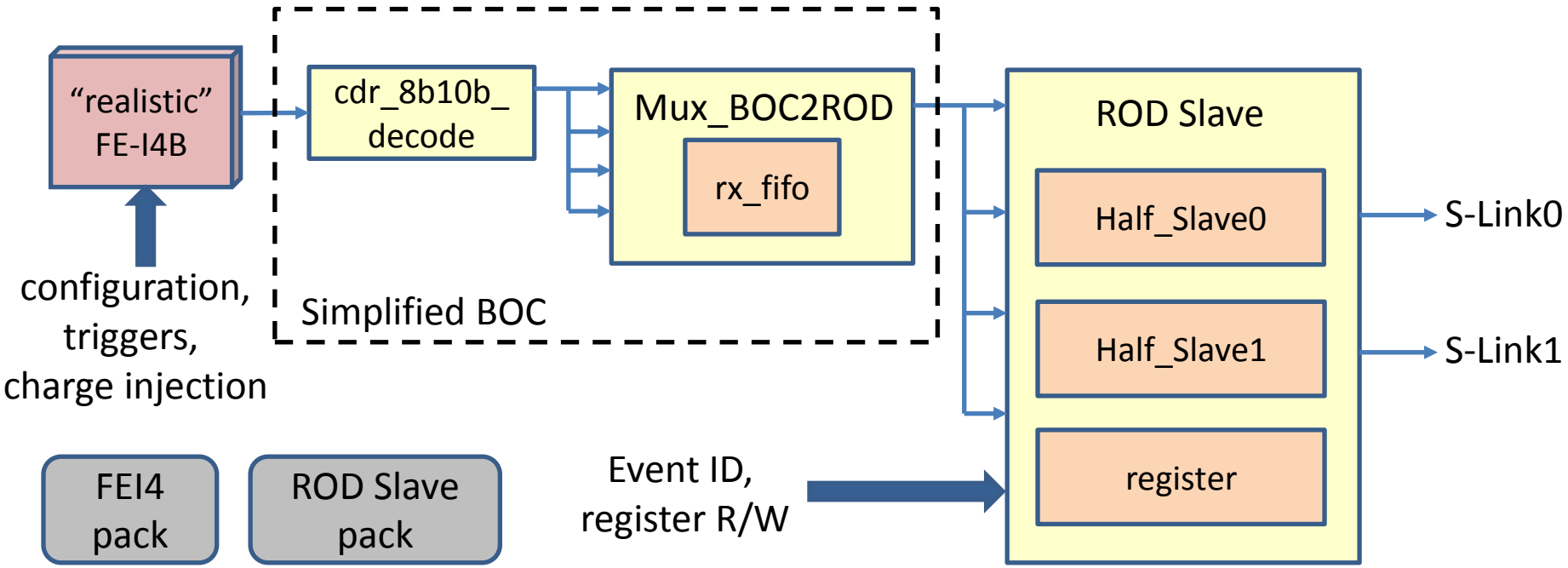


"Half Slave" inside ROD Slave

ROD Slave Event Fragment Builder

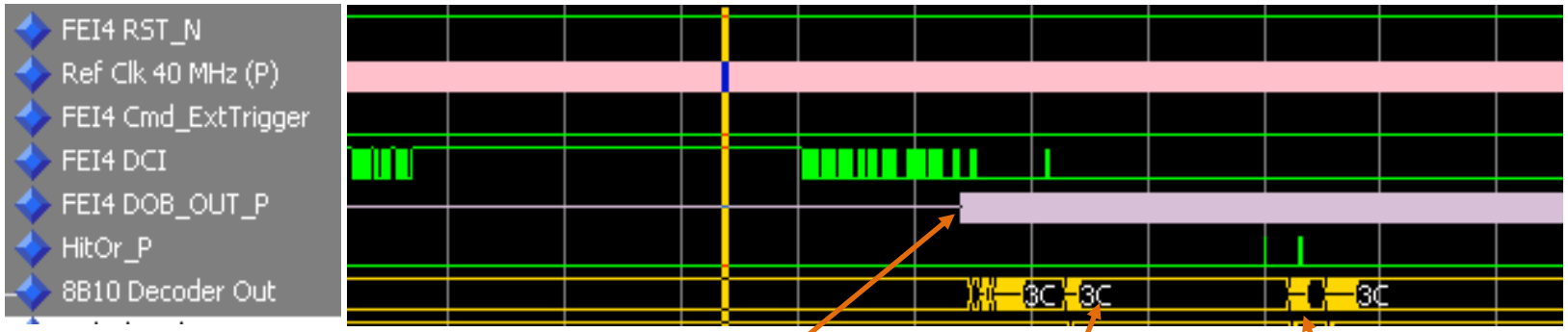


Data path simulation with realistic FE-I4 Model



- HDL model from the FE-I4 developers
- Service records and allows hits injection
- Accelerated ROD data path firmware development and greatly reduced debugging time

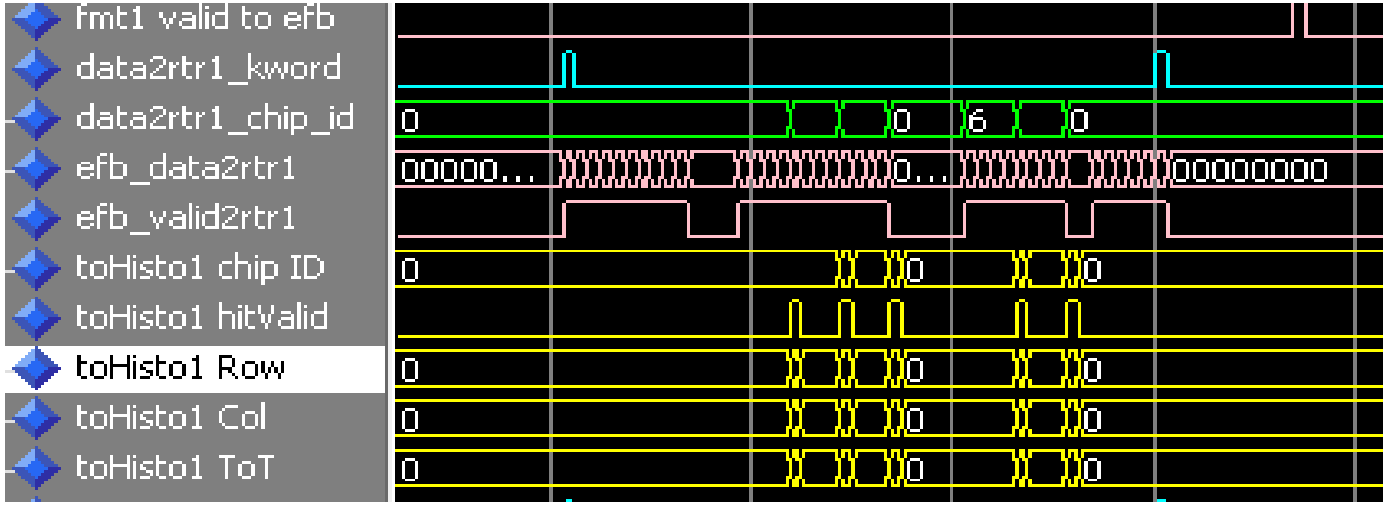
Simulation Results



FE-I4 model configured

Decoded 8b/10b idle signal

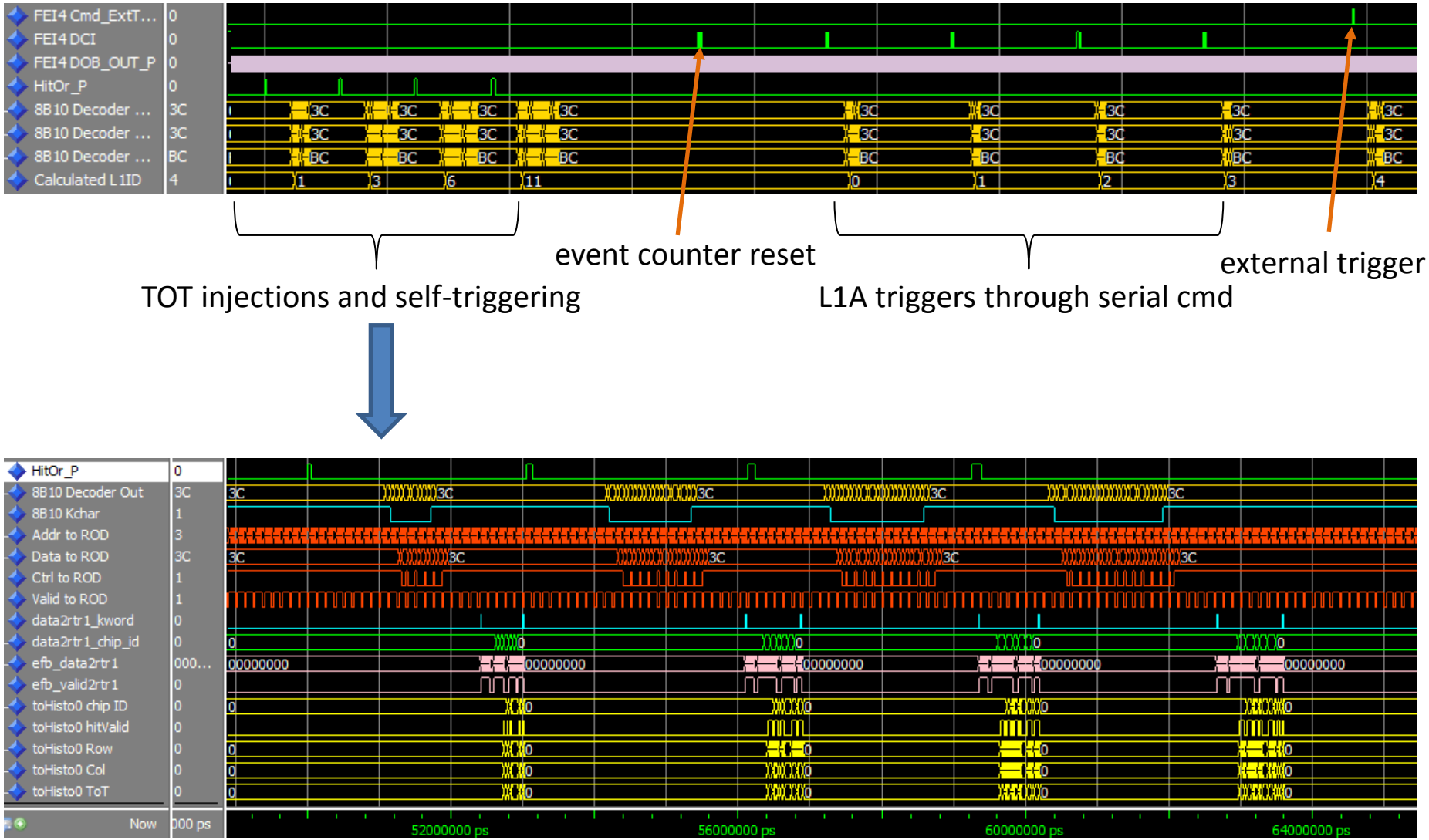
Output with injected hits



S-Link data to the Router

Extracted hit Info for the Histogrammer

Simulation Results cont.

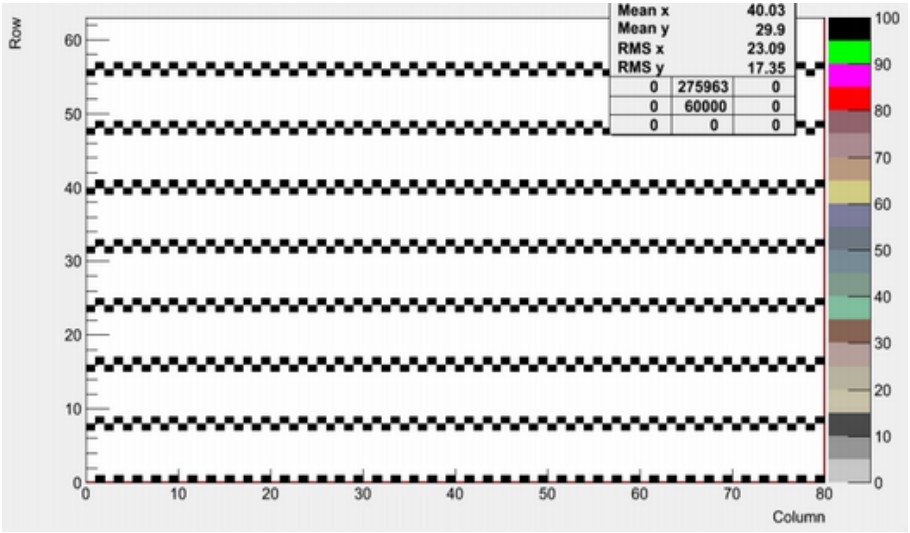


Hardware Readout Chain Tests

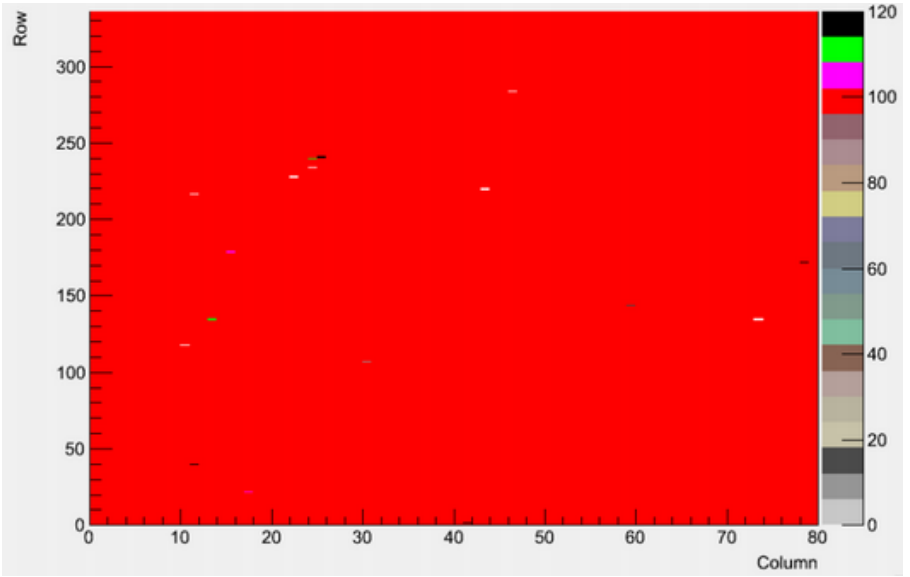
- TIM – ROD – BOC – S-Link – ROBIN
- Two sources of data are used:
  - ROD slave-generated readout link test data to ROS
  - Triggers to all 32 FE emulators on each BOC, process event on ROD, and send to ROS
- ROD can process all FE data at trigger rate of 200 KHz
  - No data corruption at ROS
  - ROBIN buffer becomes full quickly
  - IBL expect to run at 100 kHz
- Successfully triggered 16 million emulated events at 50 kHz without data corruption at ROS

Calibration Scan Results

- **Digital scan, 100 triggers,** 1/8 mask

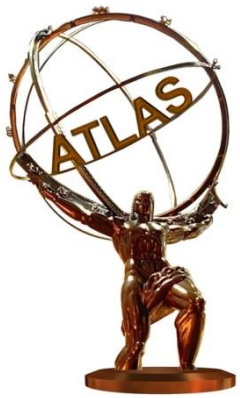


- **Analog scan, 100 triggers,** 8/8 mask



Summary

- New FPGA-based IBL RODs are commissioned for the IBL
- Higher bandwidth and integration
- Data taking and calibration functions in place
- Realistic FE model used in data path firmware development
- ROD data taking functionality verified via ROS test.
- Near future developments:
  - Develop built-in tests for IBL ROD firmware
  - Integration of Pixel readout into IBL ROD



Thank you for your attention!

Backup

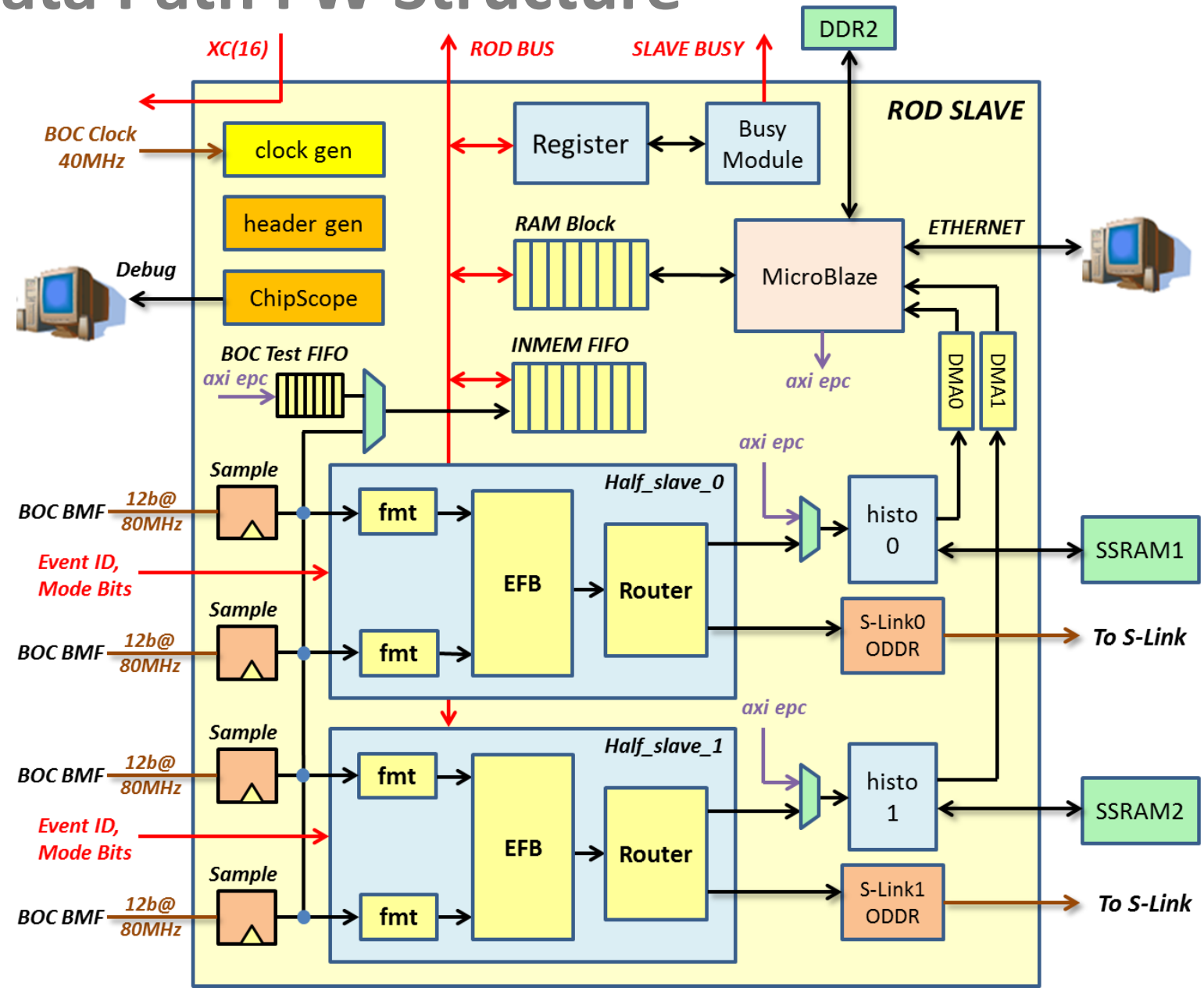
Old vs New ROD

	Pixel ROD	IBL ROD
FPGAs	1 Master + 8 Formatter + 1 EFB + 1 Router + 1 PRM	1 Master + 2 Slaves + 1 PRM
Control	Master DSP + 4 Slave DSP	Embedded PPC & MicroBlaze
Memory Components	Many External	Mostly Internal to FPGA except SSRAMs + DDR2s
Data RX rate from BOC	40 MHz (all channels enabled)	80 MHz

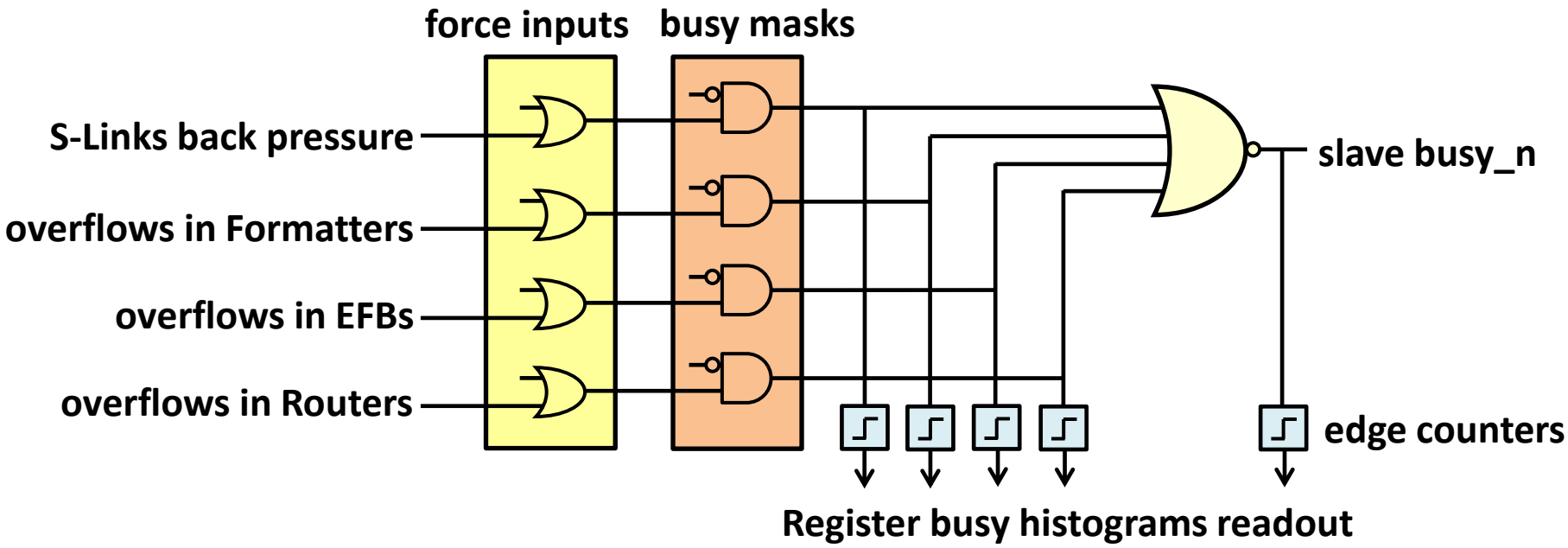
Pixel FE-I3 vs IBL FE-I4

	FE-I3 (requires MCC)	FE-I4
Pixel Size	50 um x 400 um	50 um x 250 um
Pixels/chip	2880	26880
Active area	~75%	~90%
Serial data out	40 Mbit/s	160 Mbit/s

Data Path FW Structure



Slave Busy Logic



ROD Slave Router Block