The Upgrade of the ALICE Inner Tracking System
—
Status of the R&D on Monolithic Silicon Pixel Sensors

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CERN and TU Vienna

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Outline

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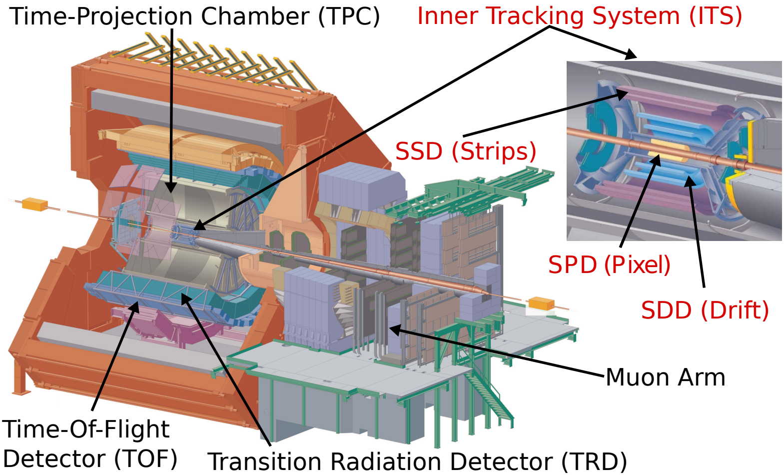
1. A Large Ion Collider Experiment (ALICE)
2. ALICE Inner Tracking System (ITS) upgrade
3. Status of R&D on monolithic silicon pixel sensors

ALICE with its present ITS



- ALICE is the experiment at the LHC optimized for A-A and p-A
- Its main goal is the study of the Quark-Gluon Plasma

ALICE Upgrade Strategy

Motivation:

- High precision measurements of rare probes at low p_T

Requirements ⇒ Targets:

- Large sample of events recorded on tape
  - Pb-Pb recorded luminosity: $10\,\mathrm{nb}^{-1}$ plus pp and p-A data
    → gain factor 100 in statistics for minimum bias trigger over current program
- Improved vertexing and tracking capabilities

Strategy:

- New silicon trackers:
  - Inner Tracking System (ITS) covering mid-rapidity
  - Muon Forward Tracker (MFT) covering forward rapidity
- Upgrades
  - TPC
  - Online systems
  - Readout of several detectors

C. Lippmann, 2.a Experiments and Upgrades,
Session 1: *Upgrade of the ALICE detector*

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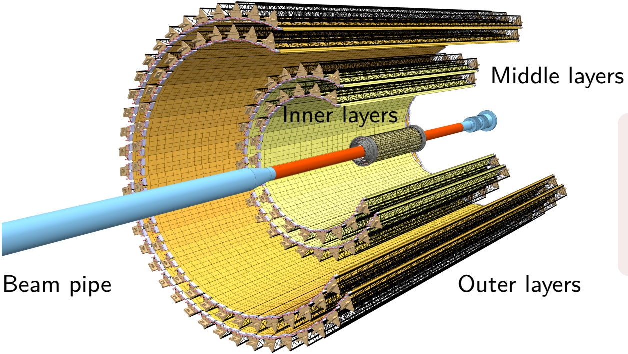
ALICE ITS upgrade design objectives

1. Improve **impact parameter resolution** by factor $\approx 3(5)$ in r-ϕ(z) at $p_T = 500\,\mathrm{MeV}/c$
   - move closer to IP (position of first layer): 39 mm $\rightarrow$ 22 mm
   - reduce material budget: X/X_0/layer: $\sim 1.14\% \rightarrow 0.3\%$ (inner layers)
   - reduce pixel size: $50\,\mu m \times 425\,\mu m \rightarrow O(30\,\mu m \times 30\,\mu m)$
2. Improve **tracking efficiency** and p_T **resolution** at low p_T
   - increase granularity: 6 layers $\rightarrow$ 7 layers
3. **Fast readout** (now limited at 1 kHz with full ITS):
   - Pb-Pb: > 50 kHz
   - pp: several 100 kHz
4. Fast insertion/removal
   - possibility to access for yearly maintenance

The new ALICE ITS will fully replace the present ITS

Layout of upgraded ALICE ITS

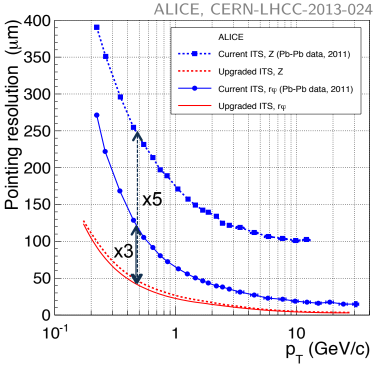


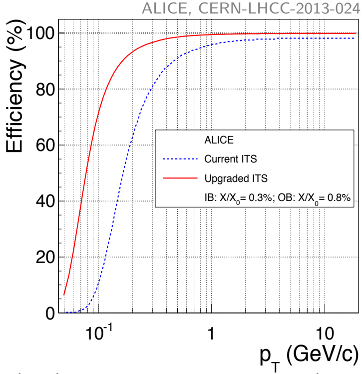
- $\approx$ 12.5 Gigapixels
- Binary readout
- $\sim 10\,\mathrm{m}^2$ of silicon

- Radiation level (innermost layer, including a safety factor 10):
  - 700 krad (TID) and 1×10^{13} 1 MeV n_{eq} (NIEL)
- Radial coverage: 22 mm to 400 mm
- η coverage: $|\eta| \leq 1.22$, for tracks from 90 % most luminous region

- Very **thin sensors**
- Very **high granularity**
- **Large area** to cover
- **Modest radiation levels**

⇒ **Monolithic silicon pixel sensors**





Exected improvement of pointing resolution (left) and tracking efficiency (right)

Outline

1. A Large Ion Collider Experiment (ALICE)
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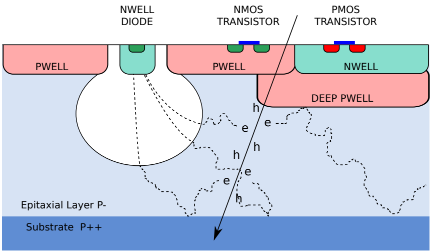
- **Monolithic silicon pixel sensors** using TowerJazz 0.18 µm CMOS Imaging Process
  - **High-resistivity epitaxial** layer on p-type substrate
  - Special deep p-well for **full CMOS within the matrix** (based on the experience of RAL)
  - **Working principle:**



schematic cross section of pixel of monolithic silicon pixel sensor

NWELL diode output signal:

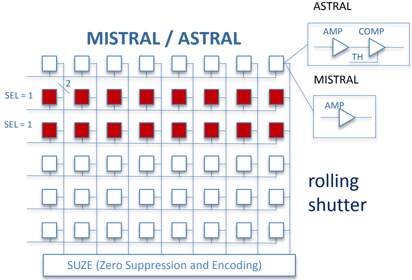
$$\mathbf{V \sim Q/C}$$

- Mitigate charge spread over different pixels
- Minimize capacitance:
  - diode surface
  - depletion volume
    $\rightarrow$ (reverse) biasing

Pixel chip architectures under development

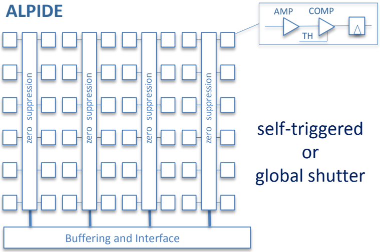
- **Different architecture design streams**:

— ASTRAL (MISTRAL):



based on the experience of the STAR PXL detector

— ALPIDE:



A. Collu, poster 26, *An innovative Monolithic Active Pixel Sensor for the Upgrade of the ALICE ITS*

General requirements:

- Chip size: 15 mm × 30 mm
- Sensor thickness: 50 μm
- Spatial resolution: ≈ 5 μm
- Integration time: < 30 μs
- Power density: < 100 mW/cm^2

Pixel chip - R&D

- Dedicated **R&D** started in 2011 :
  - Improve **Signal/Noise Ratio** (SNR):
    - optimization of charge collection diode, apply reverse-bias voltage
    - optimize thickness and resistivity of epitaxial layer
  - Study **different front-end and readout architectures**
    - reduce power consumption and integration/readout time
  - Study **radiation effects**
- Several small and large scale **prototypes**, each focussing on particular aspect:

Architecture	**Analogue**	**Digital**	
		small-scale	*full-scale*
ASTRAL (MISTRAL)	MIMOSA-32-X MIMOSA-34	MIMOSA-22THR-X AROM-0/1	FSBB
ALPIDE	Explorer-0 Explorer-1	pALPIDE	pALPIDEfs

ASTRAL (MISTRAL)

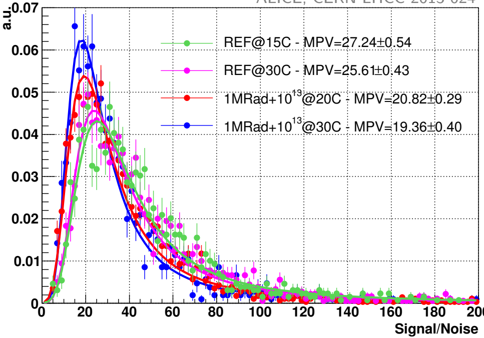
MIMOSA-32ter

analogue prototype with in-pixel pre-amplification & average noise subtraction

→ *in-pixel circuitry optimisation, radiation hardness*

- Seed pixel SNR before and after irradiation with 1 Mrad (TID) and 1×10^{13} 1 MeV n_{eq} (NIEL) at 20° and 30° C

ALICE, CERN-LHCC-2013-024



- Adequate radiation hardness

SNR measured for MIMOSA-32ter sensors (on an HR-18 wafer type) in the SPS with a 120 GeV/c pion beam

ALPIDE

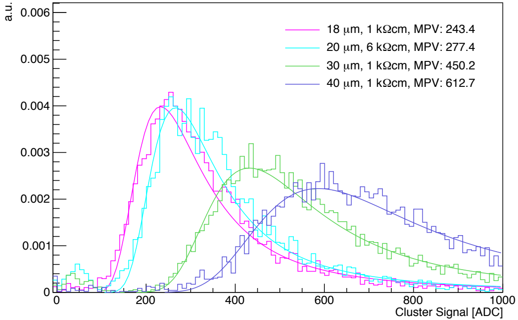
ALICE

Explorer-1

analogue prototype with variable integration and readout time, 20 and 30 μm pitch

→ *charge collection, reverse biasing, noise*

- Study of different starting wafers



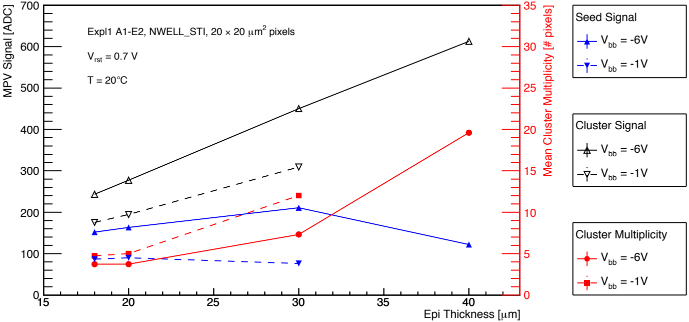
Epitaxial Layer		
Type	**Thickness** [μm]	**Resistivity** [kΩ cm]
HR-18	18	> 1
HR-20	20	6.2
HR-30	30	≈ 1
HR-40A	40	≈ 1
HR-40B	40	7.2

Cluster signal for different epi thicknesses at $V_{bb} = -6\,V$ measured at test beam at DESY with 3.2 GeV/c electron beam (pixel size $20\times 20\,\mu m^2$)

ALPIDE

Explorer-1

ALICE, CERN-LHCC-2013-024



Seed signal, cluster signal and multiplicity vs. epi thickness for $V_{bb} = -1\,V$ and $-6\,V$

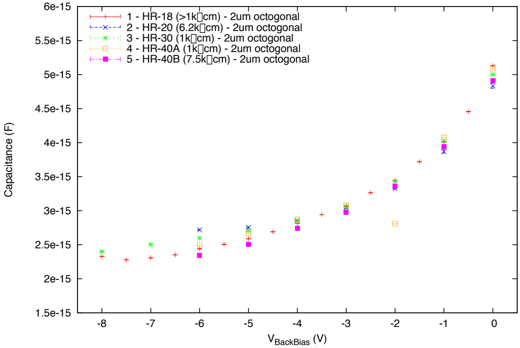
Average pixel noise ≈ 3 ADC

- **Reverse bias:** significant increase of SNR
- Cluster charge increases linearly with the epi layer thickness
- Cluster size increases for thicker epi layer thicknesses
- **Largest SNR** (seed pixel): HR-30 for $V_{bb} = -6\,\text{V}$, HR-20 for $V_{bb} = -1\,\text{V}$

Pixel chip - Experimental results

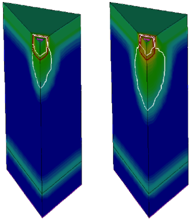
ALPIDE

Explorer-1



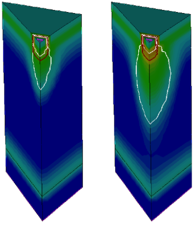
Pixel capacitance vs V_{bb} for different starting wafer types

ALICE, CERN-LHCC-2013-024



(a) $-1\,\mathrm{V}$, $10^{13}\,\mathrm{cm}^{-3}$ (b) $-6\,\mathrm{V}$, $10^{13}\,\mathrm{cm}^{-3}$

TCAD simulations



(c) $-1\,\mathrm{V}$, $10^{12}\,\mathrm{cm}^{-3}$ (d) $-6\,\mathrm{V}$, $10^{12}\,\mathrm{cm}^{-3}$

- **Pixel capacitance** drops with increasing **reverse bias**, in agreement with simulated size of depletion region
- Effect similar for all starting materials → **minor influence of epi resistivity** for current pixel layouts

ASTRAL (MISTRAL)

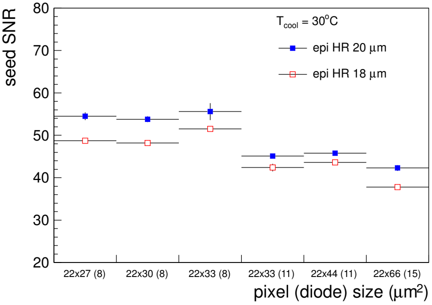
MIMOSA-34

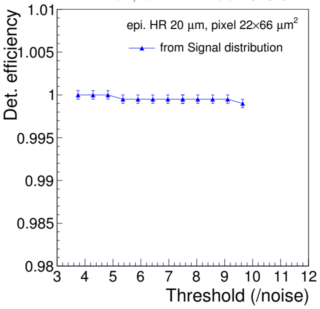
analogue prototype with no in-pixel pre-amplification and CDS circuitry

→ *sensing node optimisation as function of pixel size and epitaxial layer characteristics*

- SNR of seed pixel for pixels in the range $22 \times 27\,\mu m^2$ to $22 \times 66\,\mu m^2$

ALICE, CERN-LHCC-2013-024





Measured at test beam at DESY with 4.4 GeV/c electron beam

- High detection efficiency also for large pixels

Pixel chip - Experimental results

ASTRAL (MISTRAL)

MIMOSA-22THR

in-pixel pre-amplification and CDS circuitry, parallel column readout and discriminators at end of column, $22 \times 33\,\mu m^2$ pixels

$\rightarrow$ *used to validate upstream part of MISTRAL and most of ASTRAL readout*

ALPIDE

pALPIDE

in-pixel front-end, binary readout, in-matrix sparsification, $22\,\mu m$ pitch

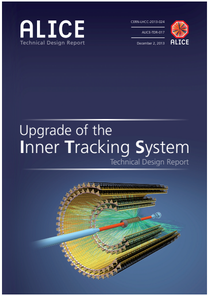
$\rightarrow$ *used for optimization of in-pixel front-end with binary readout and priority encoder*

- Measured at **test beam** at DESY with 3 to 6 GeV e^- and e^+ beams:
  - Detection efficiency: $> 99\,\%$
  - Fake hit rate: $\approx 10^{-8}/(\text{event}\times\text{pixel})$
  - Spatial resolution $\approx 5\,\mu m$

- Performance of small scale digital prototypes complies with requirements

Summary

- **New ALICE ITS** with **7 layers of monolithic silicon pixel sensors** will be installed during LS2 of the LHC in 2018/19
- **Different architectures** for the pixel chip have been explored
- Several small-scale **prototype sensors** have been characterized in test beam and laboratory
  - **adequate radiation hardness** has been proven
  - **reverse biasing**: significant increase of SNR
  - effects of different **epi layer thicknesses** and **resistivities**:
    - regions of parameter space could be excluded $\rightarrow$ approaching optimum
    - epi resistivity has minor influence for current pixel layouts
  - performance of small scale **digital prototypes** complies with requirements of pixel chip
- **Full-scale prototypes** are currently beeing characterized



TDR approved by RB on 12th March 2014

Spare slides

Pixel chip general requirements

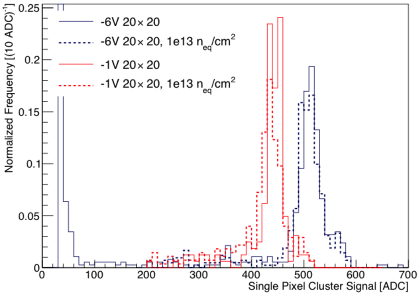
Parameter	Inner Barrel	Outer Barrel
max. silicon thickness (µm)	50	
spatial resolution (µm)	5	30
chip dimensions (mm^2)	15×30	
max. power density (mW)	300	100
max. integration time (µs)	30	

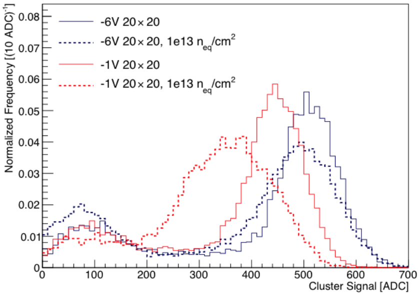
Explorer-0

analogue prototype with variable integration and readout time, 20 μm and 30 μm pitch

→ *for pixel layout optimisation (charge collection, reverse biasing, noise)*

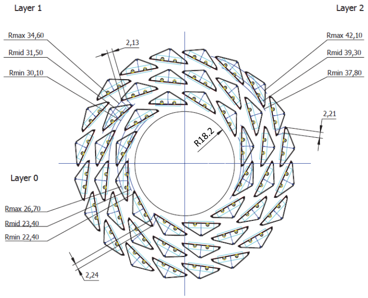
- Pixel response to X-rays from ^{55}Fe source before and after irradiation with 1×10^{13} 1 MeV n_{eq} (NIEL)

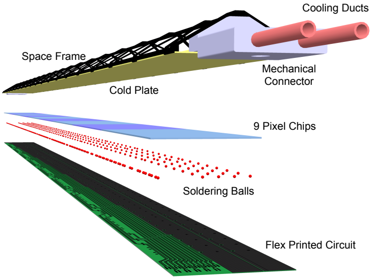




Signal of signal pixel clusters (left) and all clusters (right) at $V_{bb} = -1$ V and -6 V for pixel size of $20 \times 20\,\mu m^2$

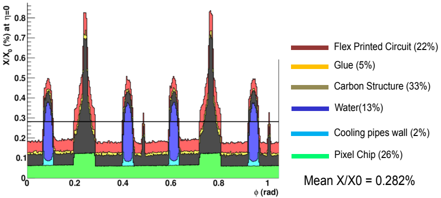
Inner Barrel

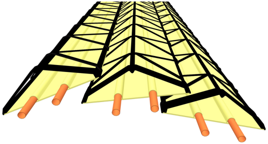


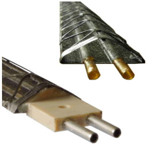


Material budget: ~ 0.3 % X_0 per layer

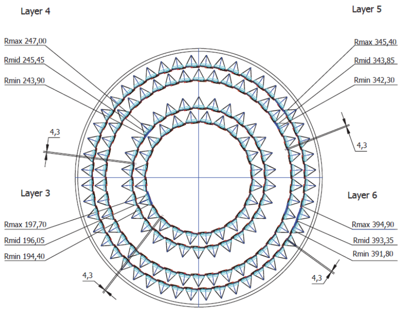
Inner Barrel Stave

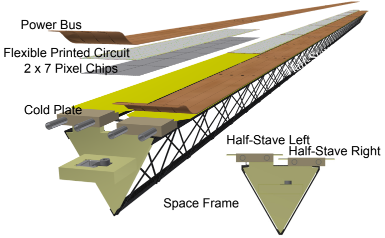






Outer Barrel





Outer Barrel Stave

Material budget: ~ 0.8 % X_0 per layer