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A power-pulsing scheme for the CLIC vertex detector and its 3D integration

The vertex detector is the innermost detector at the proposed CLIC linear electron-positron collider. It is composed of several layers of pixel sensors and readout ASICs, and the barrel region is made of "ladders". The precision physics requirements limit the material budget for sensors, readout, support, cooling and cabling to less than 0.2% of a radiation length (X0) per detection layer. However, the power consumption of the readout electronics strongly impacts the required low material budget of the detector. To reduce the cable and cooling material, the average power per unit area has to be small (<50 mW/cmˆ2). The collision at CLIC will occur in bunch crossings every 0.5 ns during a bunch train of 156 ns. The time between consecutive trains is approximately 20 ms. Turning on the readout ASICs during the bunch trains and keeping them idle in the other part of the cycle will therefore significantly reduce the average power dissipation. The use of this beam duty cycle to reduce the average power is known as power-pulsing.

The use of a power-pulsing scheme implies that the ASIC current consumption has to change suddenly from its idle value (few hundreds of mA) to full load (more than 40 Amps for a single ladder composed of 24 ASICs) within a few microseconds, then remain constant for enough time to record and process the events (few tens of microseconds) and finally drop back to the idle current value. During the bunch train, the power consumption is at its maximum and constant, and the supplied voltage for the analog components has to remain within 5% of the nominal voltage in order to allow for a correct functioning of the readout ASICs. The latter is particularly challenging, considering the big transient that takes place before the readout process. The analog and digital components of the ASICs have different constraints and therefore will be powered separately.

A power-pulsing scheme based on a controlled current source allows achieving a material contribution of 0.1% of X0, which is expected to be reduced as the silicon capacitors technology improves. It consists of a controlled back-end current source that charges silicon capacitors in the ladder with low current during the idle time. In this way, the charging current is reduced to less than 100 mA for a whole ladder. The charge accumulated in these capacitors is then delivered to the ASICs during the bunch crossing time and the voltage is regulated using Low Dropout Regulators (LDOs). A prototype of this back-end current source was implemented using an FPGA. A dummy load emulating the power consumption of the analog and digital components has been implemented.

In order to consolidate the proposed scheme the integration of such a system was studied. This implementation requires the use of through silicon vias, silicon capacitor die structures, and 3D connections to an LDO and a low mass interconnection cable.

This talk will present the proposed powering scheme and the possible solutions of the 3D integration problem.

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