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Vertex-Detector R&D for CLIC

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The CLIC vertex detector must have excellent spatial resolution, full geometrical coverage extending to low polar angles, extremely low mass, low occupancy facilitated by time-tagging, and sufficient heat removal from sensors and readout. These considerations, together with the physics needs and beam structure of CLIC, push the technological requirements to the limits and imply a very different vertex detector than the ones currently in use elsewhere. A detector concept based on hybrid planar pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. In this talk, the CLIC vertex-detector requirements are reviewed and the current status of R&D on sensors, readout and detector integration is presented.

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