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DEPFET Active Pixel Detector

Ultra-transparent DEPFET pixel detectors for future e^+e^- experiments

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DEPFET Collaboration

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The DEPFET Collaboration

- Charles University, Prague
- DESY, Hamburg
- IFCA, Santander
- IFIC, Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- LMU Munich
- MPI, Munich
- HLL, Munich
- TU, Munich
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen
- University of Tabuk

Outline

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- DEPFET for future colliders
  - SuperKEKB and ILC
- DEPFET system
  - Sensor development
  - ASICs
- Latest results
  - Lab and beam tests

Future Vertex Detectors

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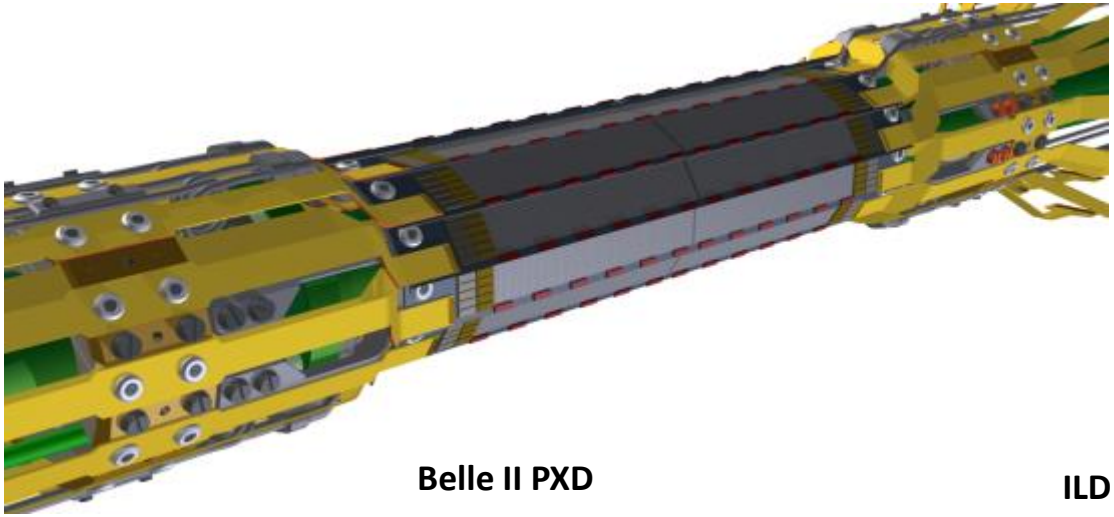
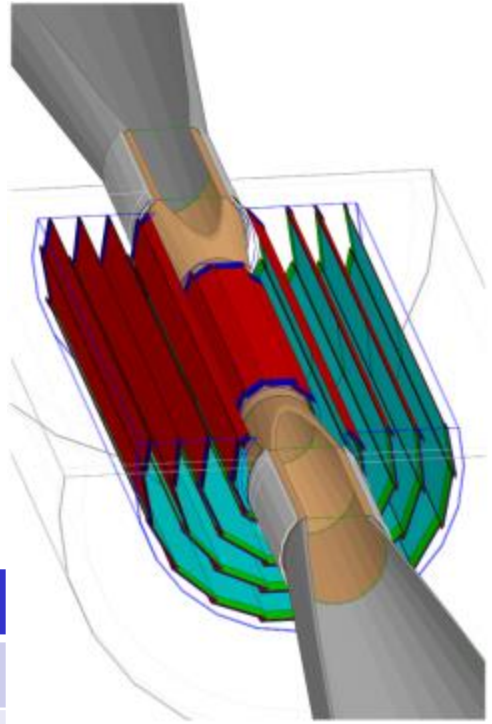
The Belle II Collaboration decided on DEPFET as baseline for the pixel detector



Belle II PXD



ILD 5-layer VXD

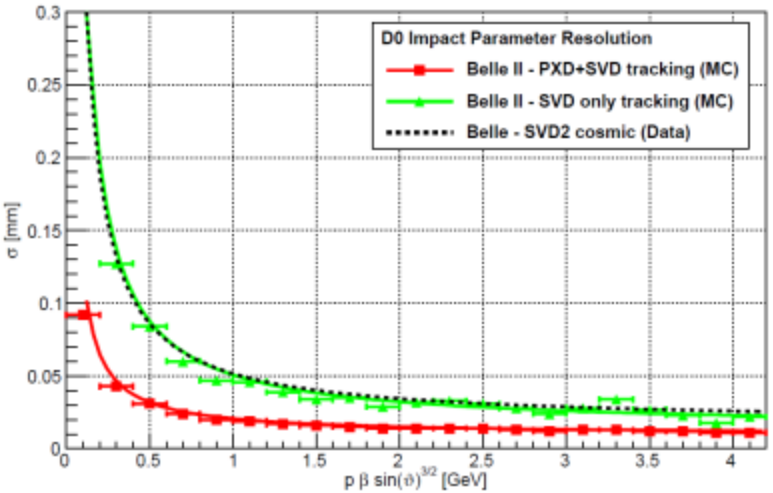
	Belle II	ILD LOI 5-layer layout	
Radii	14, 22	15, 26, 38, 49, 60	mm
Ladder length	90 (L1), 122 (L2)	123 (L1), 250 (L2-L5)	mm
Sensitive width	12.5 (L1-L2)	13 (L1), 22 (L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel size	50x50 (L1), 50x75 (L2)	25x25 (L1-L5)	μm^2
Frame rate	50	20 (L1), 4 (L2-L5)	kHz

The Belle II PXD DEPFET ladders: *almost* prototypes for L1 and L2 of ILD

↘ **Positive impact on DEPFETs for ILC**

Belle II Vertex Detector Requirements

	Belle II
Occupancy	0.4 hits/μm^2/s
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Duty cycle	1
Frame time	20 μs
Momentum range	Low momentum (< 1 GeV)
Acceptance	17º-155º
Material budget	0.21% X_0 per layer
Resolution	15 μm (50x75 μm^2)



- Modest resolution (15 μm), dominated by multiple scattering → Pixel size (50 x 75 μm²)
- Lowest possible material budget (0.2% X_0/layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services

ILC Detector Concepts and Belle II

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	Belle II	ILC
Occupancy	0.4 hits/μm^2/s	0.13 hits/μm^2/s
Radiation	2 Mrad/year	< 100 krad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year	10^{11} 1 MeV n_{eq} per year
Duty cycle	1	1/200
Frame time	20 μs	25-100 μs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	17º-155º	6º-174º
Material budget	0.21% X_0 per layer	0.12% X_0 per layer
Resolution	15 μm (50x75 μm^2)	5 μm (20x20 μm^2)

- Excellent resolution (5 μm) → Pixel size (20 x 20 μm²)
- Lowest possible material budget (0.1% X_0/layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services

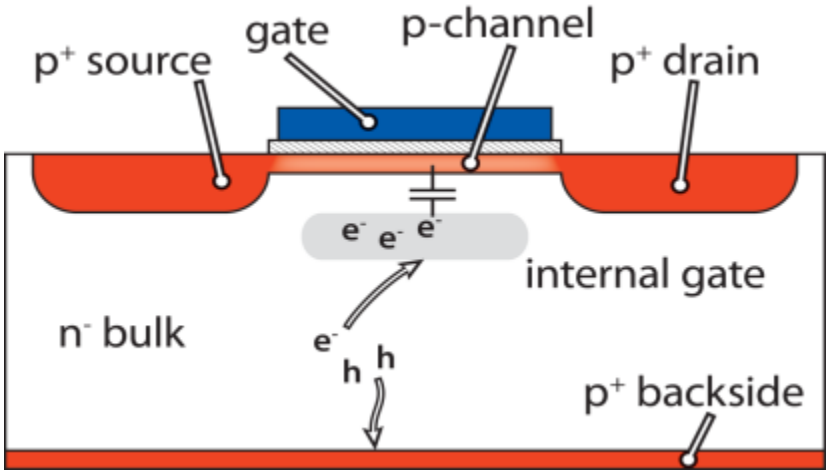
→ Both detectors have very similar requirements

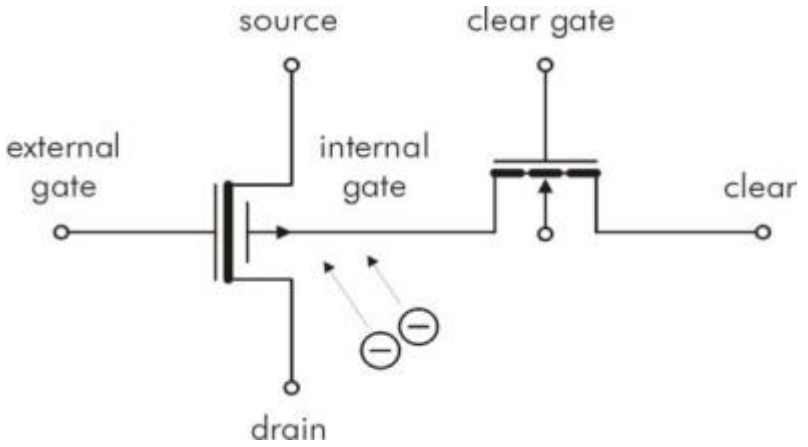
DEPFET – DEpleted P-channel FET

- Each pixel is a p-channel FET on a completely depleted bulk.
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)
- Signal electrons in the internal gate modulate the transistor current

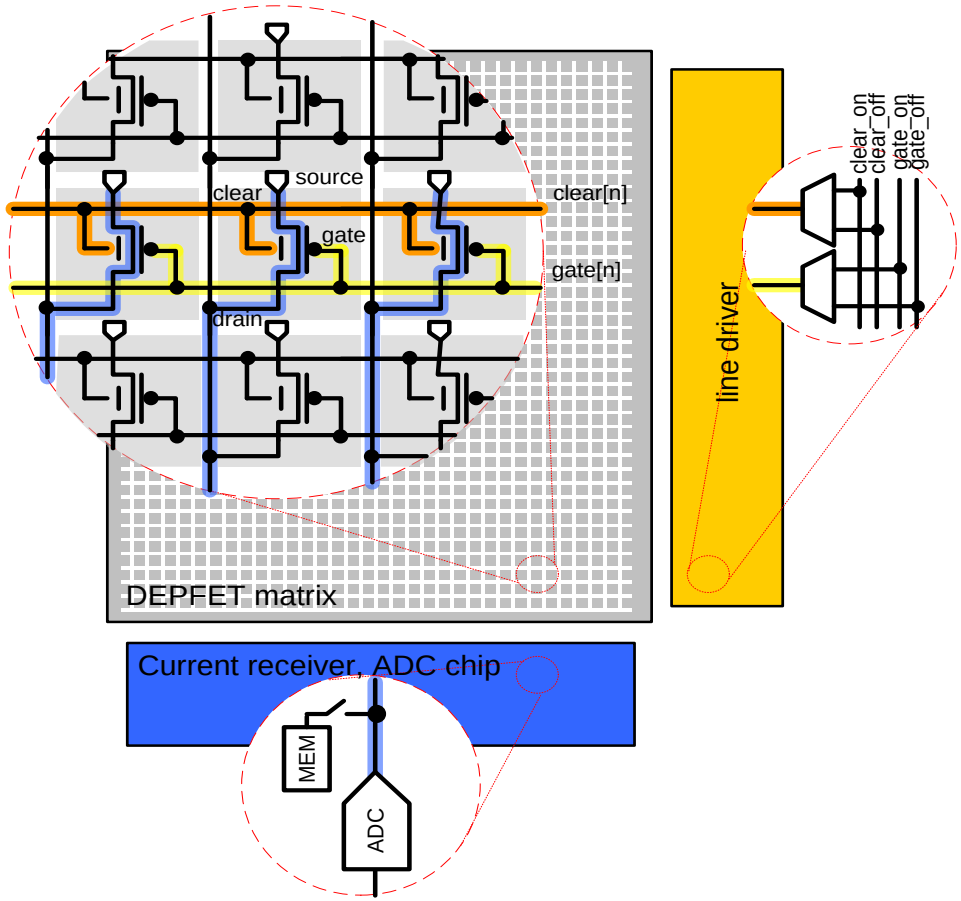
$$g_q = \frac{\partial I_d}{\partial q} \propto \left(\frac{I_d}{L^3 W C_{ox}}\right)^{1/2} \sim 500 pA/e^-$$

- Detection and internal amplification
- Small intrinsic noise
- Low power consumption





DEPFET Pixel Array



- Pixels are arranged in a matrix
- Row wise readout (4 rows at a time)
- Gate, clear lines need Switcher steering chip
- Long drain readout lines to keep material out of the acceptance region
- Only ‘activated’ rows consume power
  - The others are still sensitive to charge
  - Low power consumption

The DEPFET Ladder

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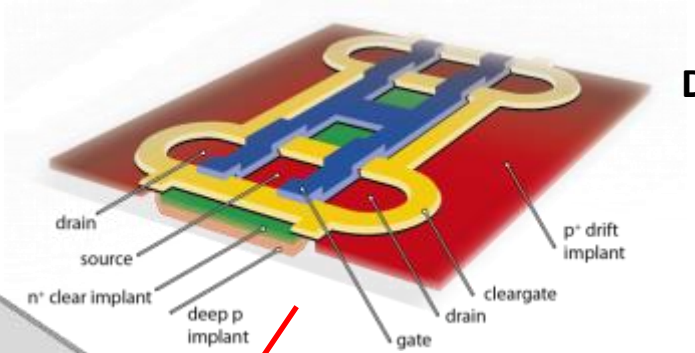
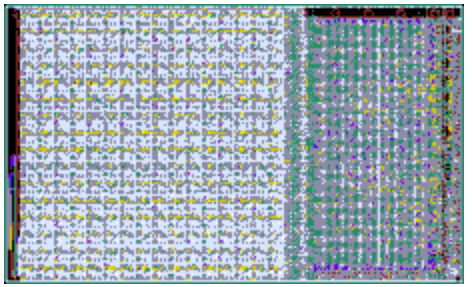
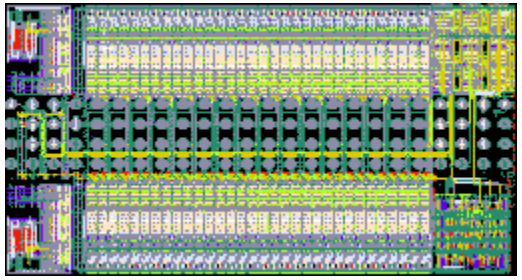


DCDB (Drain Current Digitizer)
Analog frontend



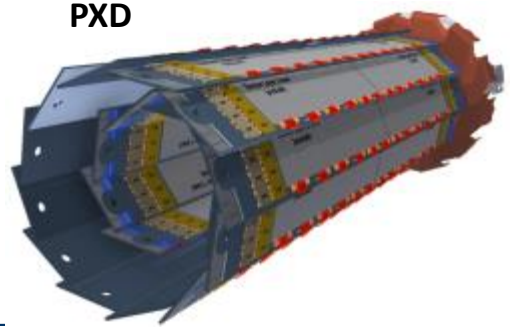
UMC 180 nm
Size 5.0×3.2 mm^2
TIA and ADC
Pedestal compensation
Rad. Hard proved (20 Mrad)

SwitcherB
Row control

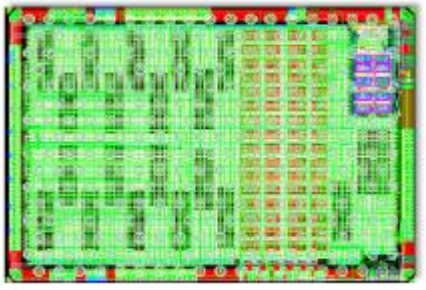


AMS/IBM HVCMOS 180 nm
Size 3.6×1.5 mm^2
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

PXD

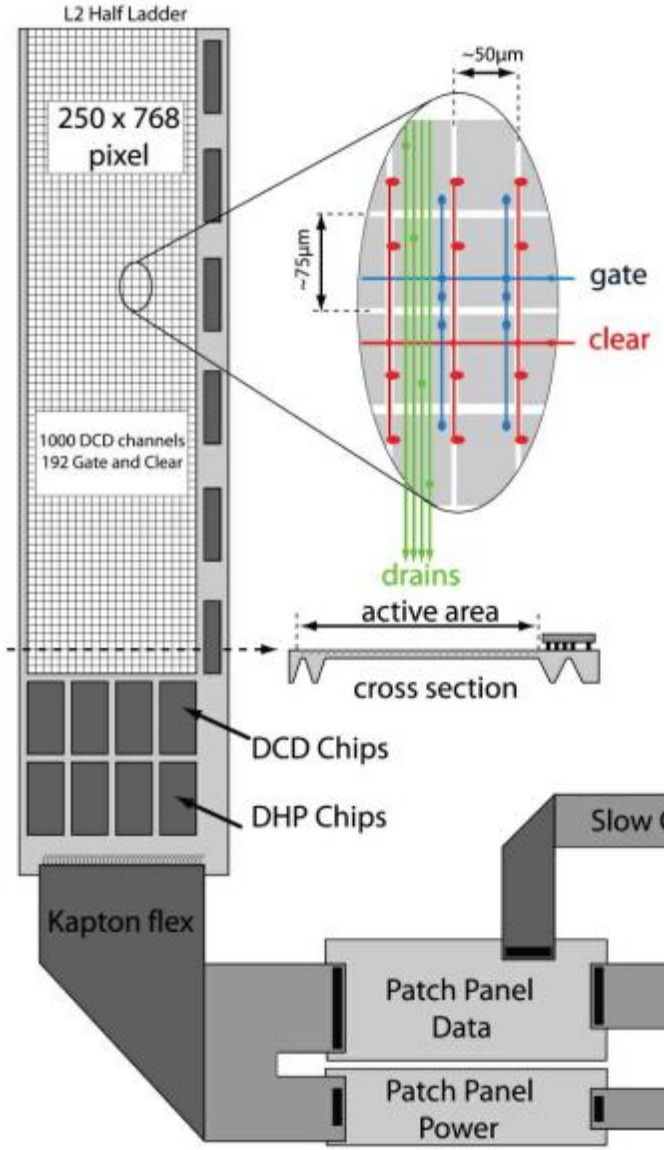


DHP (Data Handling Processor)
First data compression



TSMC 65 nm
Size 4.0×3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

Off-module Data Flow

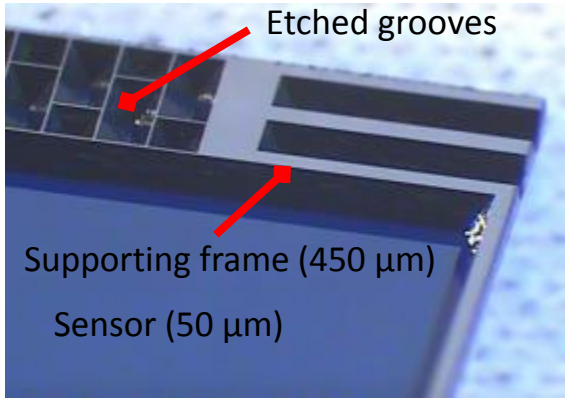


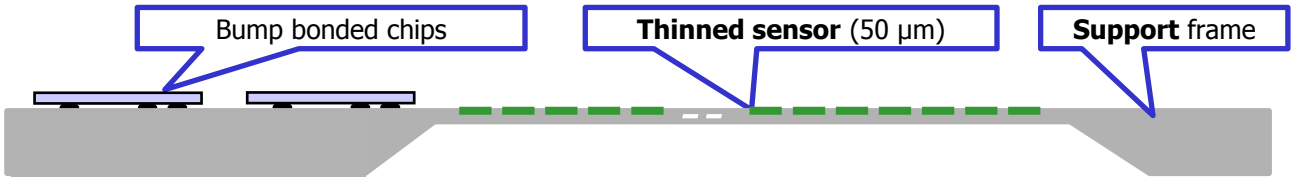
- **DHH** (Data Handling Hybrid)
  - Electrical - optical interface
  - Slow control master (JTAG)
  - Clustering
- **ONSEN**
  - Data buffer
  - Reduction via ROI selection (DATCON, HLT)

Thin DEPFET Sensors

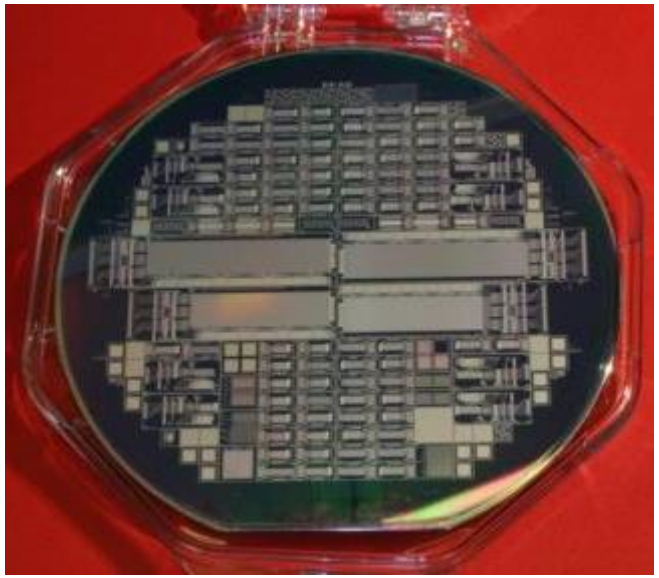
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

- One material: uniform and small thermal expansion
- The DEPFET thickness is a free adjustable parameter

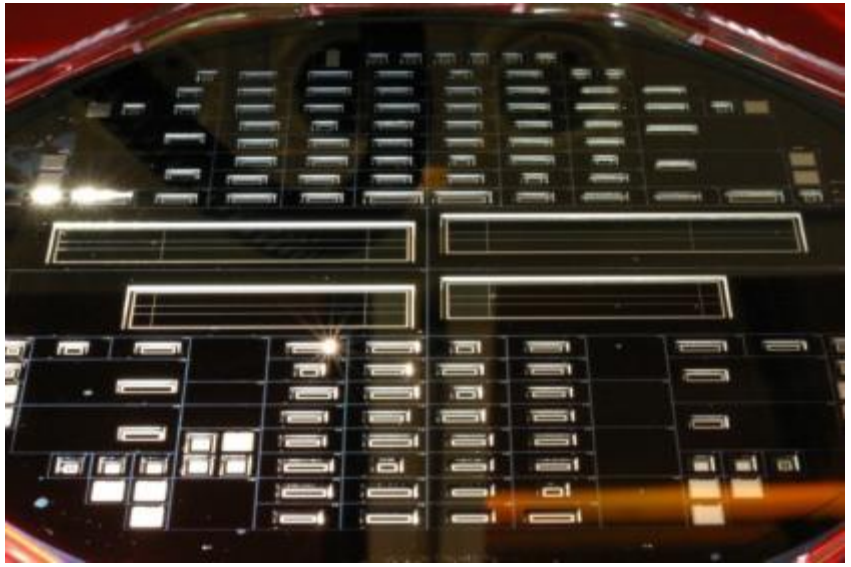


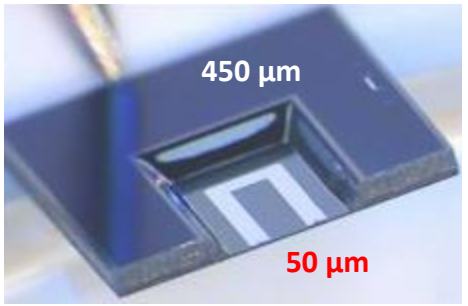


PXD6 Prototype Production



8 SOI wafers with 50 µm thin sensors (450 µm handle)
- Small test matrices with design variations
- Full size sensors for prototyping

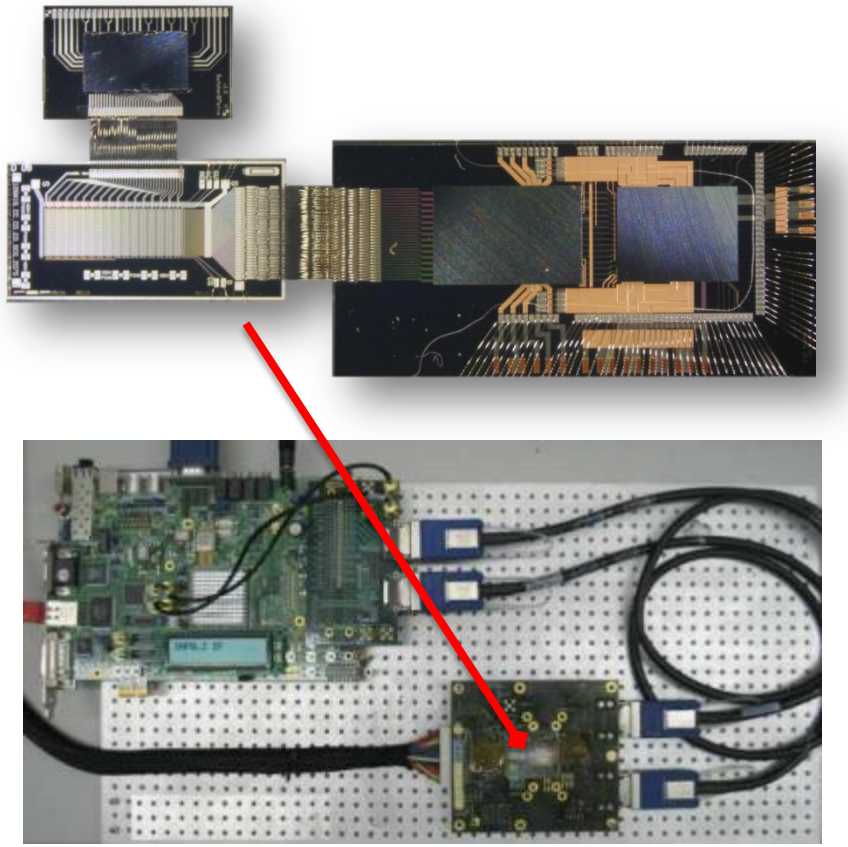


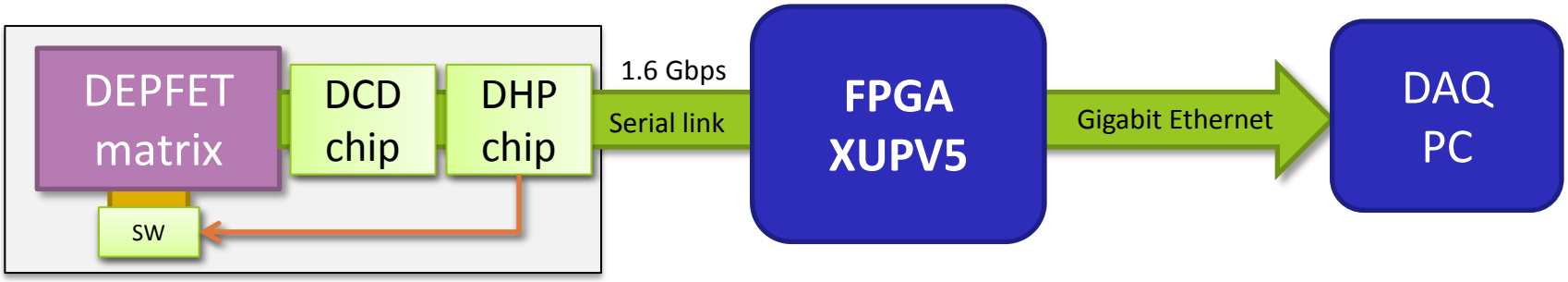


90 steps fabrication process:
- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- 1 Copper layer
- Back side processing

Hybrid 5.0 - Full System Test

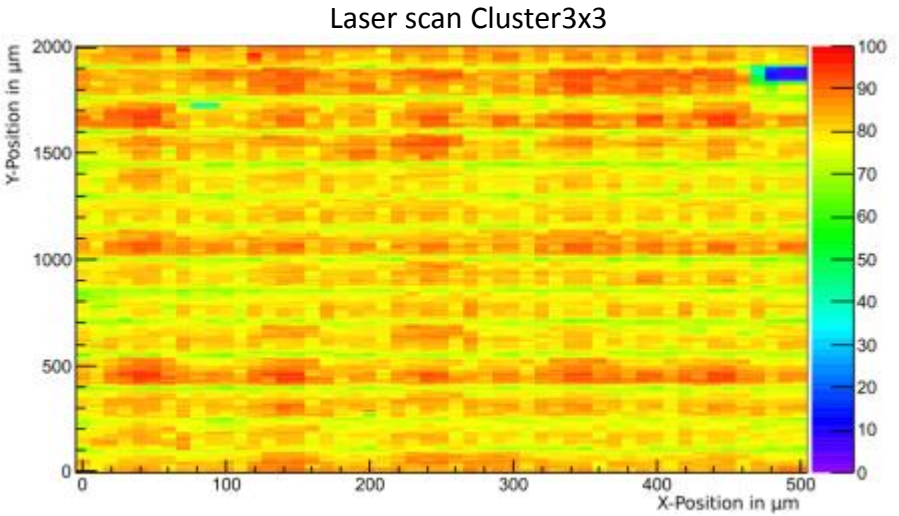
- Zero suppressed readout with the minimum necessary amount of components:
  - One Switcher-B
  - One DCDBv2
  - One DHP 0.2
  - Small thin matrix: Belle II SD PXD6 type, 16x128 pixels, 50x75 µm² pitch



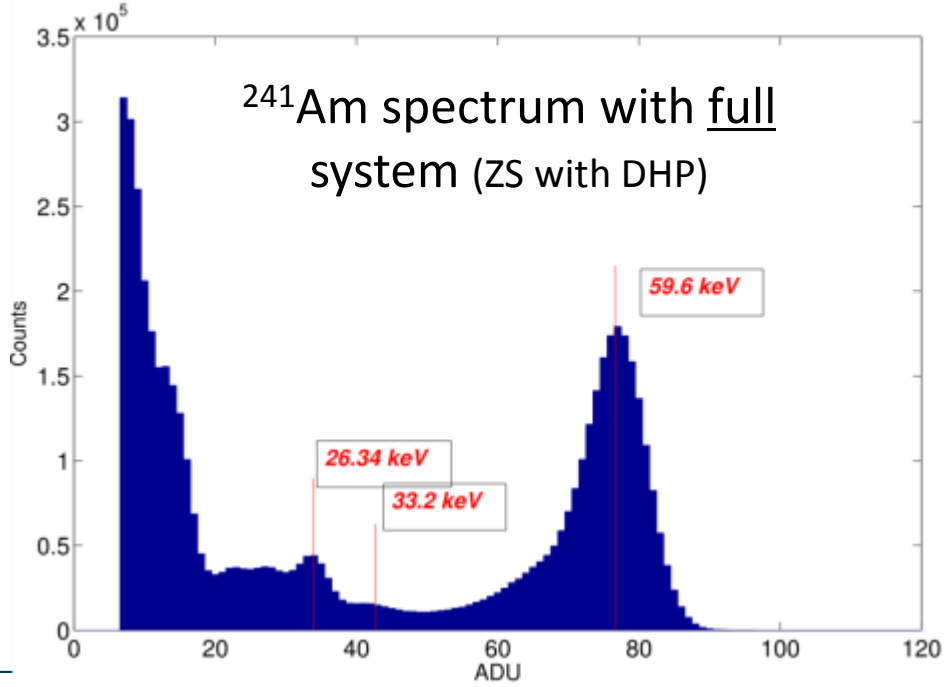


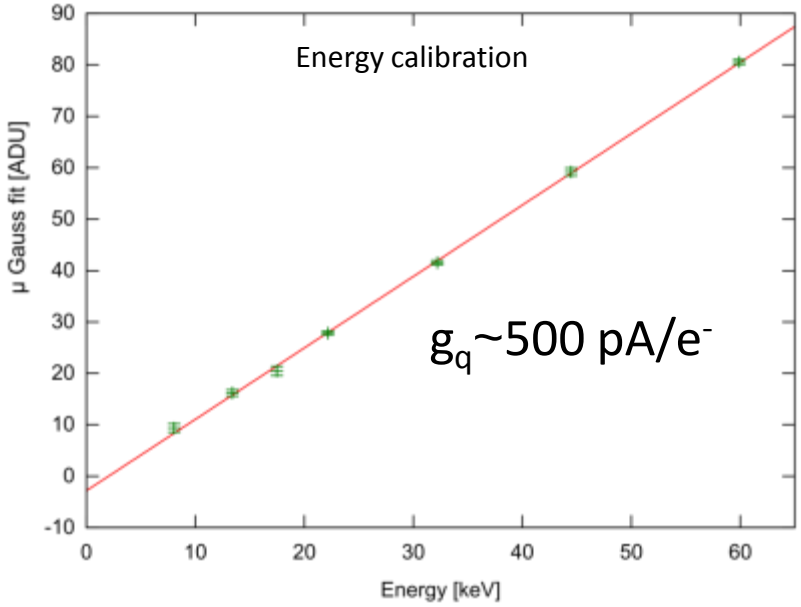
DEPFET Sensor Characterization

- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
  Charge collection homogeneity
  In pixel studies
- Radioactive source
  System calibration



Homogeneous charge collection





Beam tests

- DEPFET PXD6 extensively tested over the last campaigns
  120 GeV pions at CERN-SPS
  1-5 GeV electrons at DESY
  Magnetic field

- Sensor properties
  Charge collection homogeneity, operating points, efficiency, angular scans
  Various pixel sizes, gate lengths, clear structures, drift regions and pixel designs

- System related aspects
  Power supply prototypes
  DHH and ONSEN readout

Here, just an appetizer

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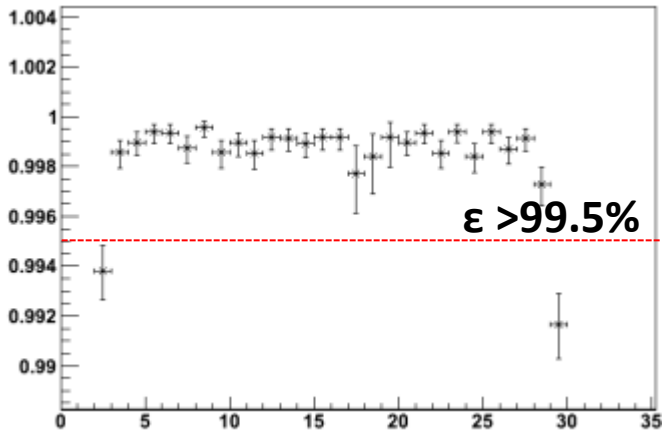
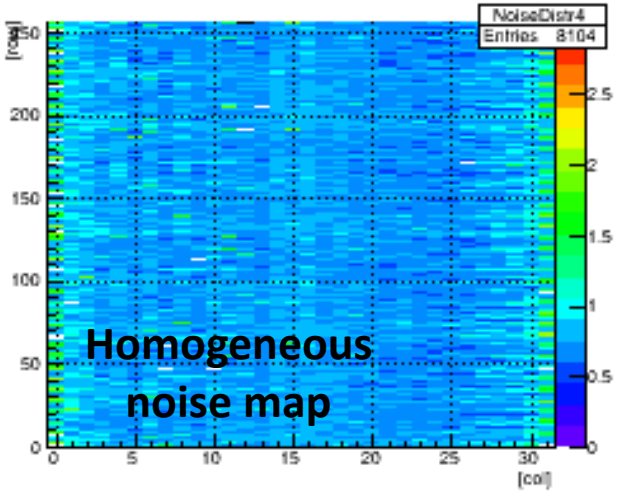
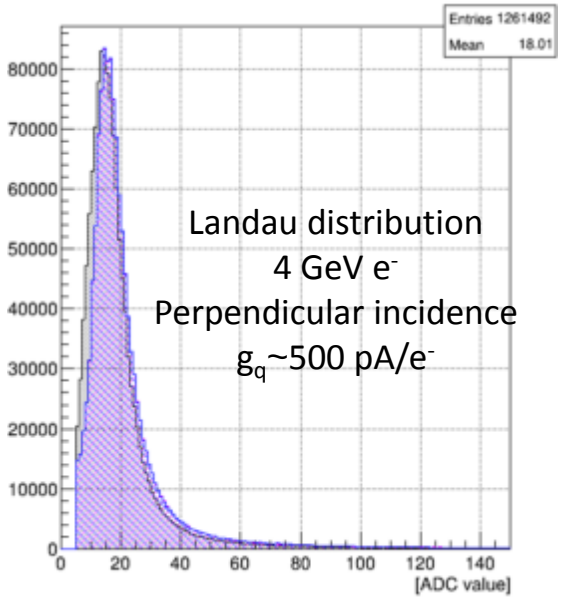
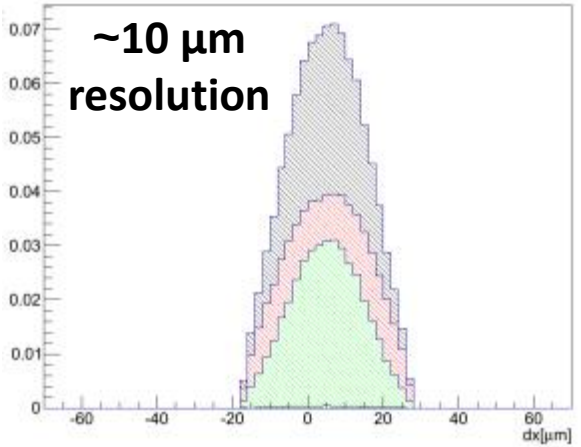
Summary Test Beam Campaigns

PXD6 Belle II design
Thin **50** µm sensor
Pitch 50x75 µm²
Targeted speed readout









Prove of principle demonstrated in many test beam campaigns over the past years

Latest Test Beam Campaign – Jan2014

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- PXD+SVD common test beam in January 2014
- Small sector of the close to final prototype detectors and ASICs
  PXD half ladder + 4 SVD single module layers
- Readout using the complete DAQ chain
- CO_2 cooling, slow control, environmental sensors
- Alignment, tracking algorithms, ROI with B=1 Tesla

- **Goal**: **System integration test**

Test Beam Setup

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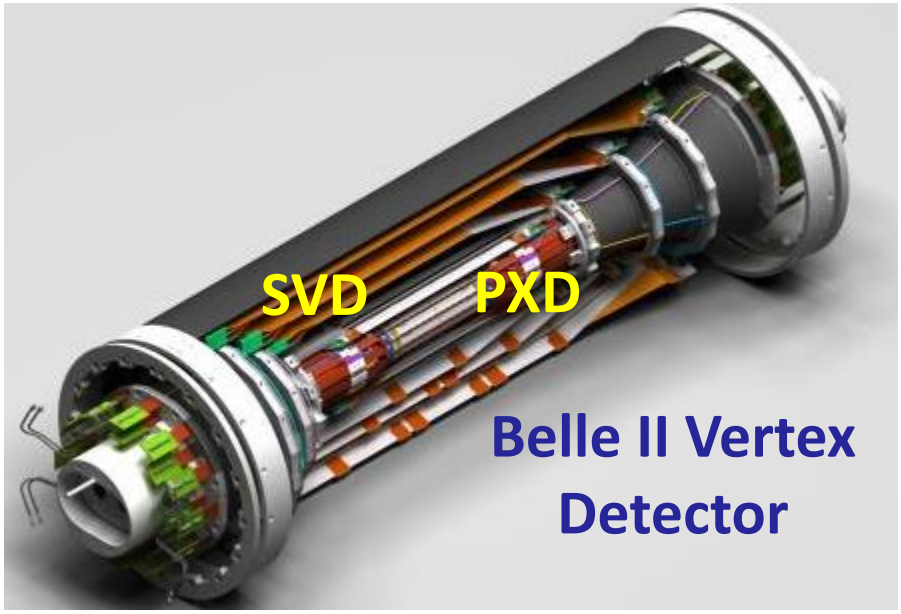
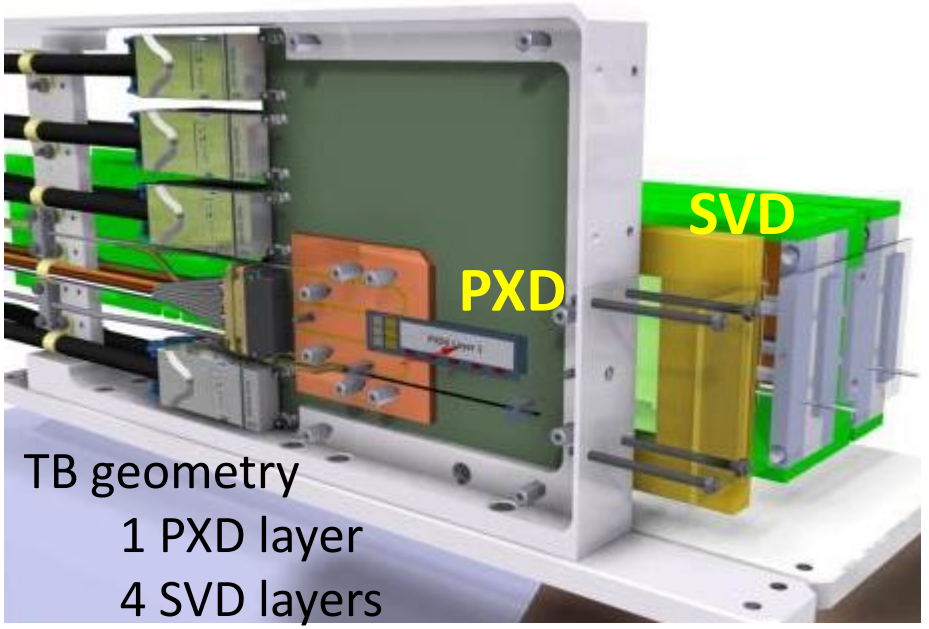
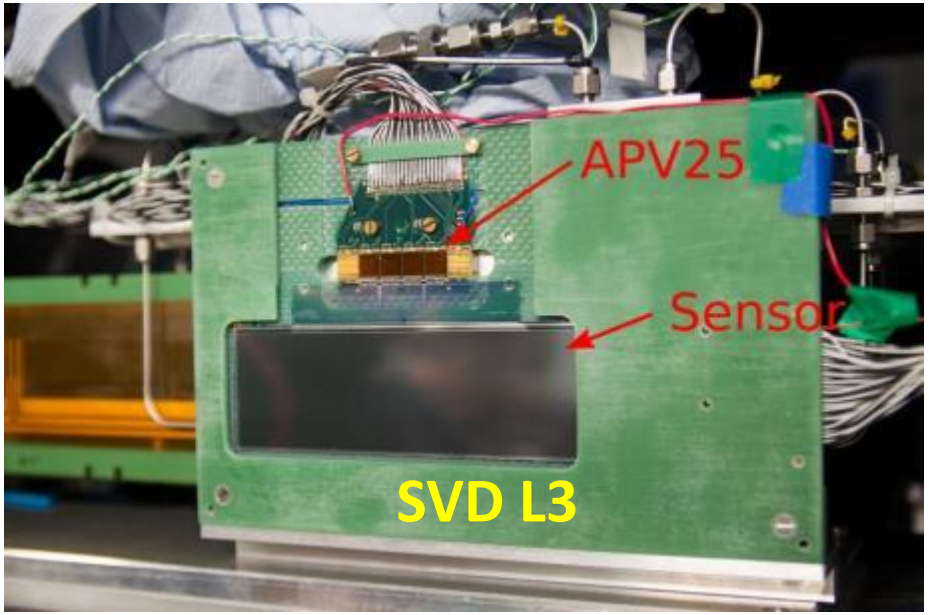
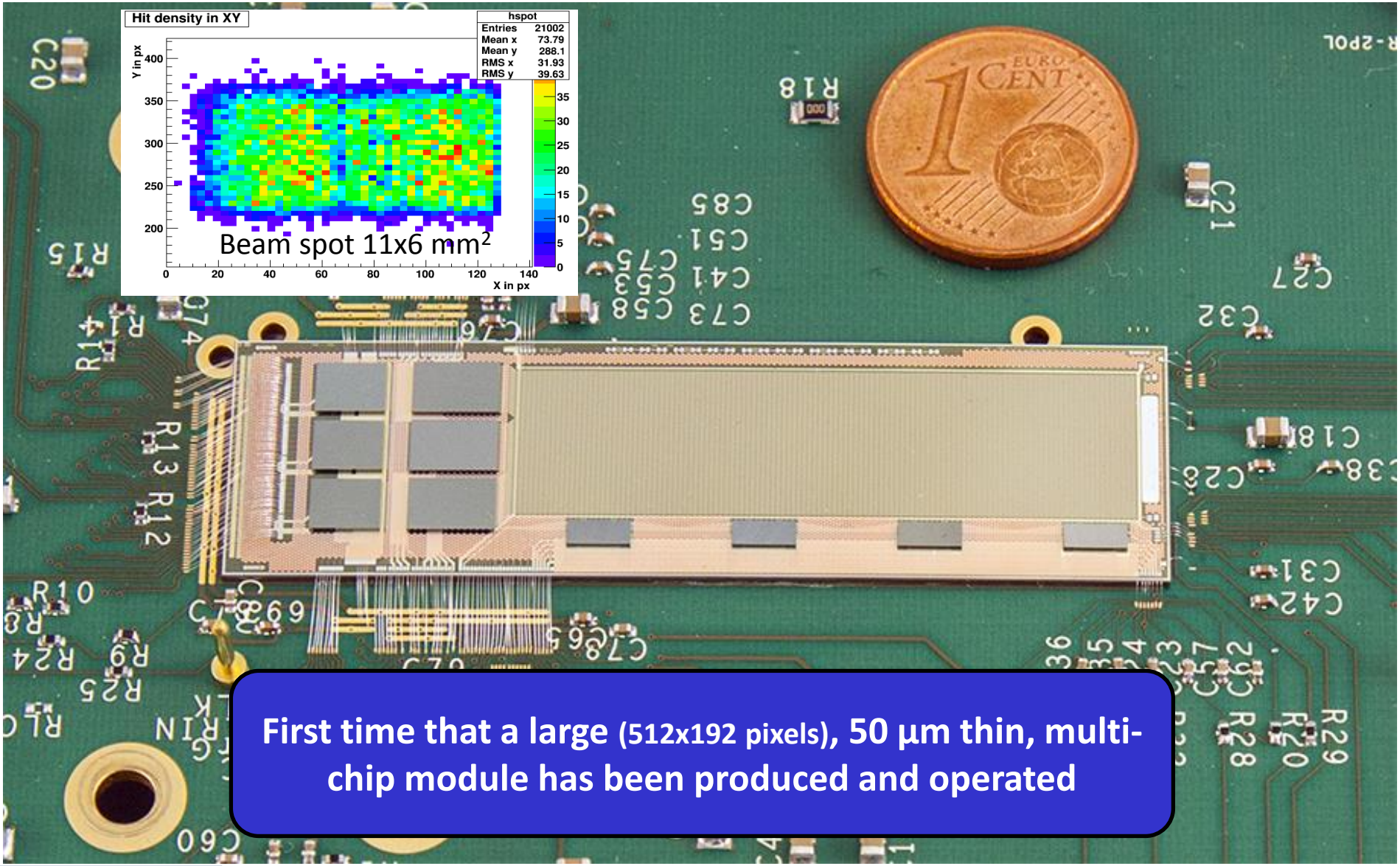




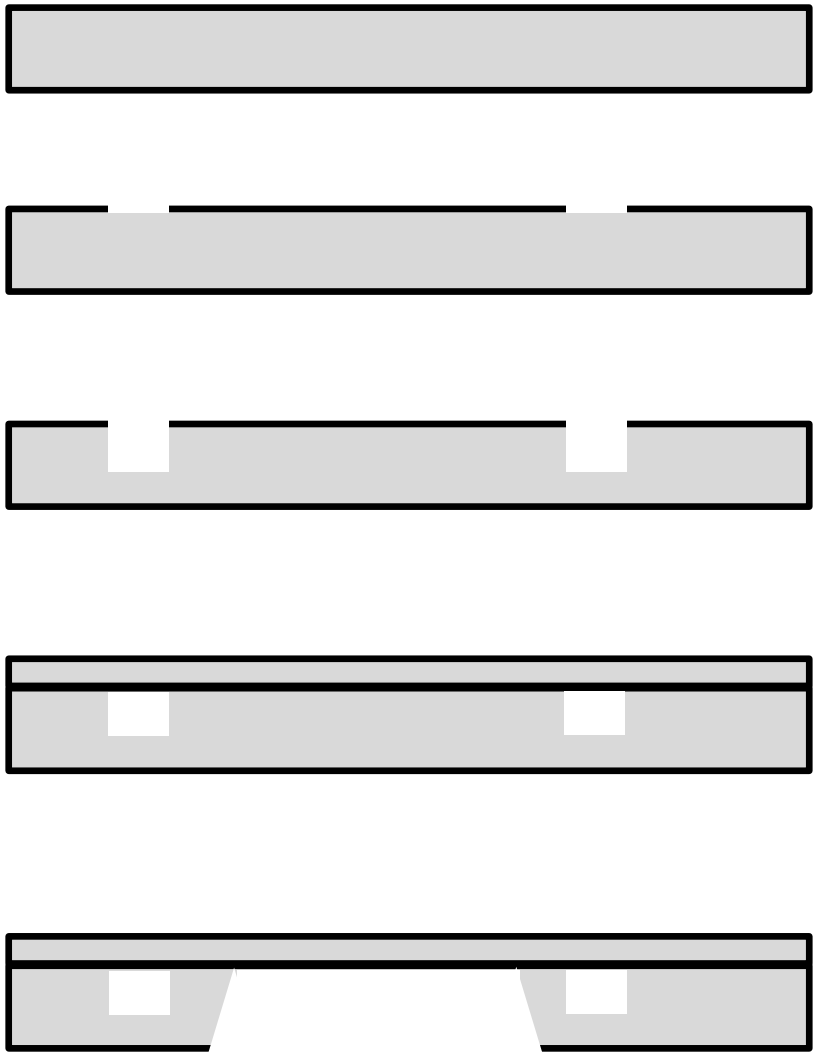


Thin Multichip Module



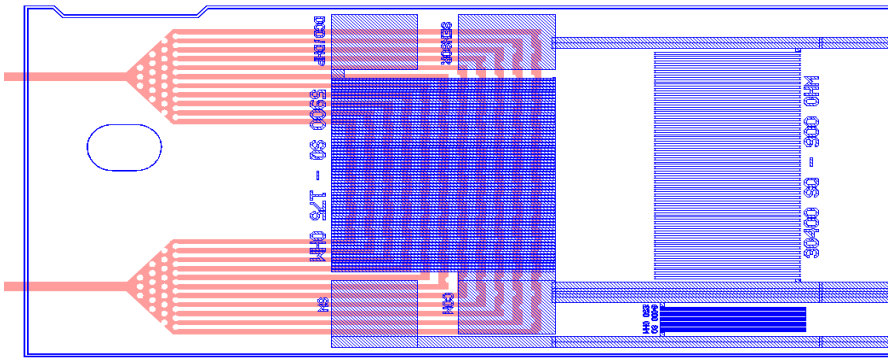
First time that a large (512x192 pixels), 50 µm thin, multi-chip module has been produced and operated

Micro-channel Cooling for ILC

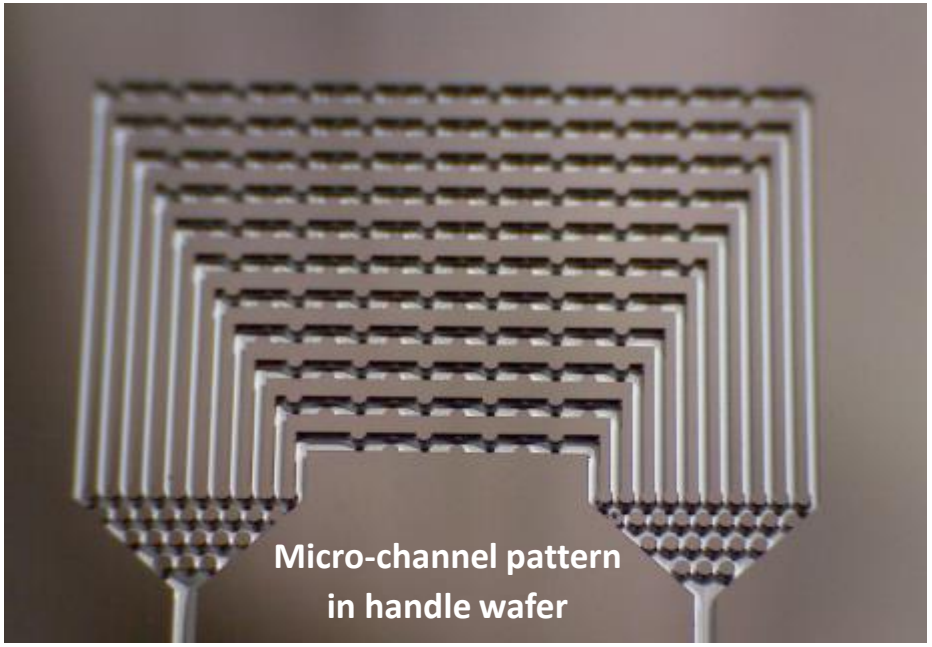


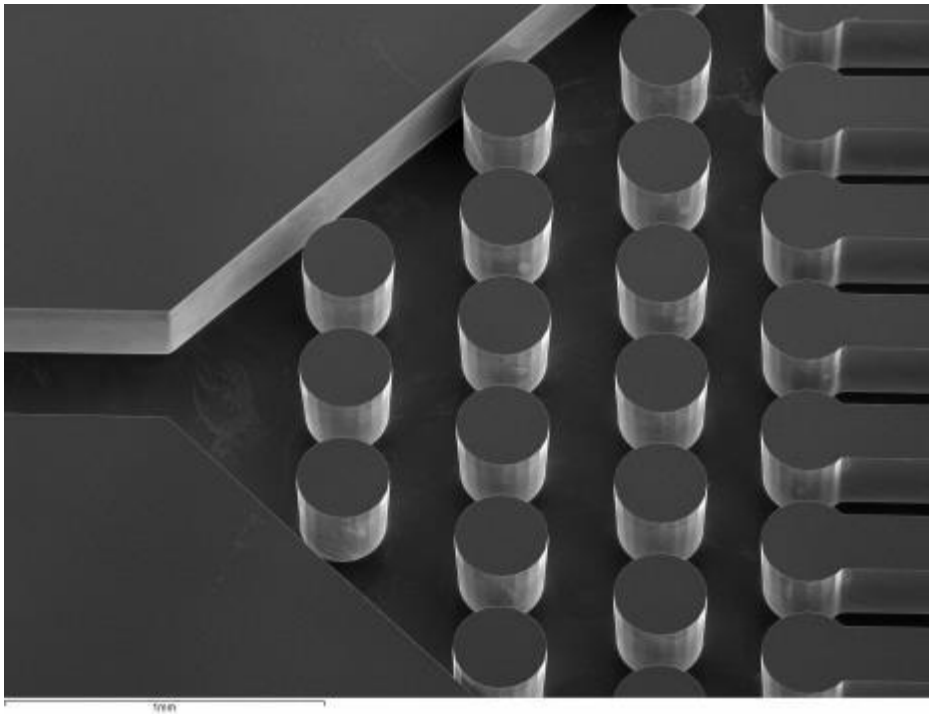
- Start with oxidized handle wafer
- Define lithographically µ-channels, etch oxide
- Etch micro-channels, blind via
- Bond prepared top wafer as usual
- Finish SOI wafer (“Cavity SOI”)
- top wafer for DEPFETs
- Handle wafer with µ-channels under ASICs
- Handle removed in sensitive area
- Channels exposed after cutting

MCC: The Realization



Aluminum layer with surface resistor
to mimic the ASICs power dissipation





Inlet and outlet: 350 µm deep, 400 µm wide

Mechanical Samples

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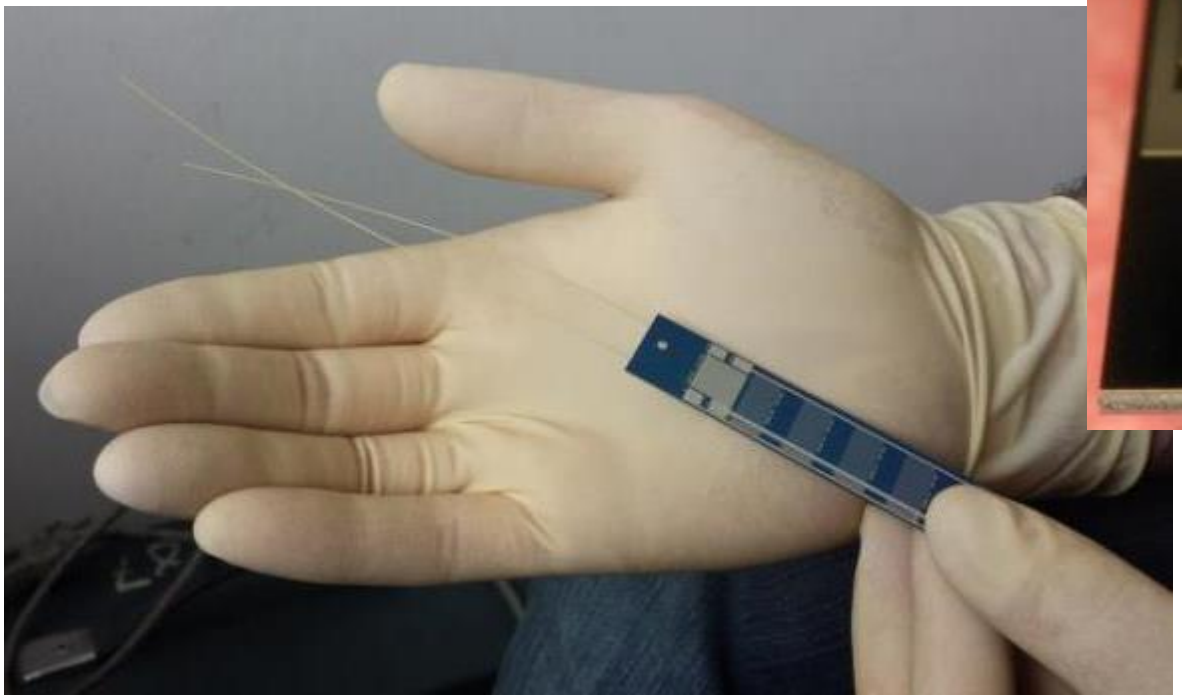
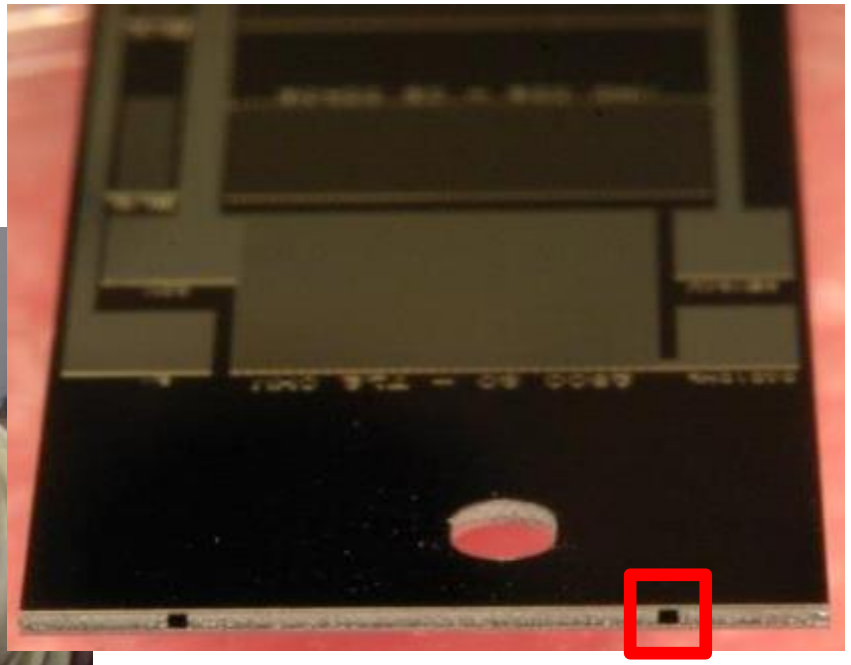
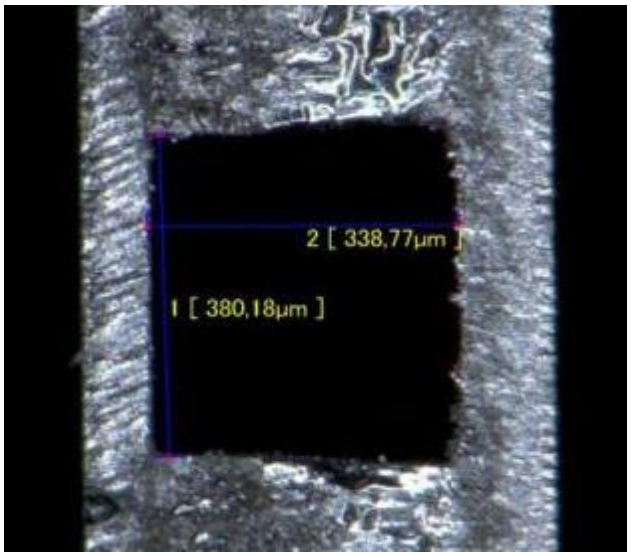
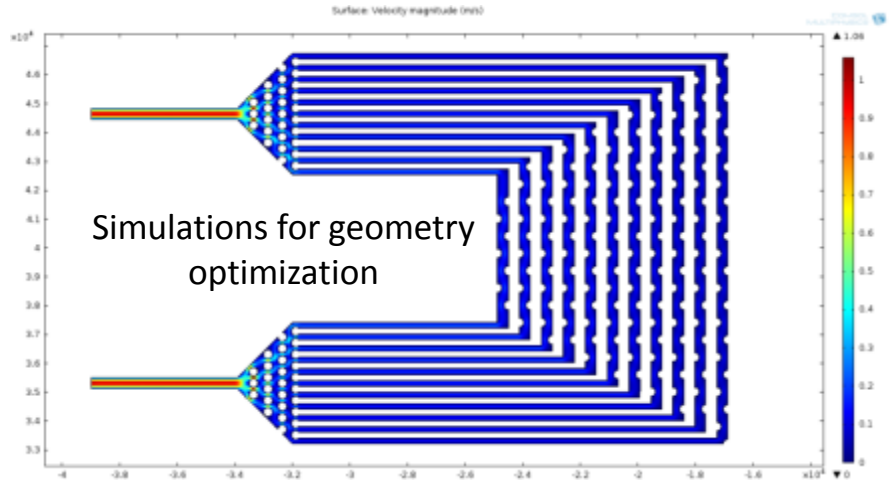
360 µm PEEK pipes

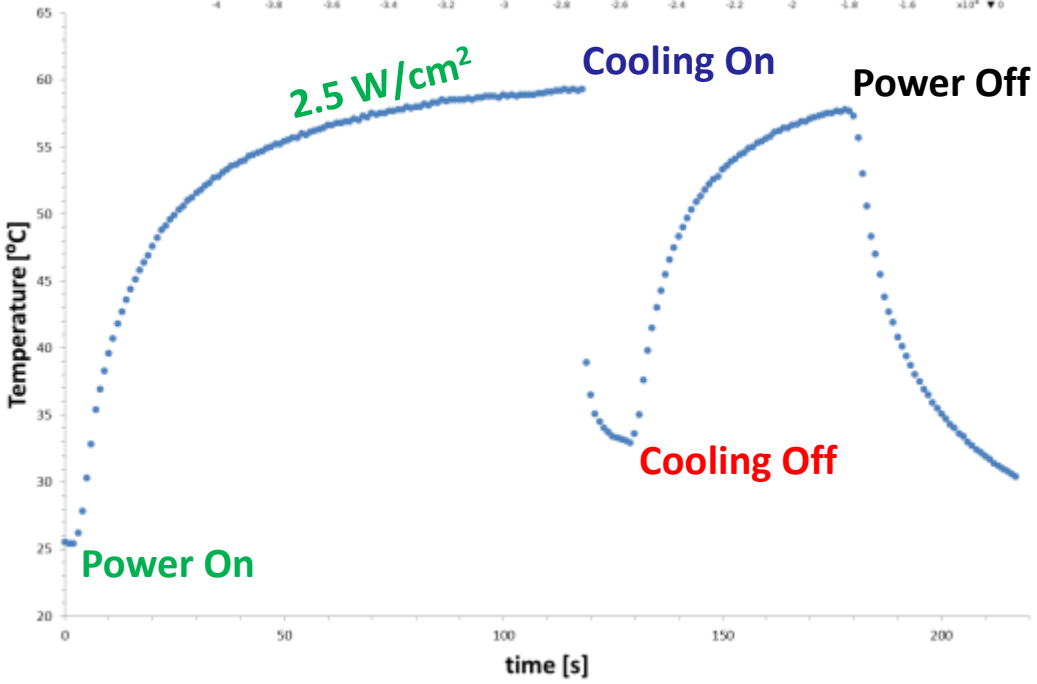


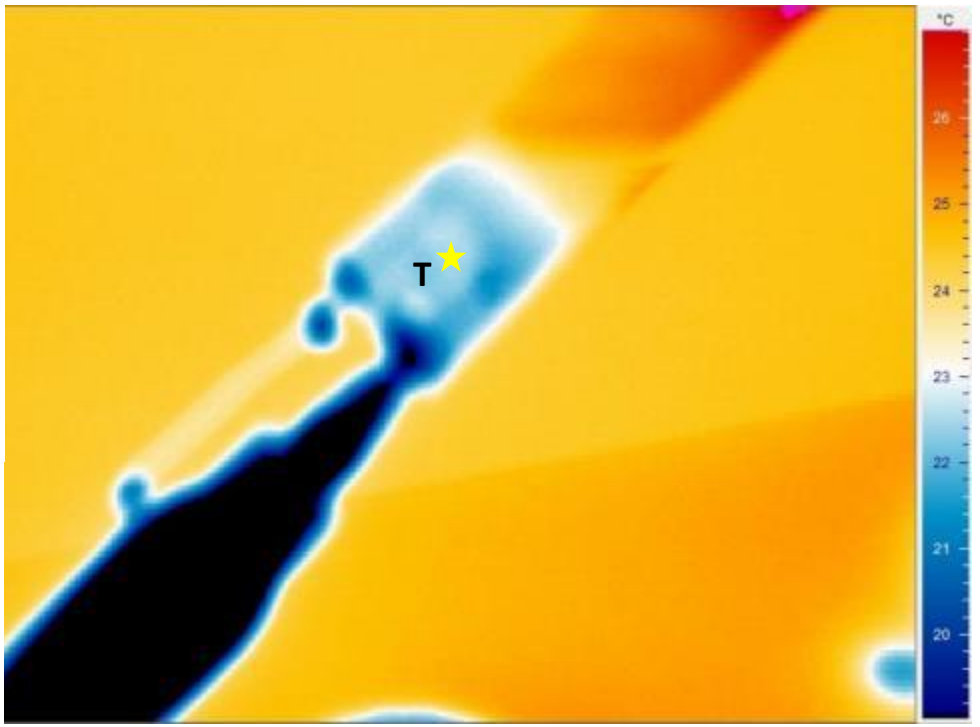




Coolant Flowing







- Mass flow= 0.1 l/h (2.5 bar)
- Water at room temperature

Proof of principle demonstrated!

Summary

- The DEPFET Collaboration is developing utra-transparent pixel sensors with integrated amplification

- The good performance of the DEPFET detector system in terms of SNR, spatial resolution, readout speed is demonstrated

- The Belle II PXD boosted the development of DEPFET detectors
  → Direct benefit towards the ILC-VXD project (ILD-VXD layer concept '*engineered*')

- Building a real system: Every detail (although not covered here) is being considered
  → Cooling, mechanics, DAQ, …

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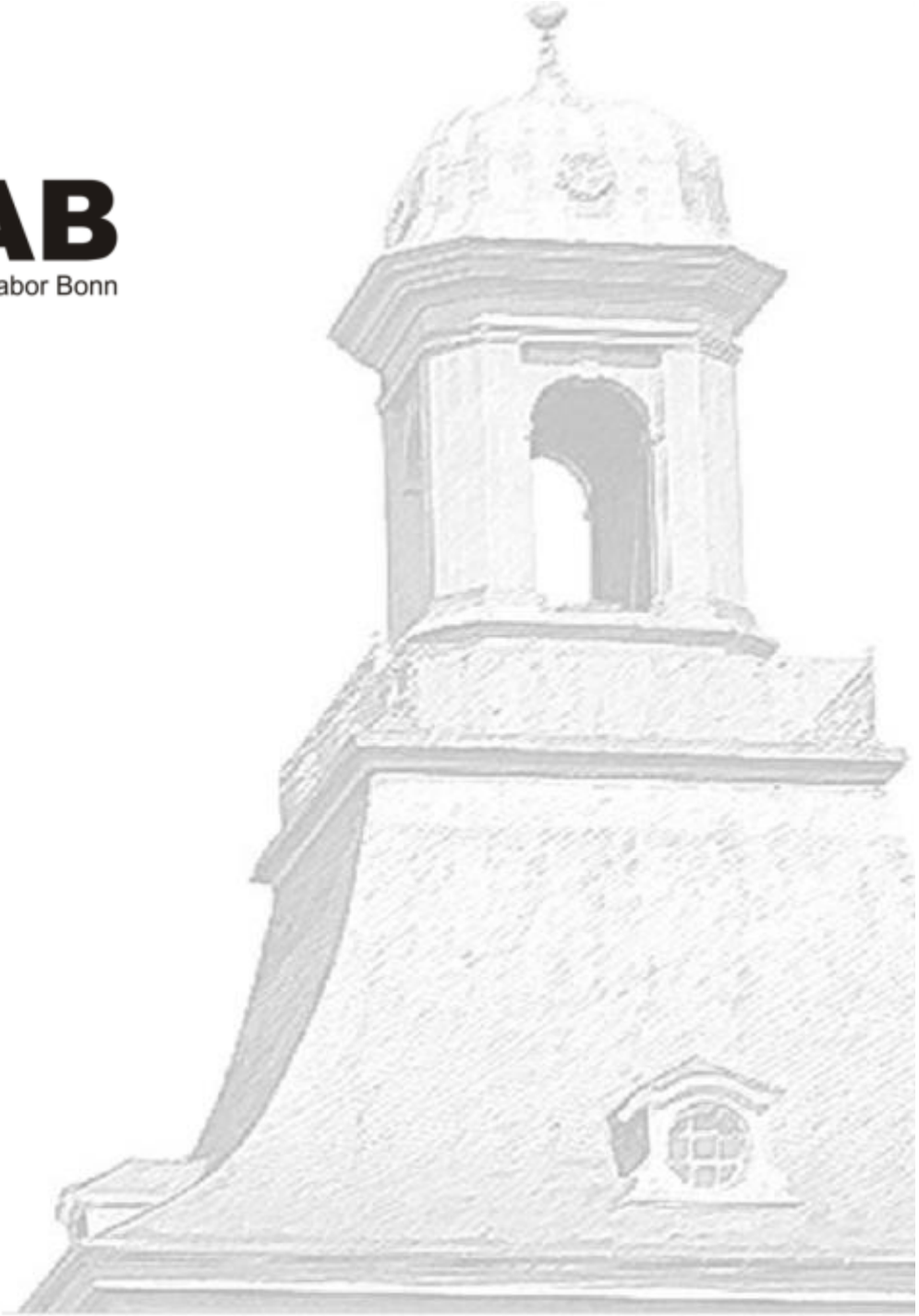

Thank you

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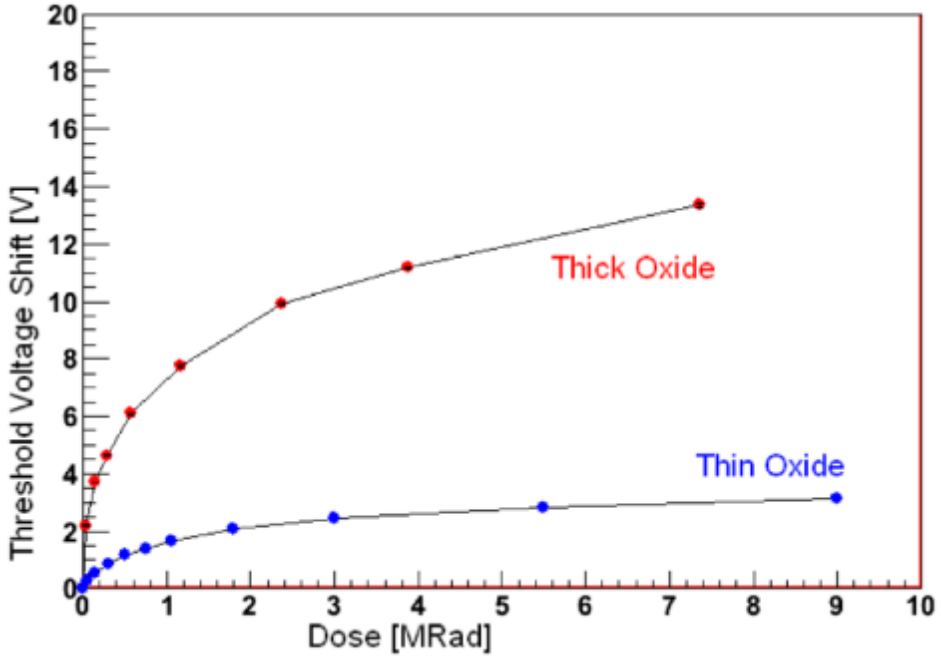
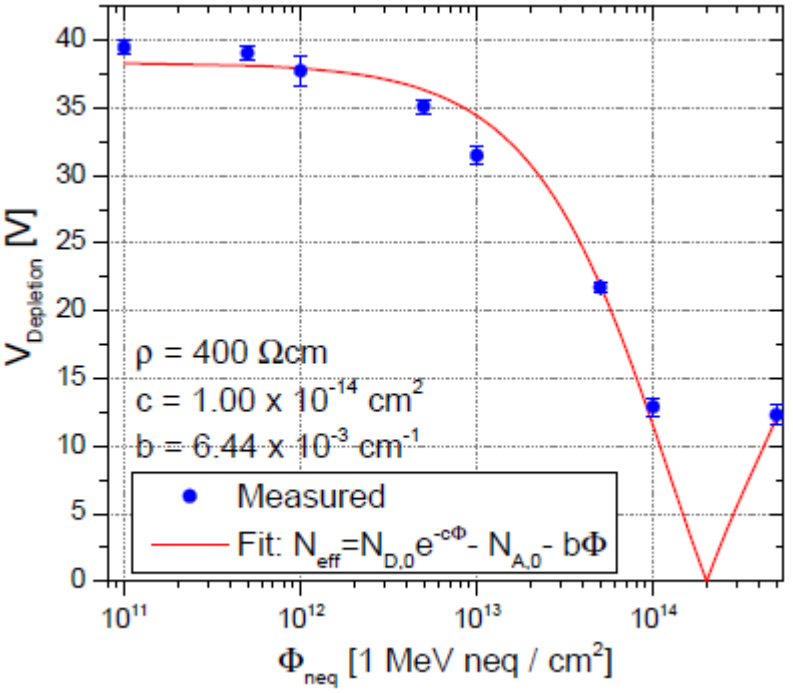
Radiation Damage in DEPFETs

- Surface damage



- Bulk damage



Electric Multichip Module (EMCM)

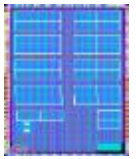
E-MCM: Everything <u>but</u> the DEPFET

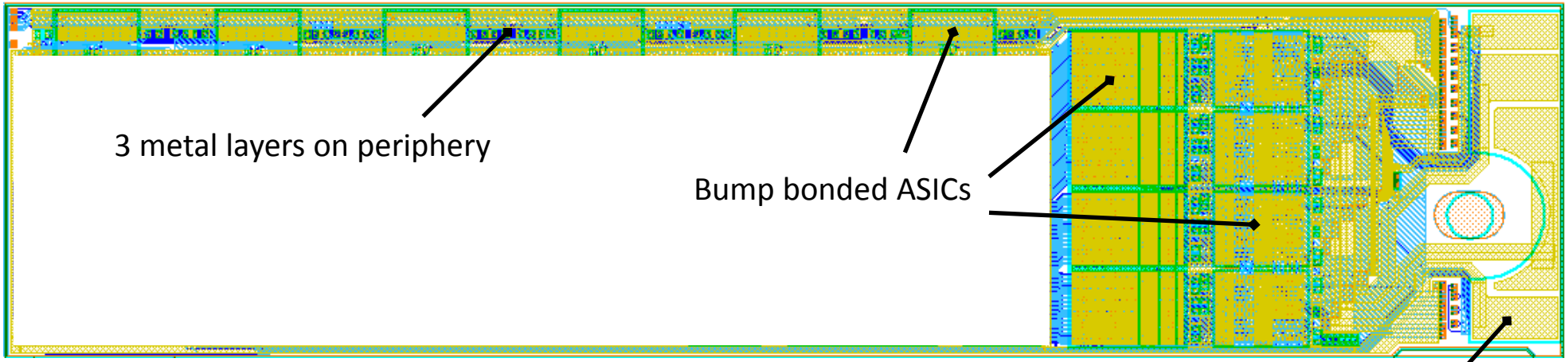
Electrically active prototype of a half ladder

SW

DCD

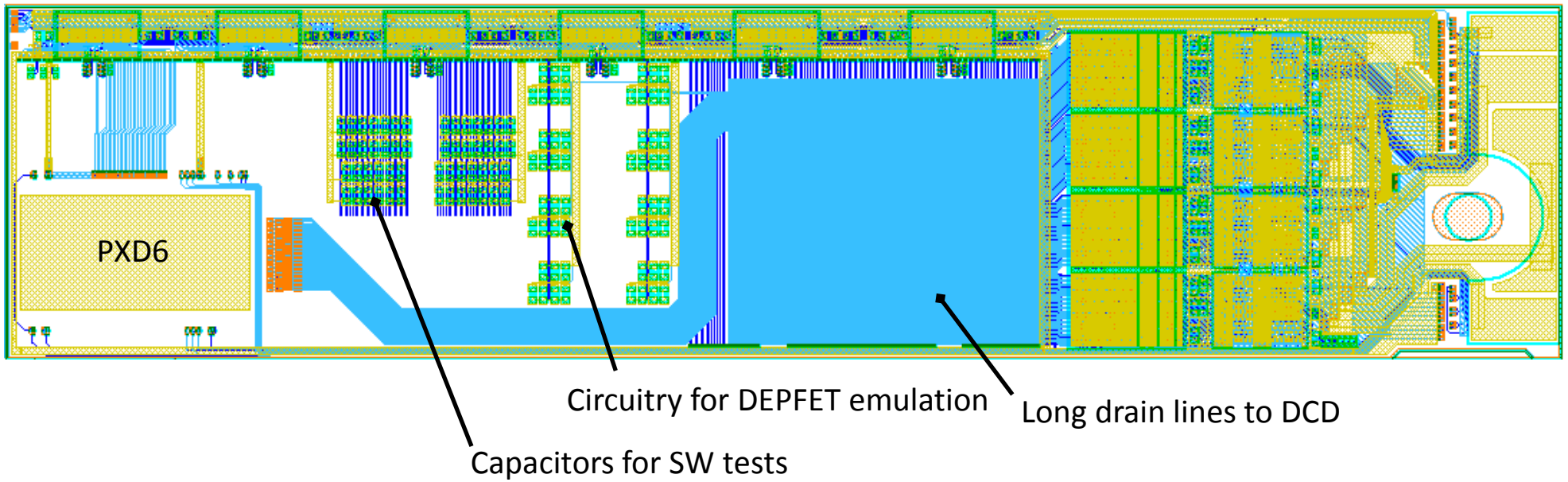
DHP





Electric Multichip Module (EMCM)

E-MCM: Everything <u>but</u> the DEPFET
Electrically active prototype of a half ladder



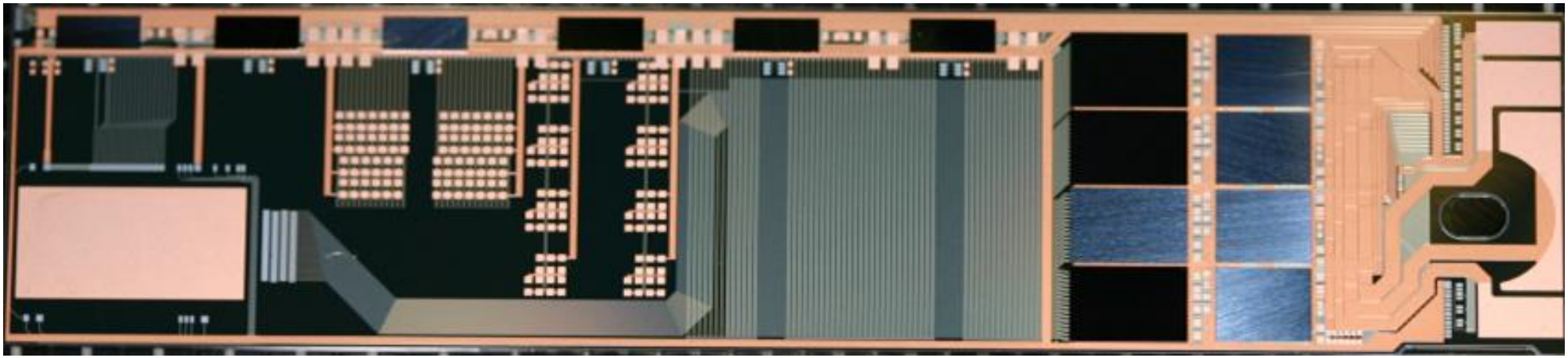
- Study and characterization of routing and electronic components
- Understanding of the technological feasibility of the 3-metal layers
- Practice flip-chipping and off-module interconnections

Electric Multichip Module (EMCM)

universitätbonn

E-MCM in reality

→ **Modules produced, tested, ASICs flip chipped and Kapton attached**

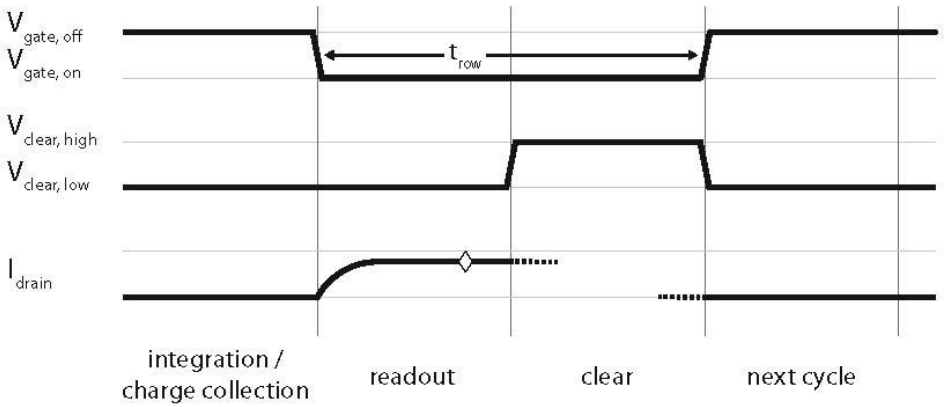


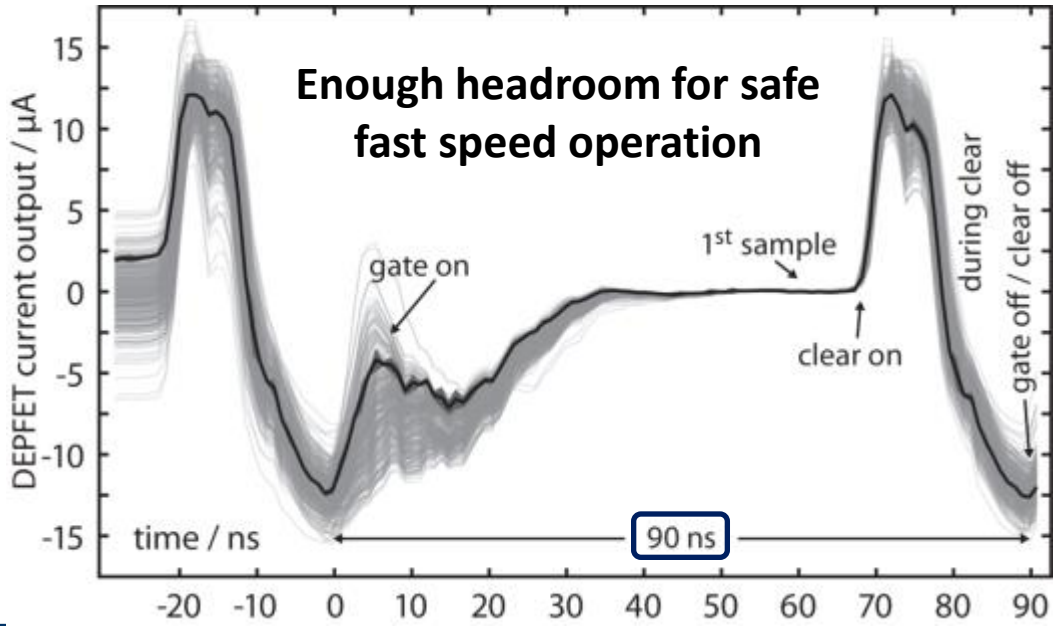
Electrical Properties under investigation

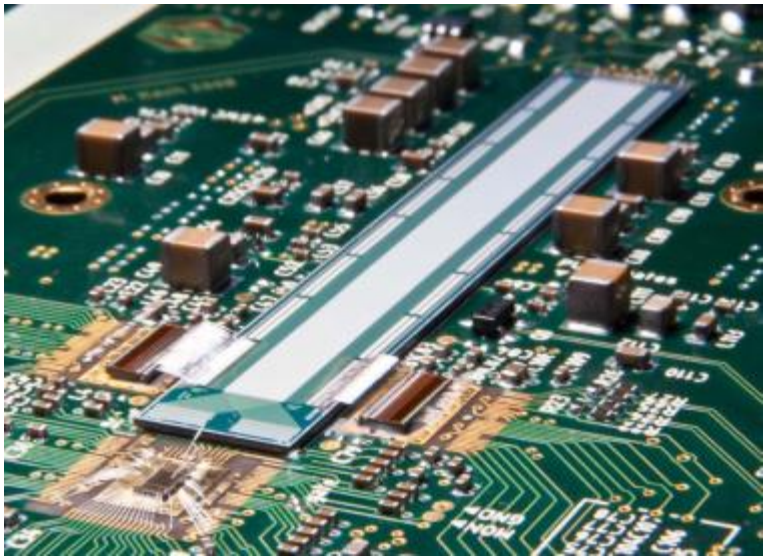
- Switchers working properly
- Communication with DCDs and DHPs

DEPFET Readout Speed

- DCD dynamic measurements
  Readout speed with single sampling
- Belle II PXD frame readout: 20 µs
  (50 KHz frame rate)
- Read-clear cycle: **100 ns**
  (768 rows, 4 fold readout)



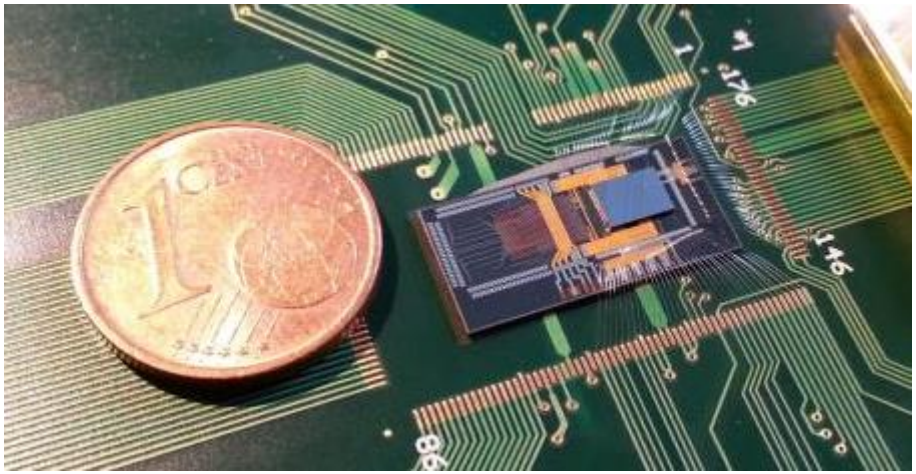




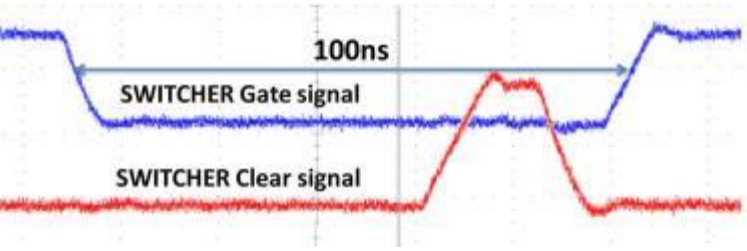
Long drain lines ~ 60 pF parasitic capacitance

DHP Functionality

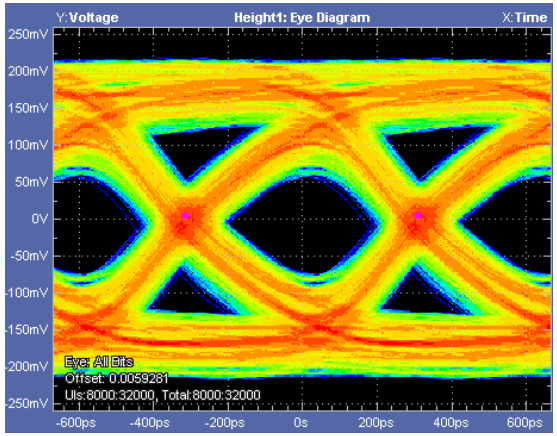
- Functionality tests
  - High speed link
  - Configuration and communication with DCD
  - Data processing
- Switcher output sequences

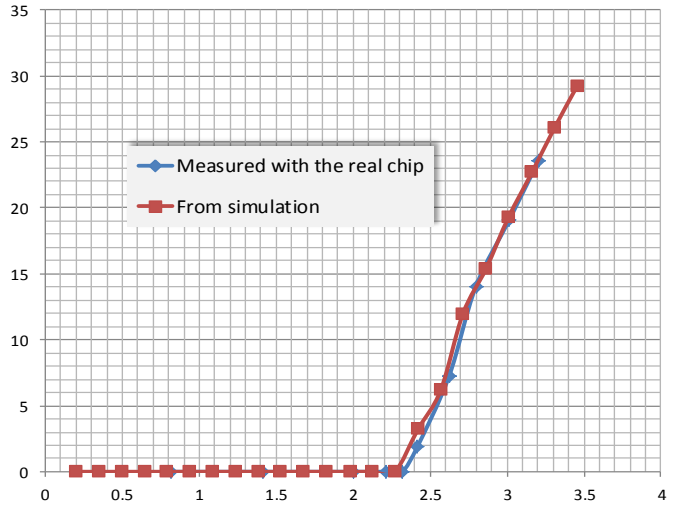


Steering Signal Output

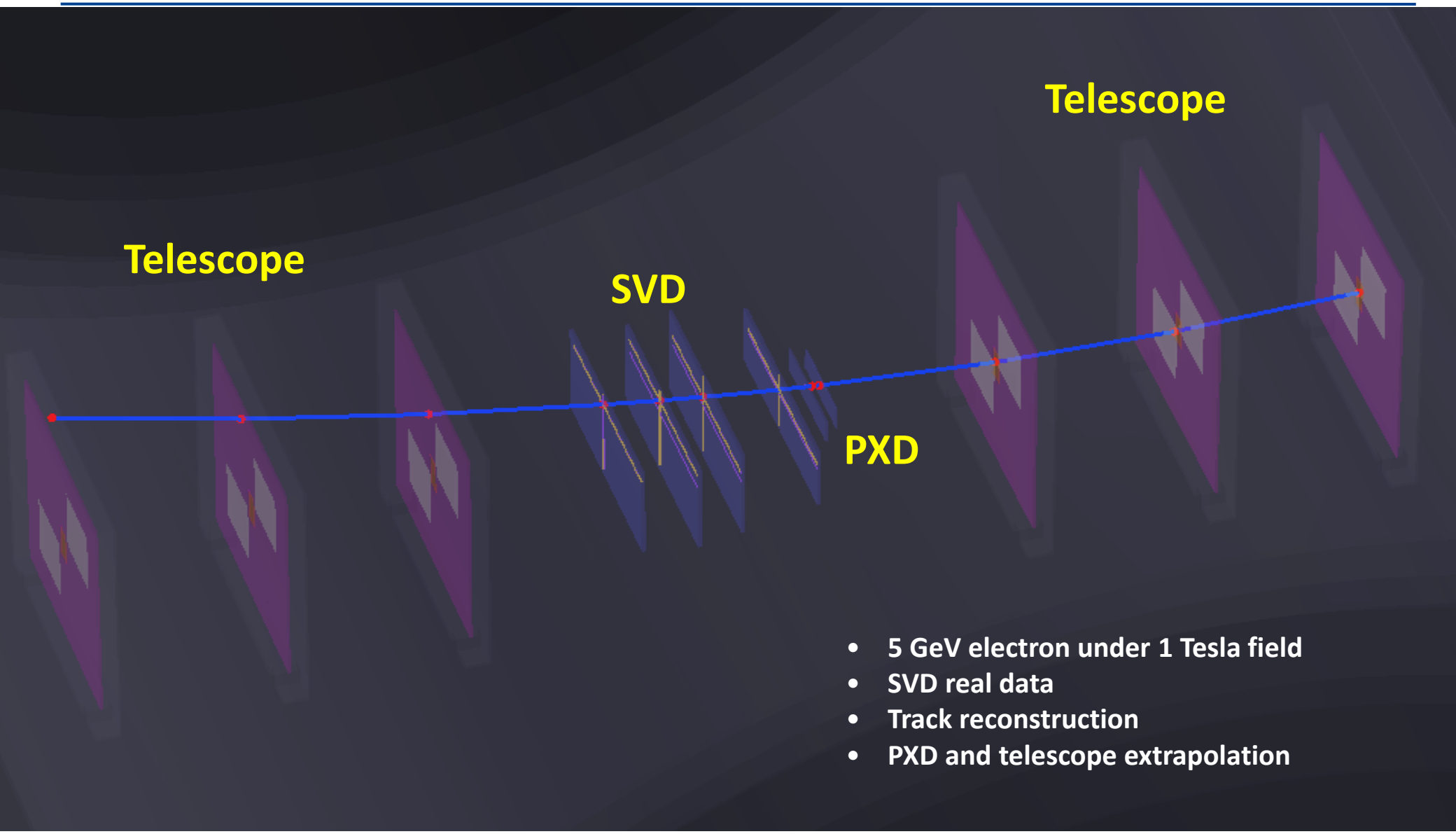


Eye Diagram after 15m Cable



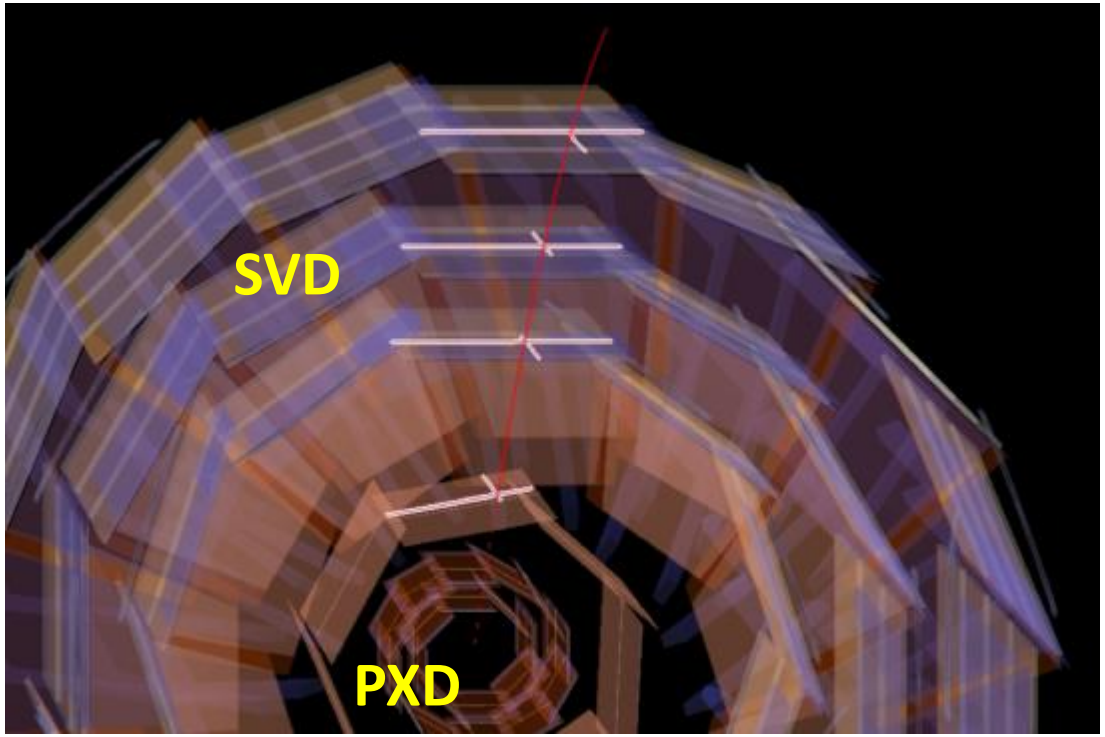


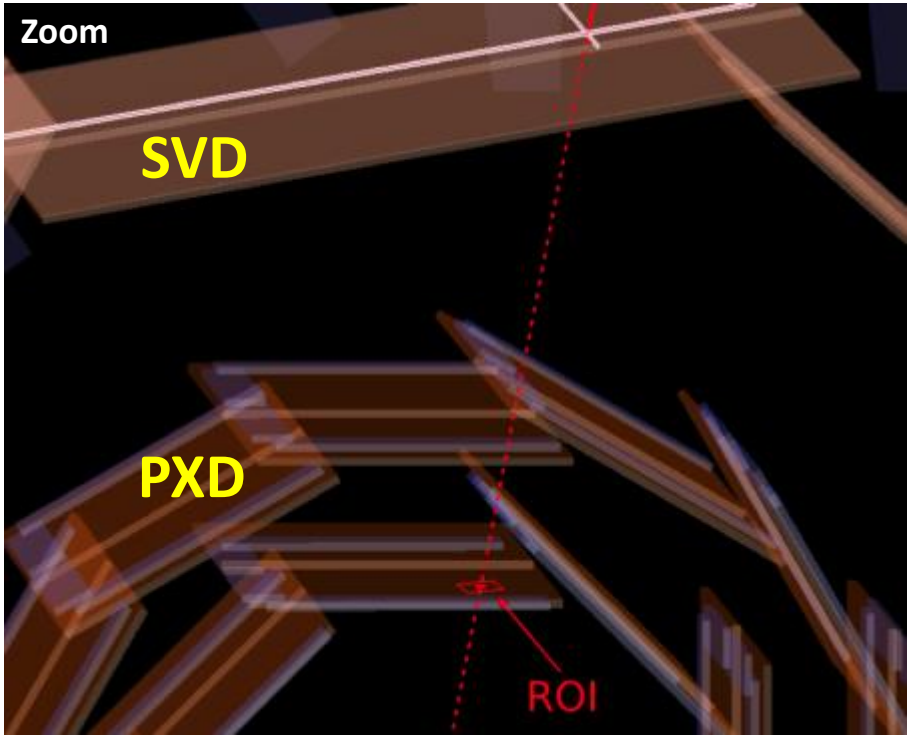
Event Display



- 5 GeV electron under 1 Tesla field
- SVD real data
- Track reconstruction
- PXD and telescope extrapolation

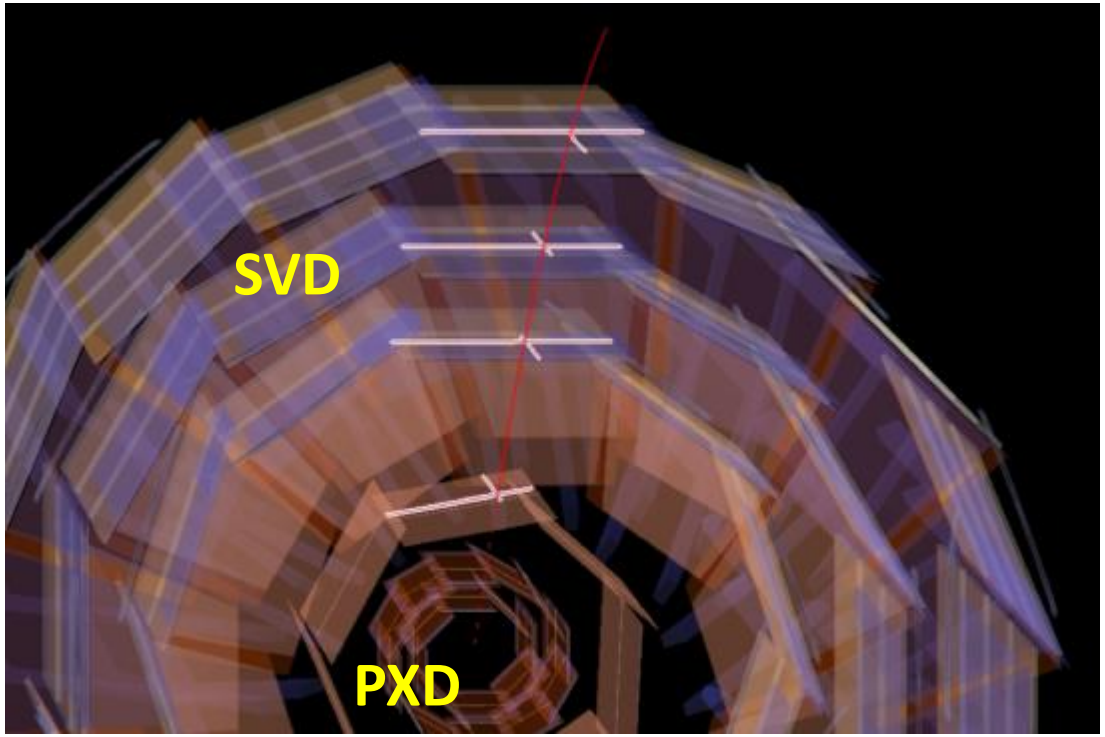
PXD Data Reduction

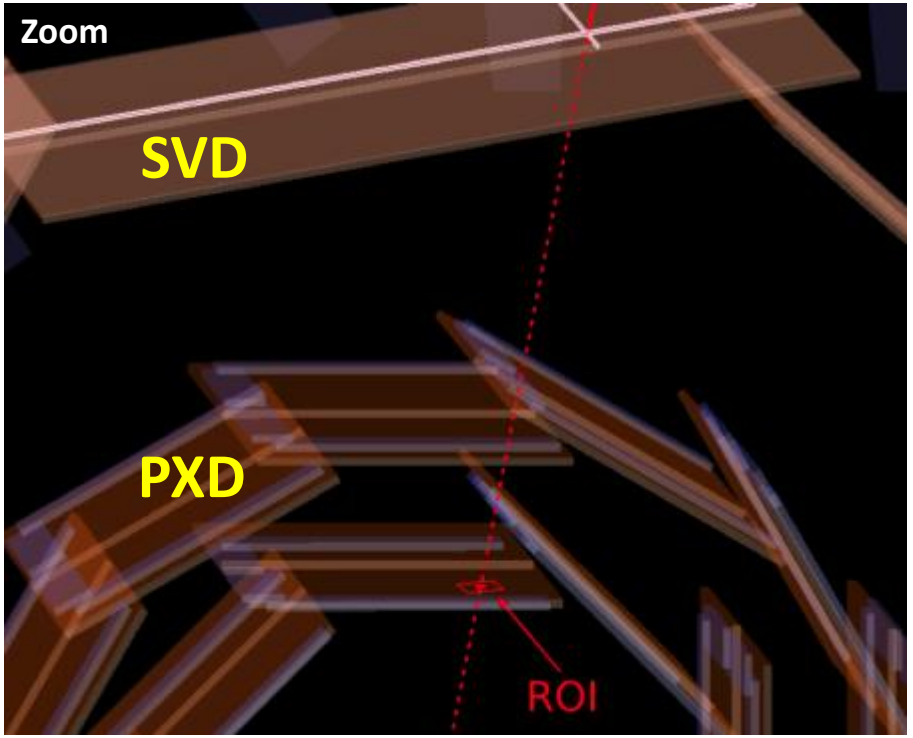




- Expected maximum occupancy 3%
- Total data rate >20 GB/s after zero suppression
- Data reduction (factor ≥10) needed for data storage
- Solution: region of interest (ROI) by track extrapolation from the outer detectors

PXD Data Reduction





- Expected maximum occupancy 3%
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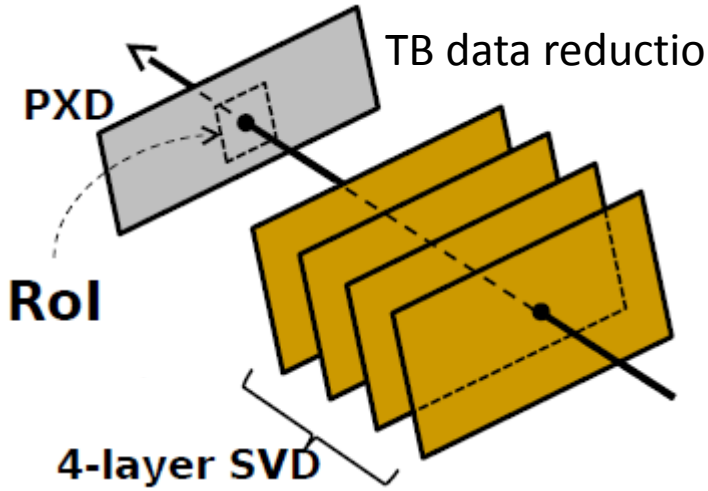
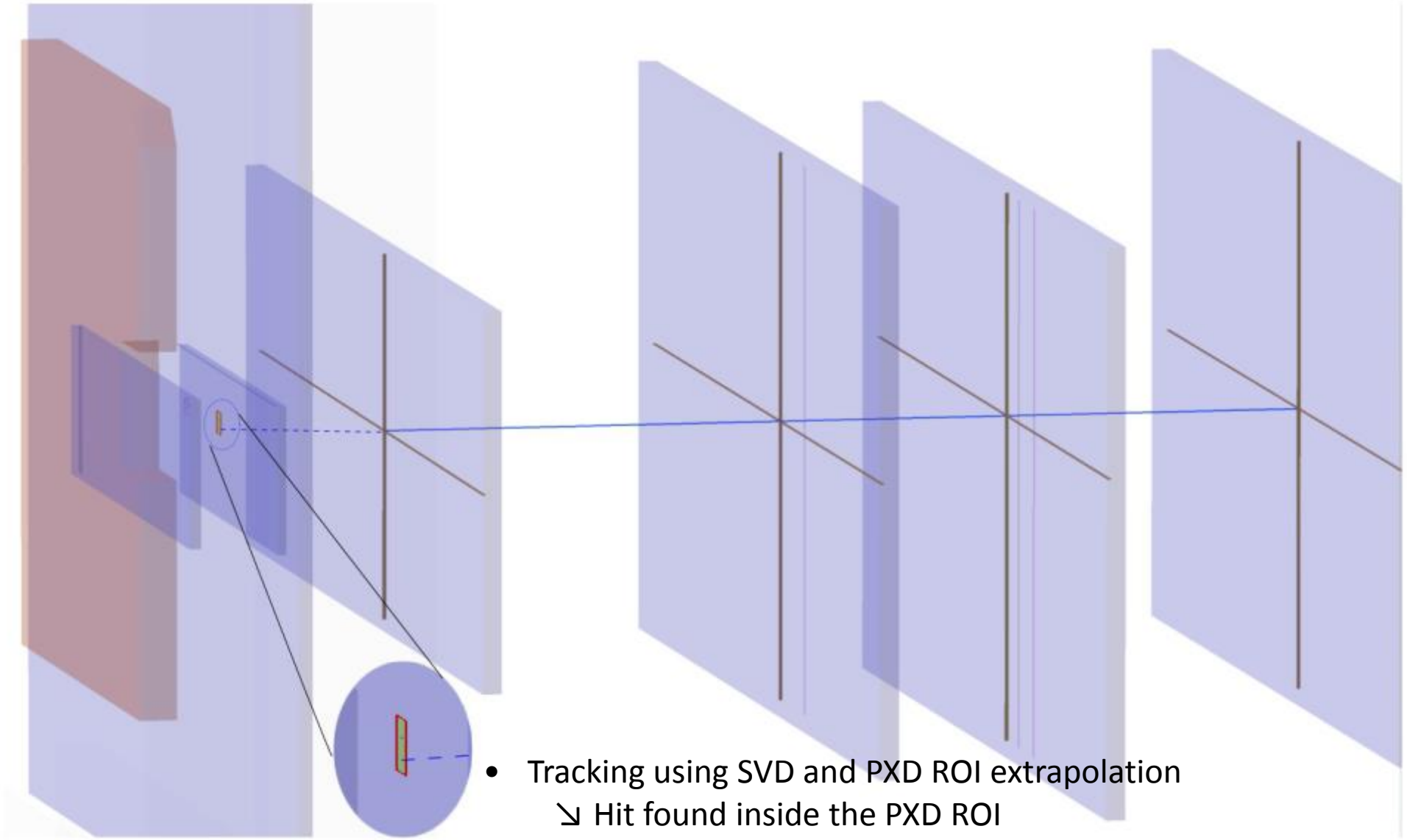
TB data reduction scheme



Region of Interest



- Tracking using SVD and PXD ROI extrapolation
  ↘ Hit found inside the PXD ROI
- Factor 6 data reduction → Further investigations ongoing