SI LAB
Silizium Labor Bonn

universitätbonn

Recent Status of Front-end Electronics for DEPFET Pixel Detectors for Belle II

Tetsuichi Kishishita

T. Hemperek, H. Krüger, M. Lemarenko, F. Lütticke, L. Germic, C. Marinas, and N. Wermes

TIPP 2014, 2-6 June. Amsterdam

Outline

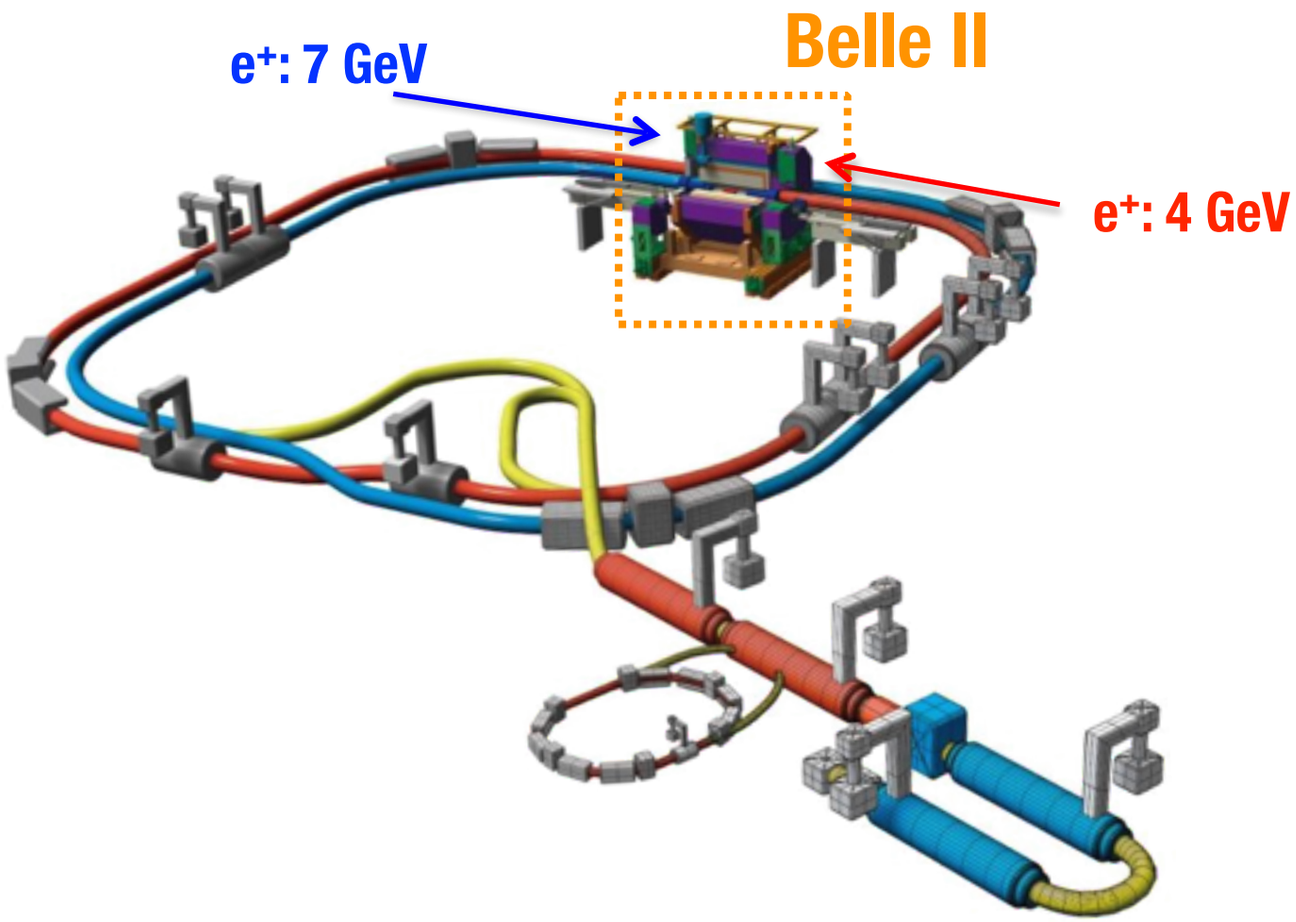
-Concept of the Belle II Pixel Detector

-Requirements to the Front-end Electronics

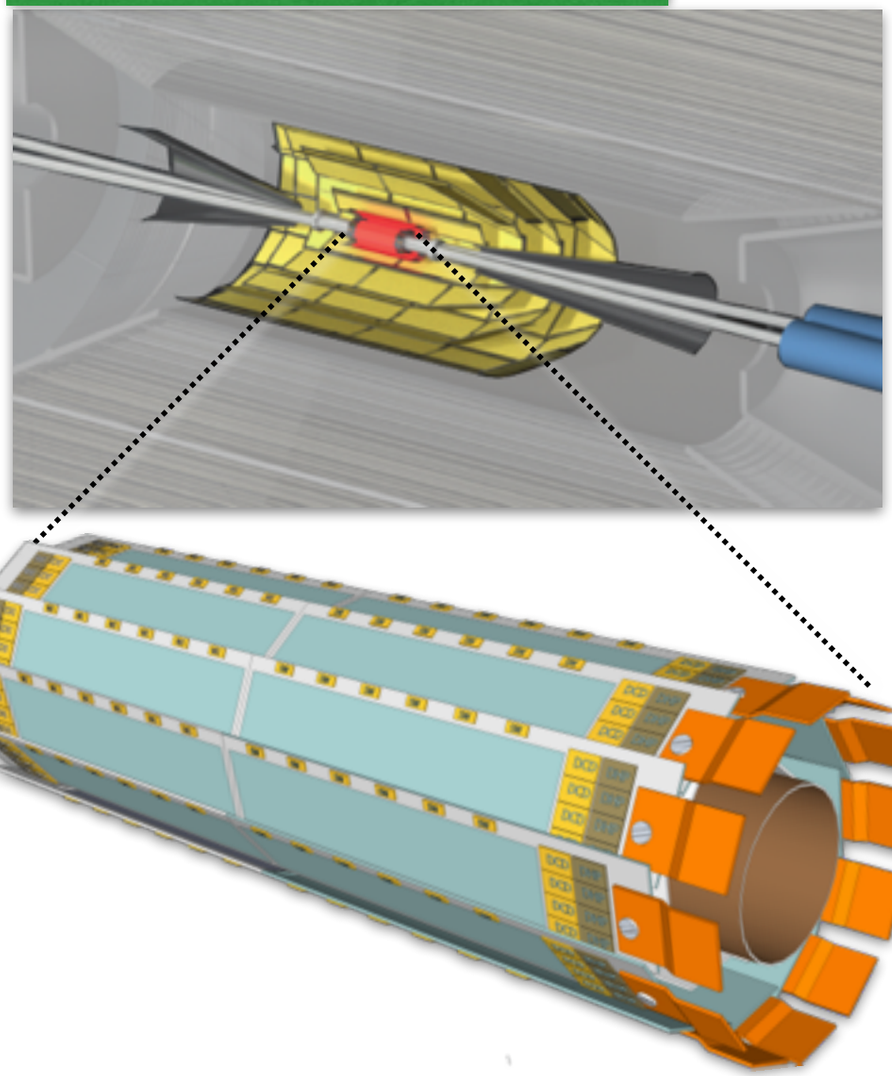
-Hybrid Module

-Test Results

Pixel Detector at Belle II Experiment



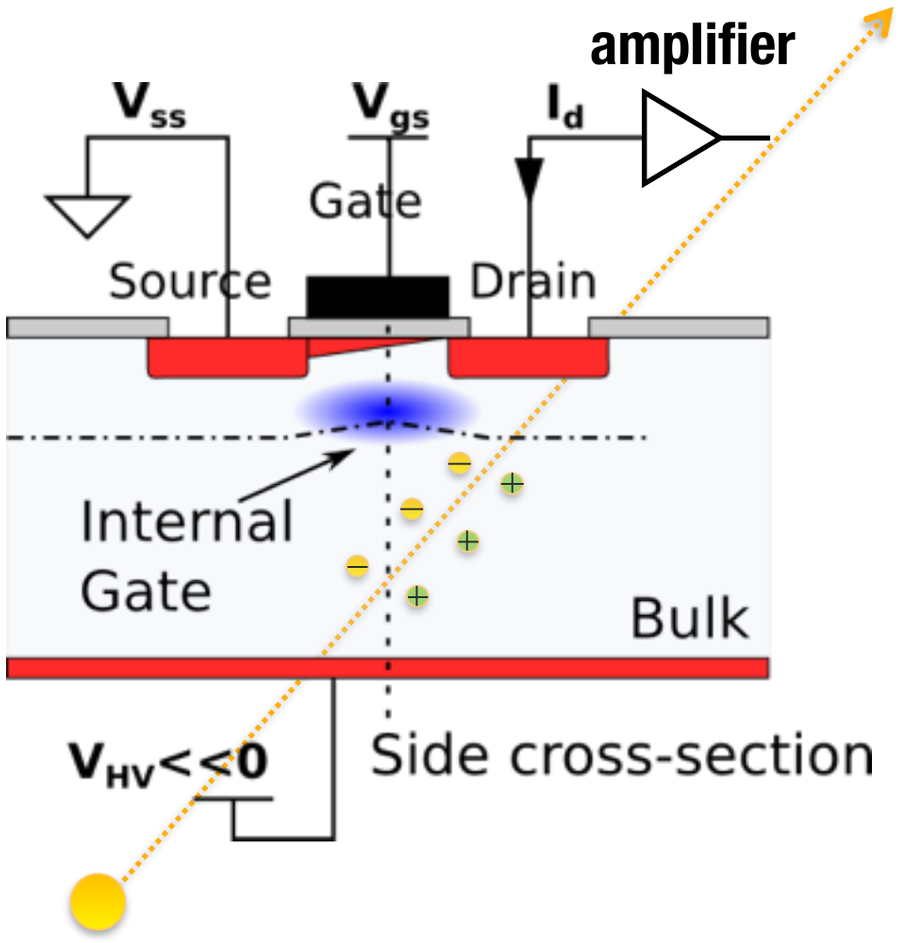
Pixel Detector (PXD)

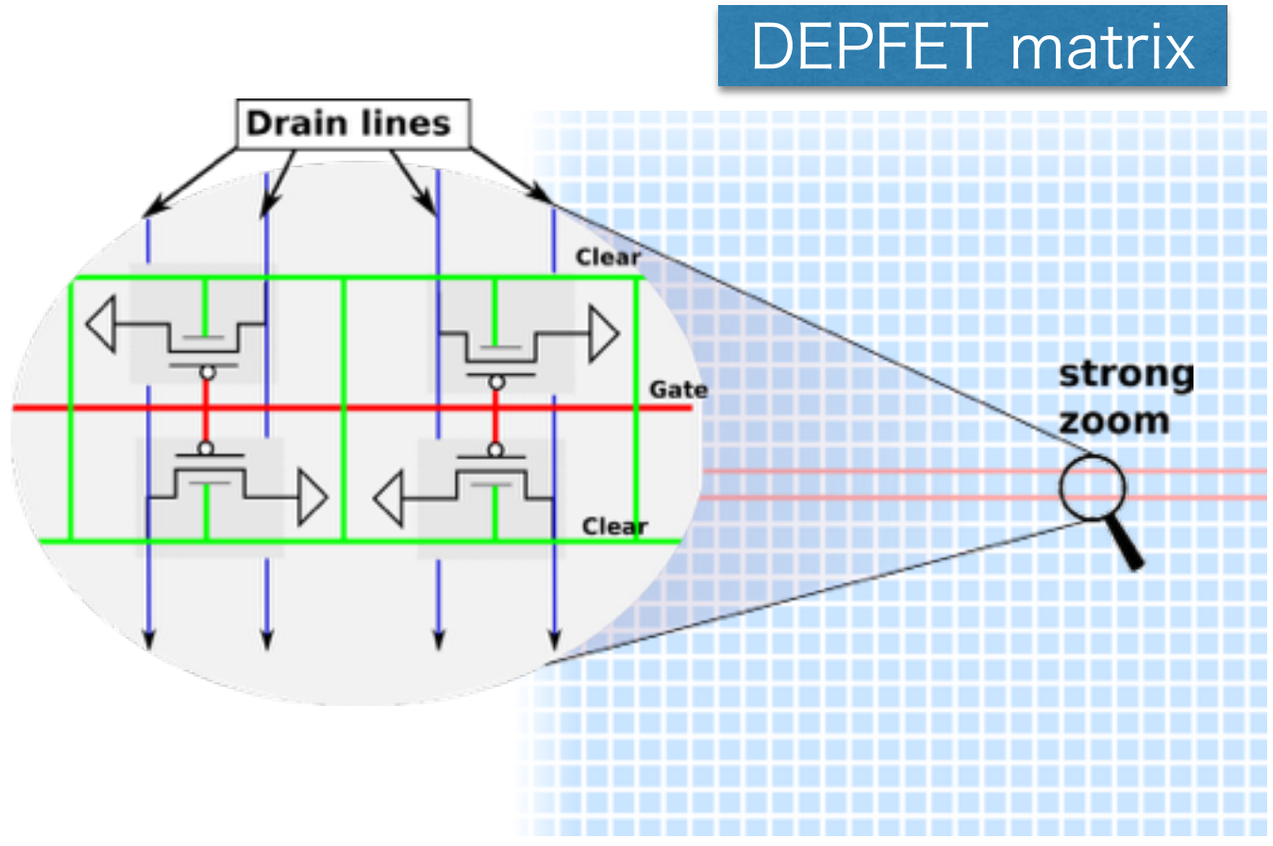


- e-/e+ collider for B^0/B^0-bar
- KEKB/Belle upgrade in Japan
- Super high-luminosity ~8×10^{35} $cm^{-2}s^{-1}$
- Refurbishment of accelerator & detector

- Innermost vertex detector (PXD) at Φ=14 & 22 mm, total 40 modules
- DEPFET sensors technology
- Frame rate of 20 us

DEPFET Sensors





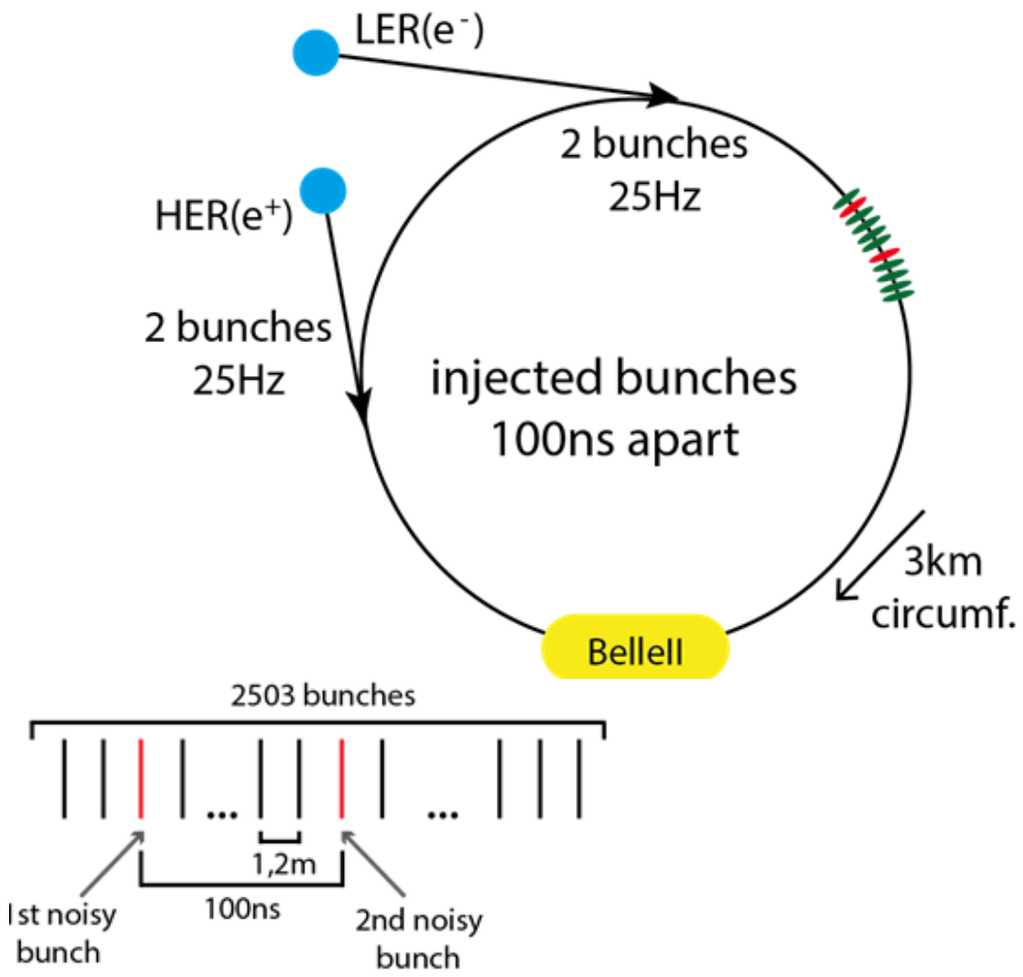
- p-FET on fully depleted bulk
- Modulation of the FET current by accumulated electrons under the internal gate (g_q~600 pA/e^-)
- Clear signals via punch-through effect

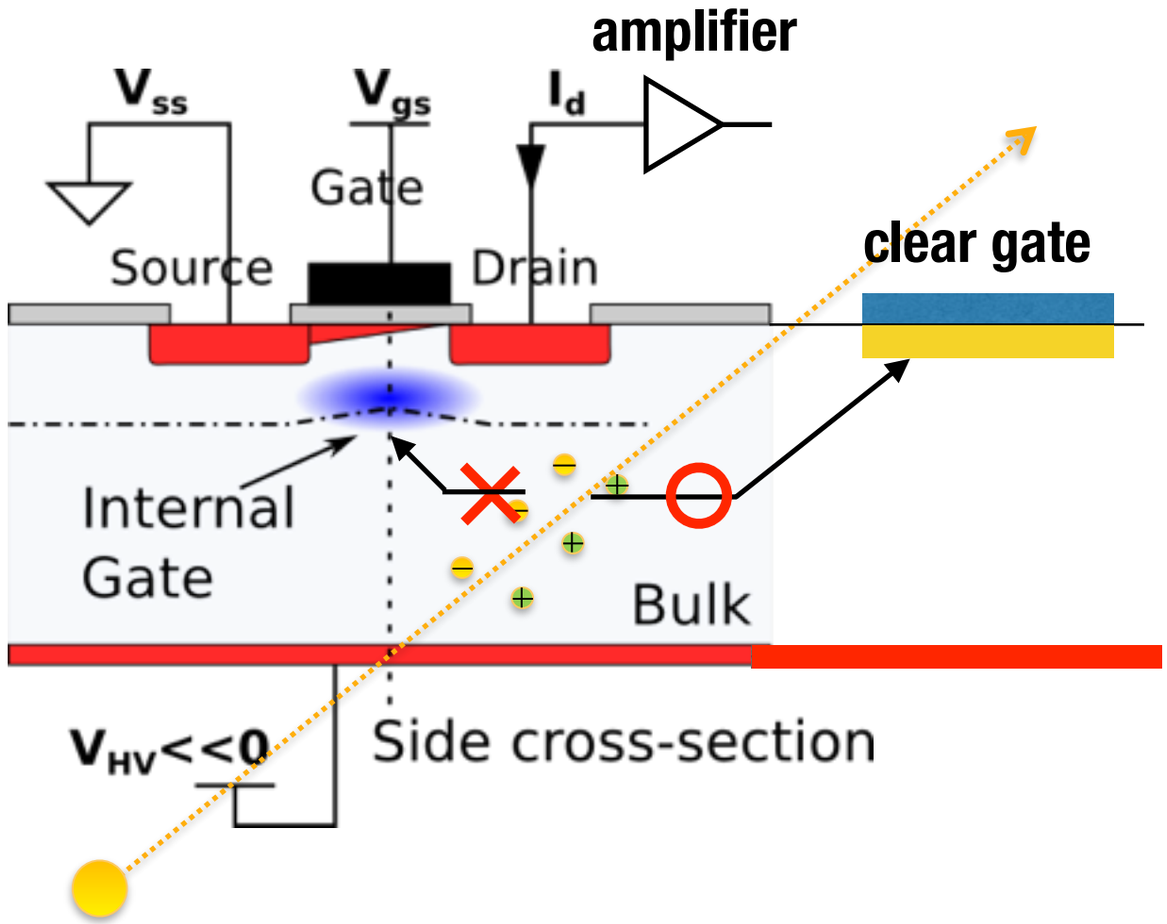
- Row-wise steering
- Column-wise connection of pixel drains
- Drain currents sampled by custom FE

Operating Mode

Normal, charge collection operation

Gated-Mode operation





Adjusting potential min. with gate and clear gates

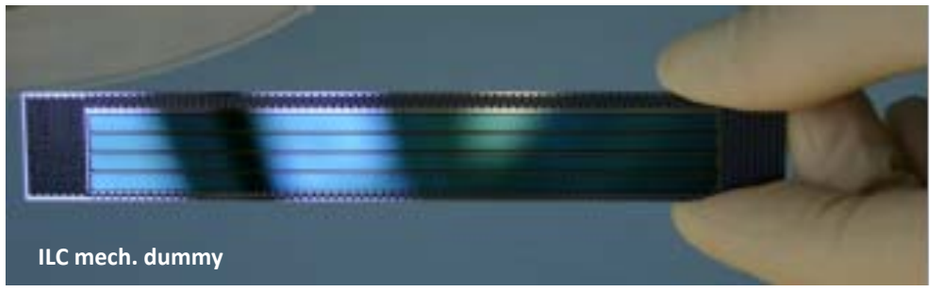
e- by noise bunch directly to clear gate

Front-end Electronics

- **Active pixel area thinned down to 75 um**
- **ASICs bump bonded on sensor substrate**

ASIC R&D more than 7 years

"All-silicon" DEPFET module



SWITCHER

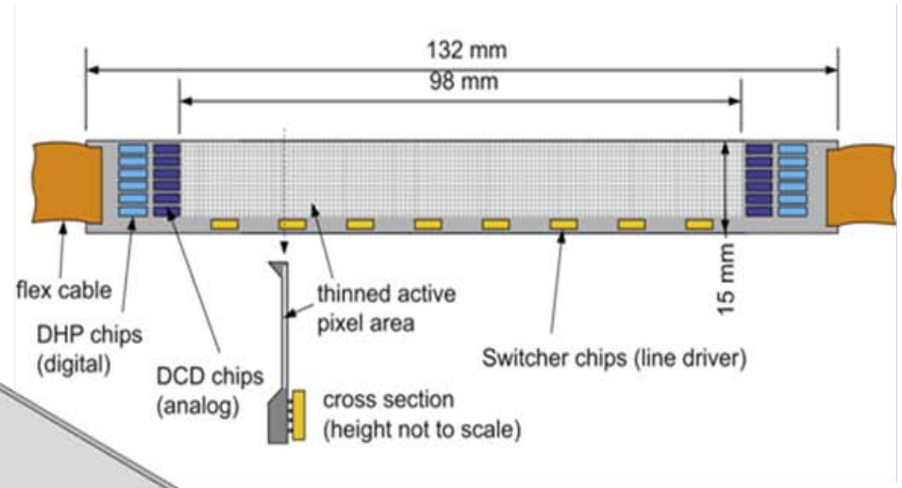
- **providing steering signals**

DCD (Drain Current Digitizer)

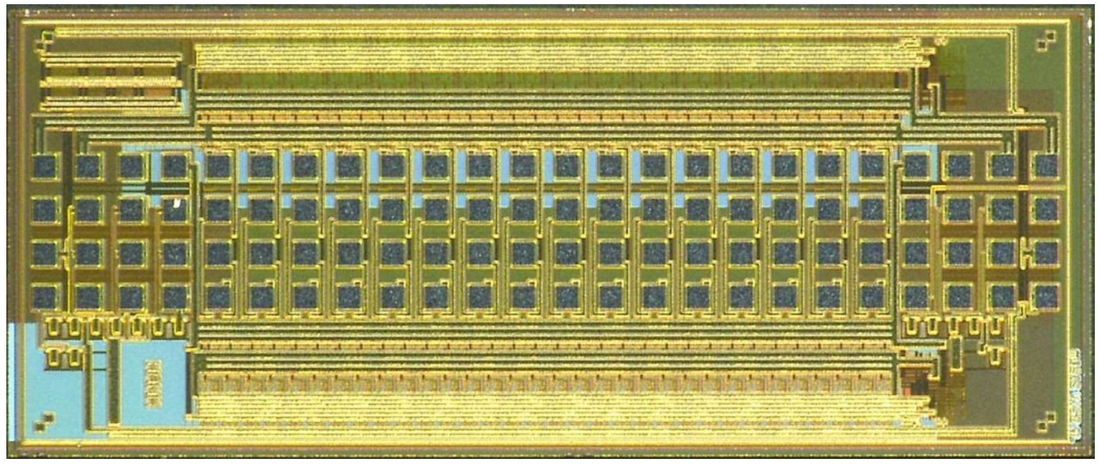
- **digitize the drain current from matrix**

DHP (Data Handling Processor)

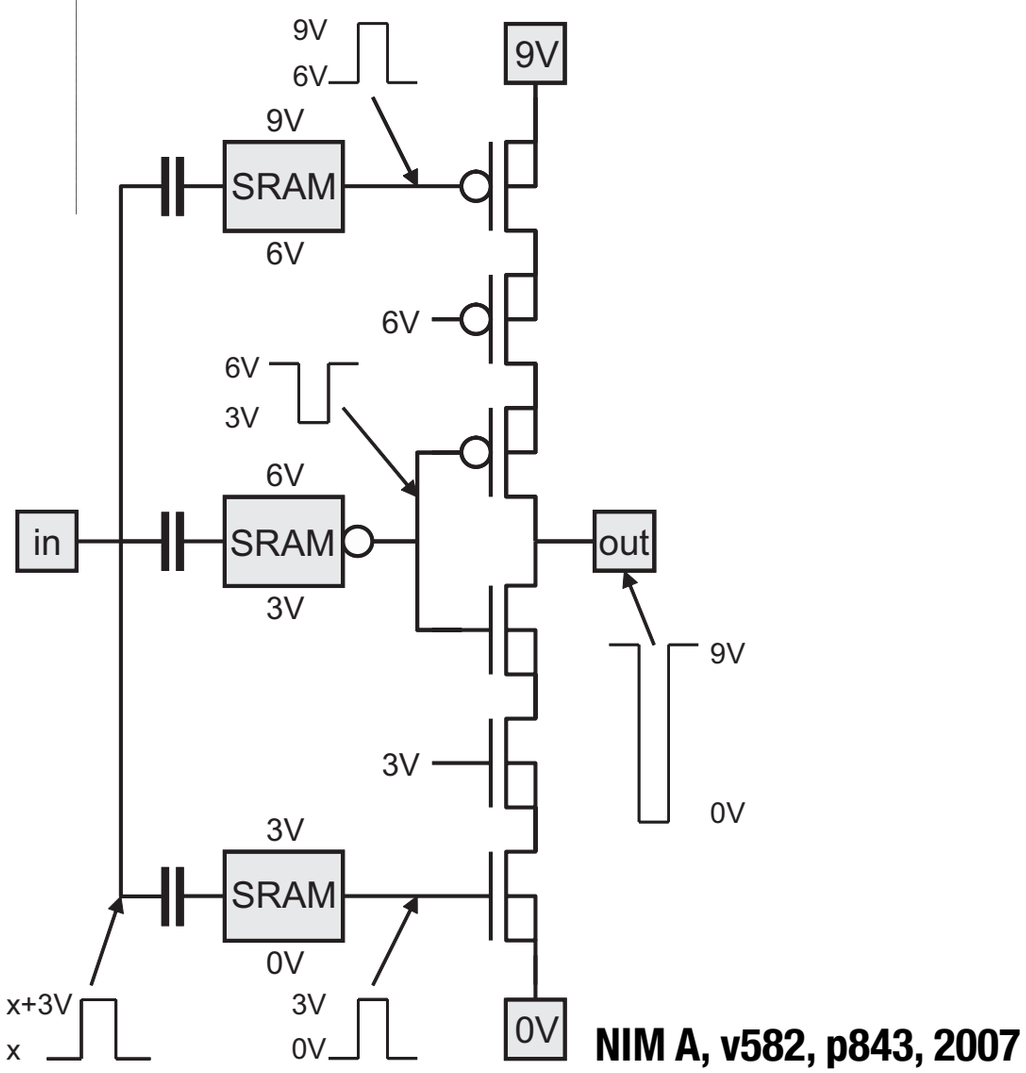
- **data reduction**
- **send data off the module to the backend elec.**



Front-end ASIC #1: SWITCHER-B



- **AMS high voltage 0.18 um CMOS**
- **Designed by Uni. Heidelberg**
- **Size: 3.6×1.5 mm^2**
- **contains additional logic for gated-mode operation**



NIM A, v582, p843, 2007

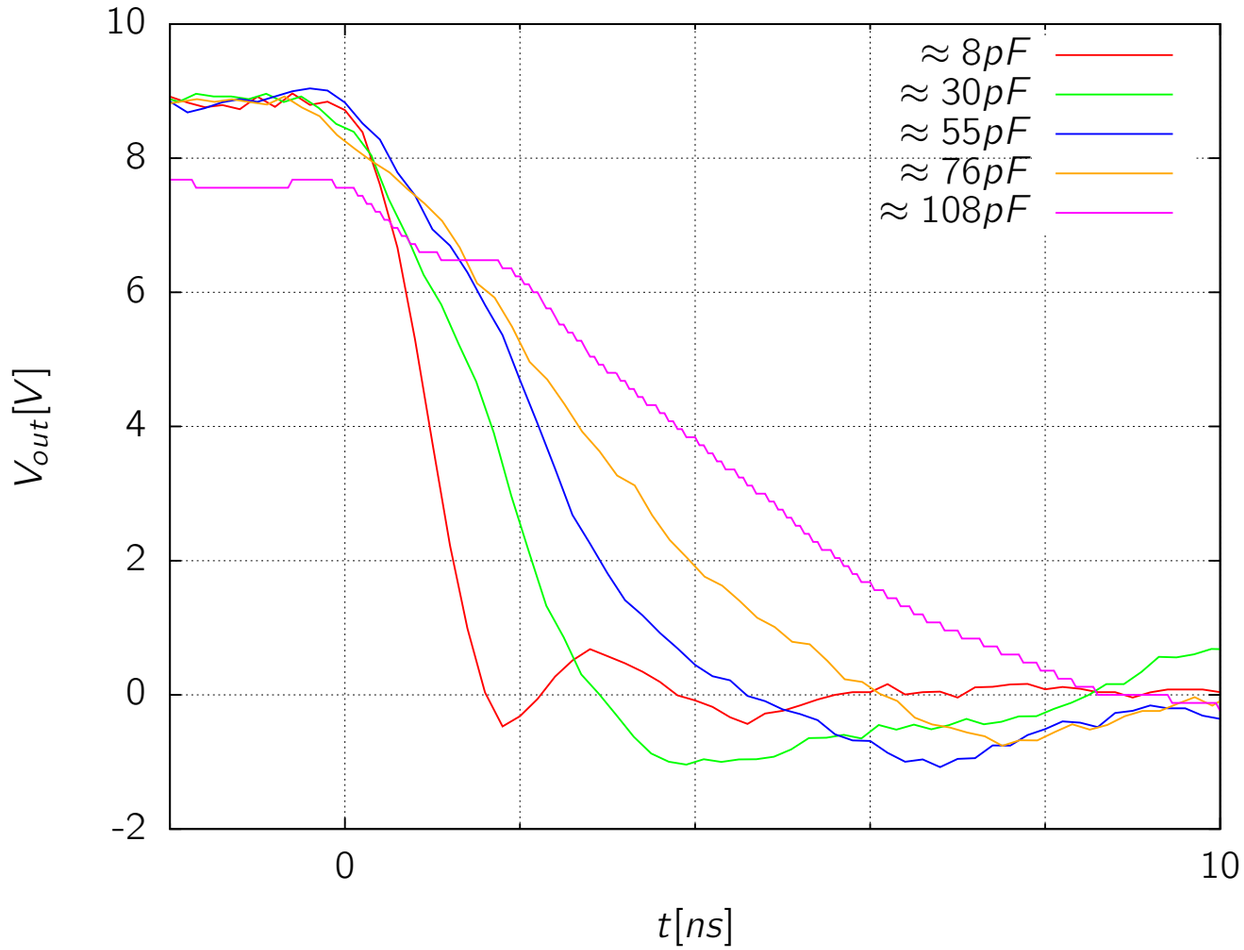
Requirements to the ASIC

- **Fast pulse to drive large line cap. (~50 pF)**
- **Fast HV up to 20 V for complete clear within ~20 ns**

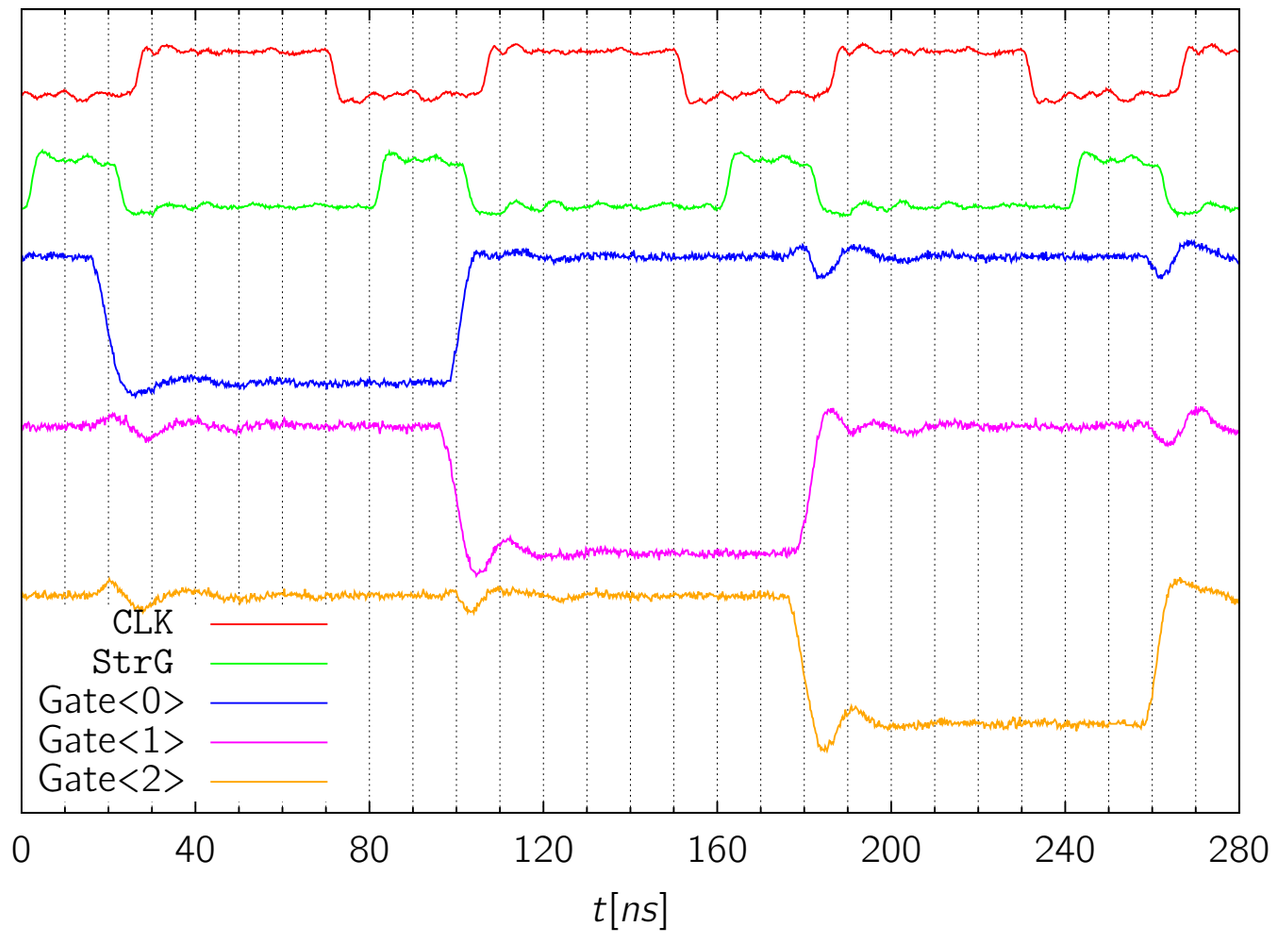
- **stacked-transistor output stage**
- **thin gate oxide transistors for rad.-hard**

Performance Verification

Falling edge with different loads

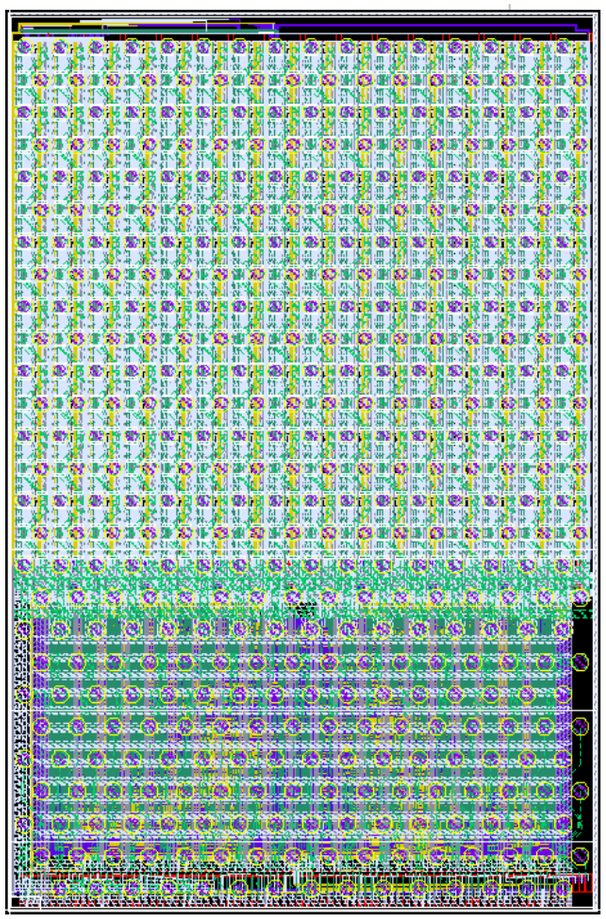


With 90 pF load and 80 ns gating



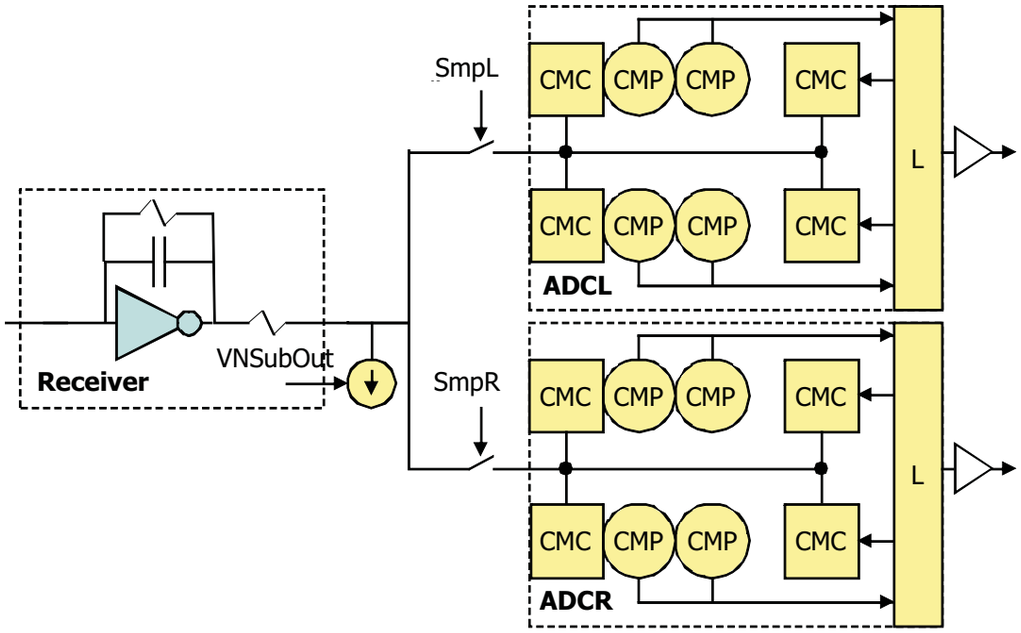
- **Flexible timing control with CLK and strobe signals**
- **Rad. Hard proven (up to 36 Mrad in previous design)**

Front-end ASIC #2: DCD (Drain Current Digitizer)



Requirements to the ASIC

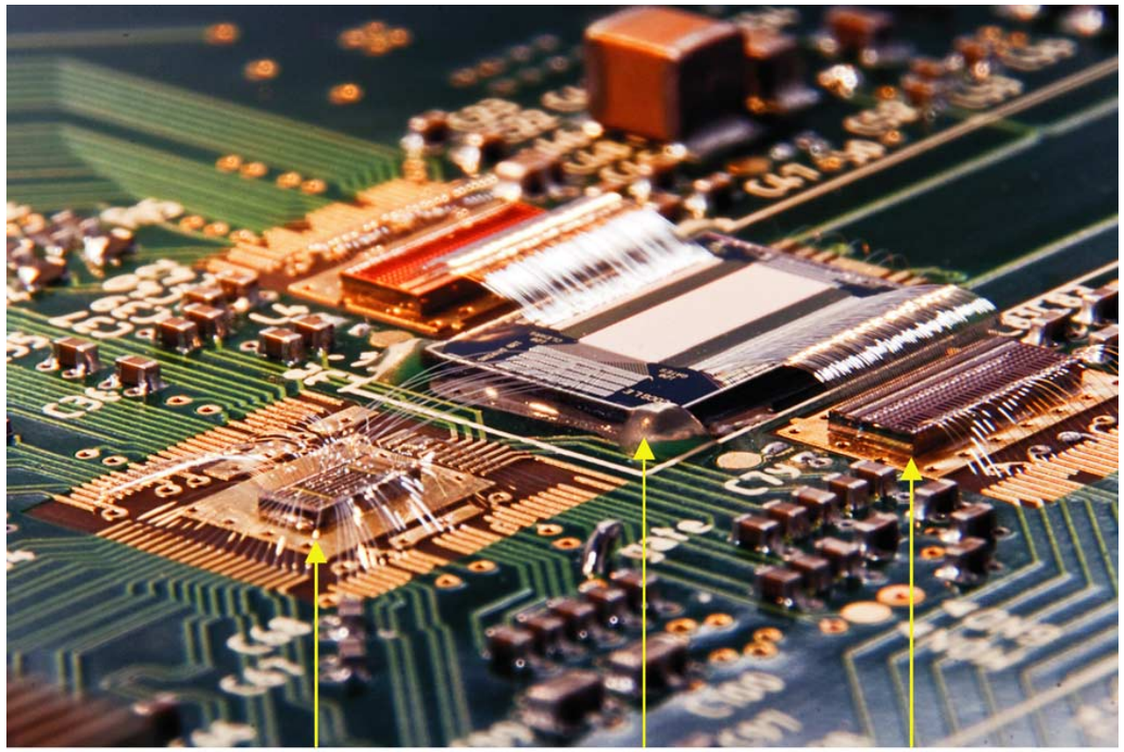
- **Low-noise & fast settling current receiver (Rs=200Ω, Cd=50 pF)**
- **10 M Sample/s**
- **256 input channels**



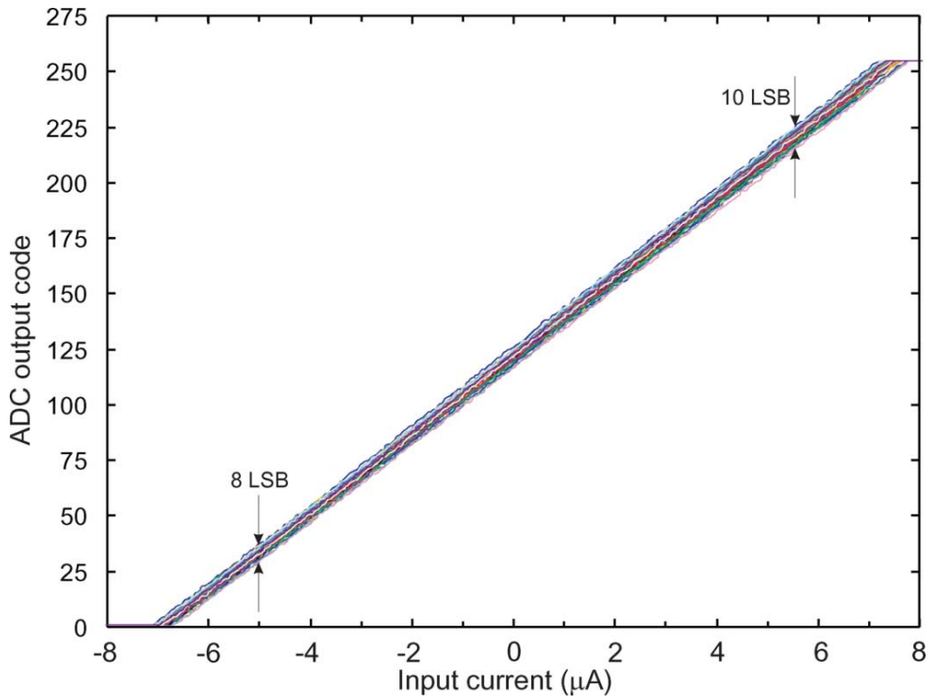
- **UMC 180 nm**
- **Designed by Uni. Heidelberg**
- **Size: 3.3×5.0 mm²**
- **Noise: 40 nA**
- **Irradiation up to 7 Mrad**

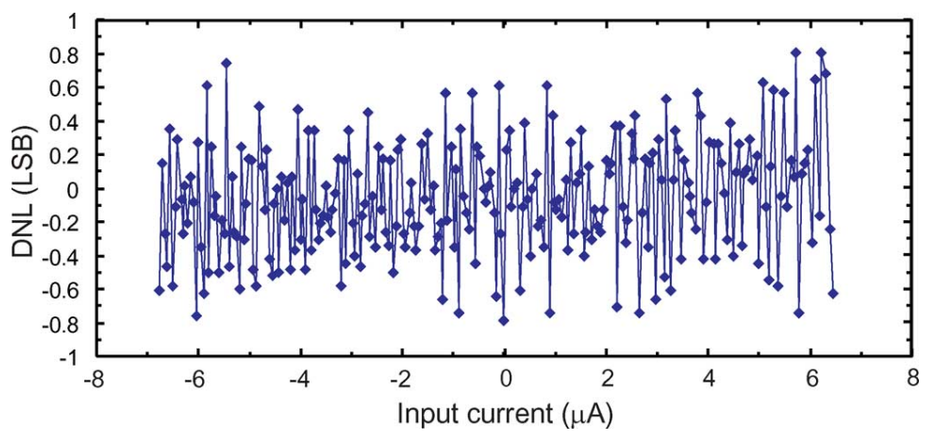
- **Trans-impedance amplifier**
- **performance adjustment with DACs**
- **Each channel with two current mode cyclic ADCs based on current-memory cells**
- **80 ns sampling period with 8 bits resolution**

Performance Verification



Transfer curve of the prototype





Technology	180 nm CMOS
Resolution	8 bits
Simulated settling time (3τ)	$\sim$ 9 ns (fast ADC: $\sim$ 4.5 ns)
Conversion rate	40 ns/bit (fast ADC: 20 ns/bit)
Full-scale current	$\pm 8\,\mu$A
DNL	$\pm 0.8 LSB$
INL	$\pm 1 LSB$
SNR	56 dB (fast ADC: 54 dB)
Power supply	1.8 V
Active area	40 μm $\times$ 55 μm or 0.0022 mm^2
Static power consumption	0.96 mW

IEEE TNS, v. 57, p. 743, 2010

TIPP 2014, 2-6 June. Amsterdam

Front-end ASIC #3: DHP (Data Handling Processor)

- TSMC 65 nm CMOS
- Designed by Uni. Bonn
- Size of 3×4 mm^2

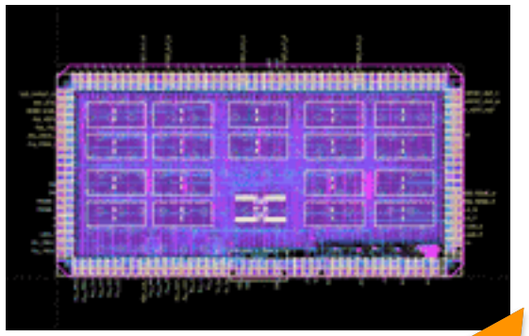
Functions of the ASIC

- Timing generation (1.6 GHz) + clock distribution
- Data processing
  - Zero-suppression
  - Only triggered data readout
  - Raw data buffering
  - Fixed pattern noise correction
  - Hit finder
  - Framing (AURORA)
  - Serializer and Gbit link driver

DHP Chip History at Bonn

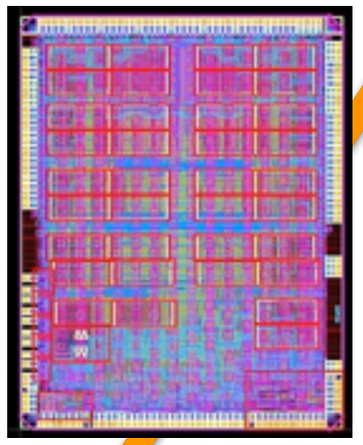
DHP 0.1, 2010, IBM 90nm

Half size prototype chip, 1.6 GHz PLL, Gbit link, memories, analog test structures, 200µm pitch bump bonds



DHP 0.2, 2011, IBM 90nm

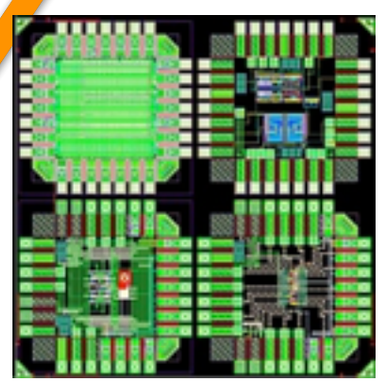
Second prototype (full size), 1.6 GHz PLL, Gigabit driver with programmable pre-emphasis, on-chip bias DACs



DHPT 0.1, 2011, TSMC 65 nm

test structures for future ATLAS and DEPFET projects.

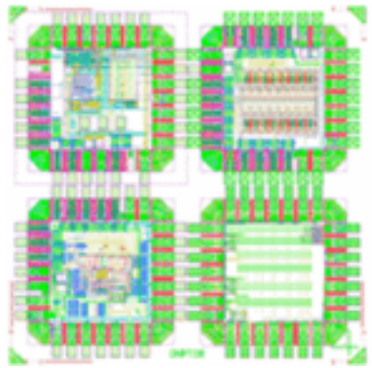
- **PLL + GBit link driver**
- **Charge sensitive amplifier**
- **Memory test structures**
- **DAC, current reference (U Barcelona)**



DHPT 0.2, 2012, TSMC 65 nm

test structures for future ATLAS and DEPFET projects.

- **LVDS IO**
- **8-bit, 10 Mbps ADC**
- **Analog Pixel Front-end**
- **Temperature sensor**



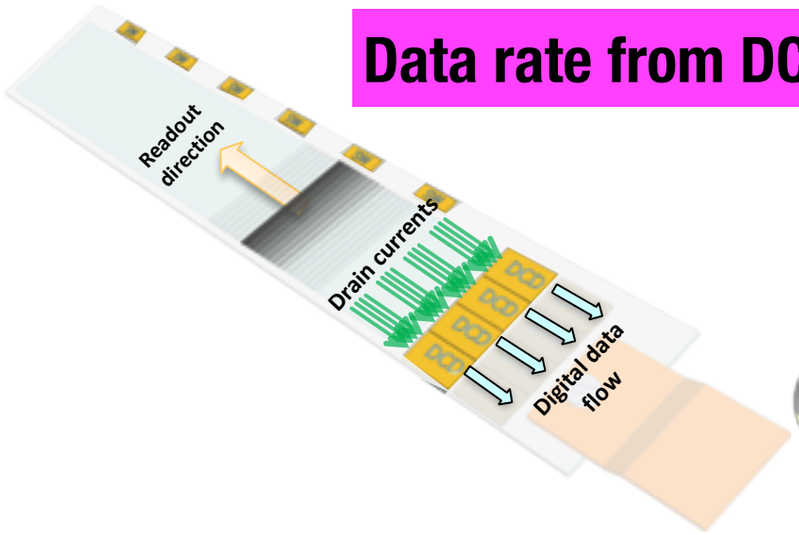
DHPT 1.0, 2013, TSMC 65 nm

First production version

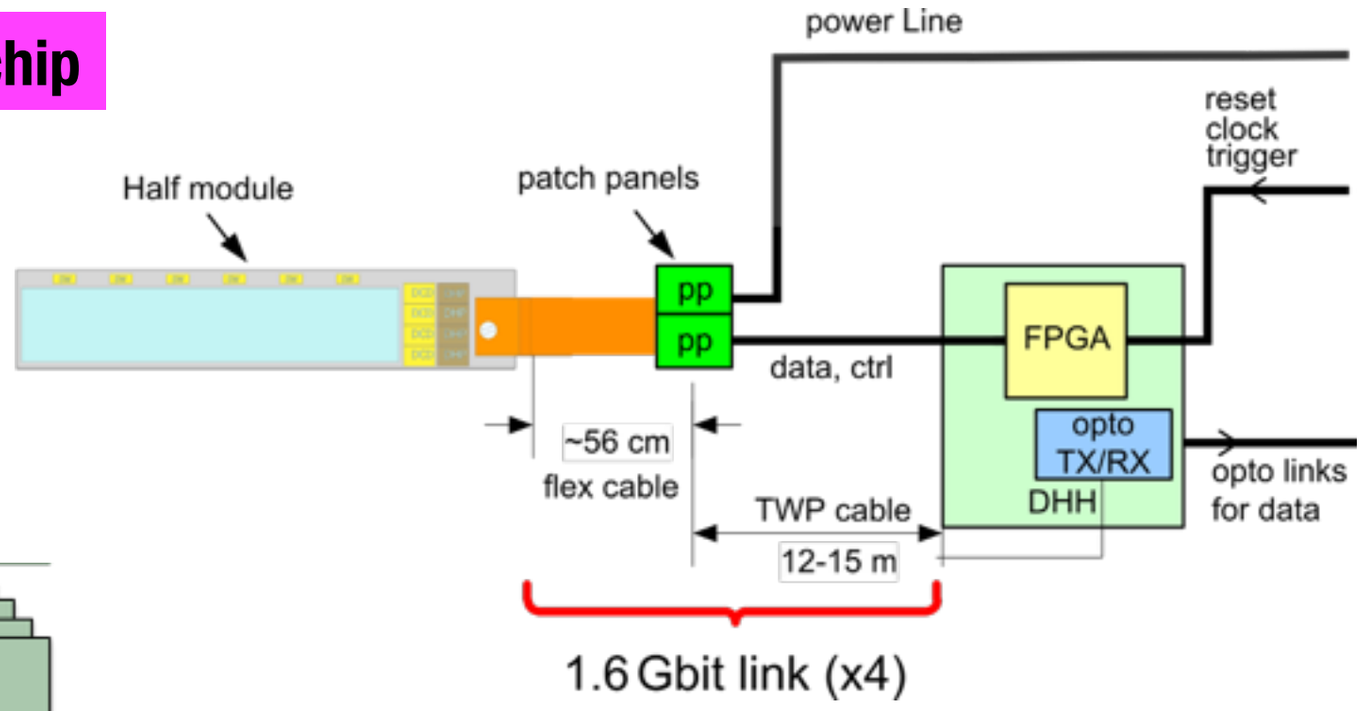
- **12 mm^2**
- **296 bumps**
- **3Mbit memory**
- **1.6 GHz data link**

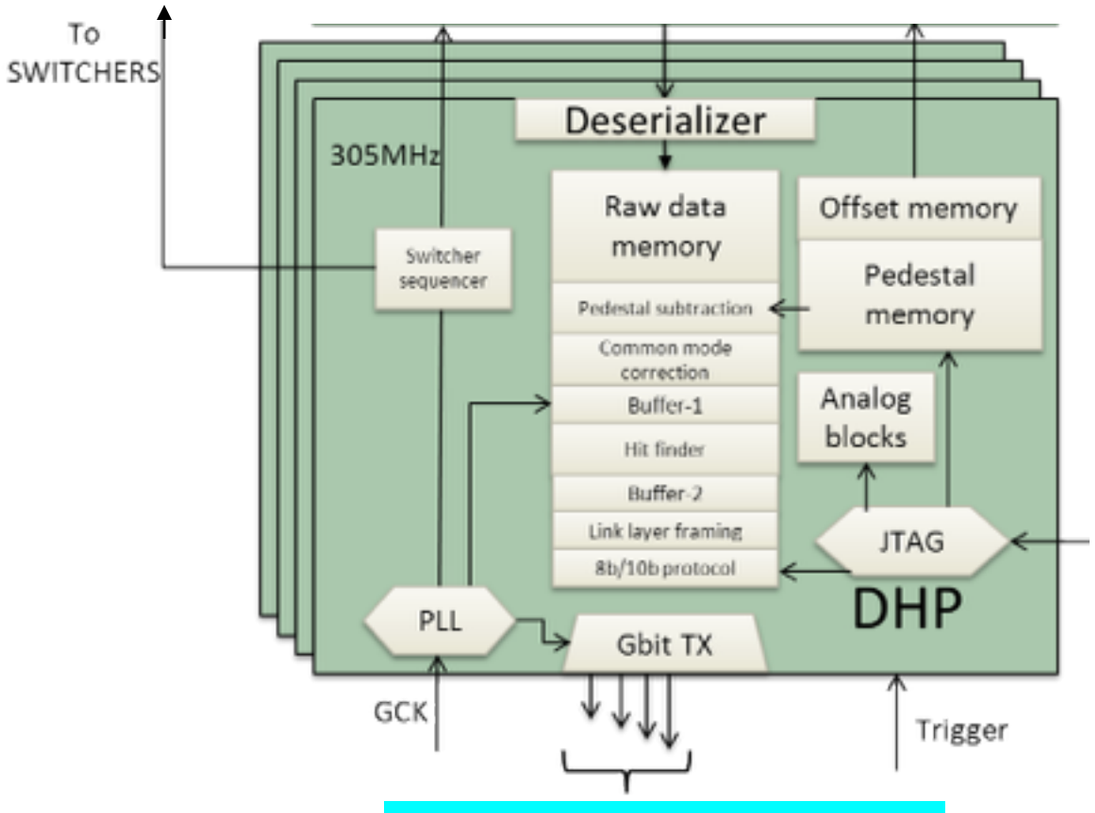
Data Link Specifications

Data rate from DCD:~20 Gbps/chip



/sec





One 1.6 Gbit link/chip

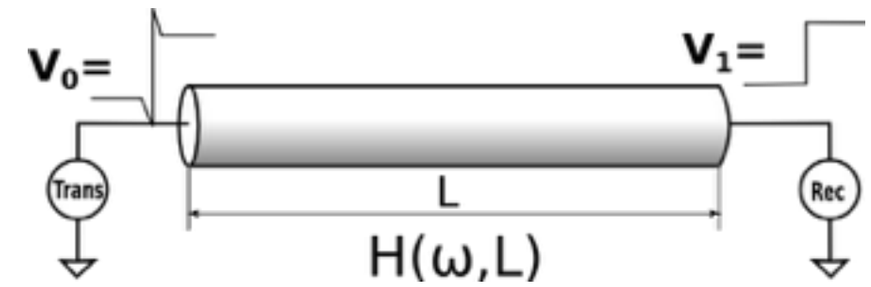
Requirements to the ASIC

-Data reduction of more than 1/10
-1.6 GHz PLL
-Link bandwidth & signal integrity (>15 m cable) are crucial

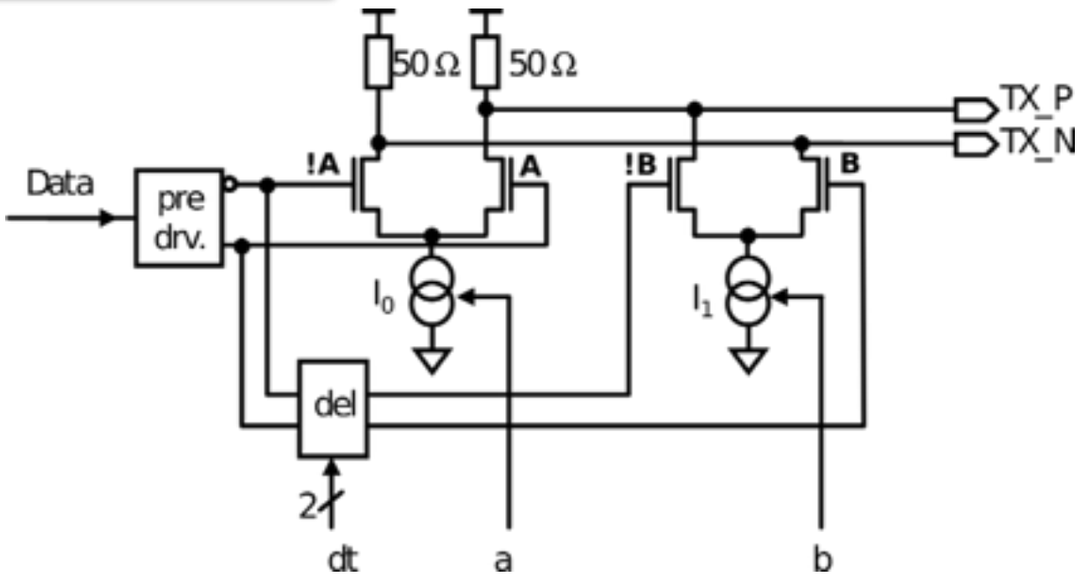
Pre-emphasis with Gbit link driver

Idea: boost high frequency components of the transmitted signal to compensate to cable attenuation

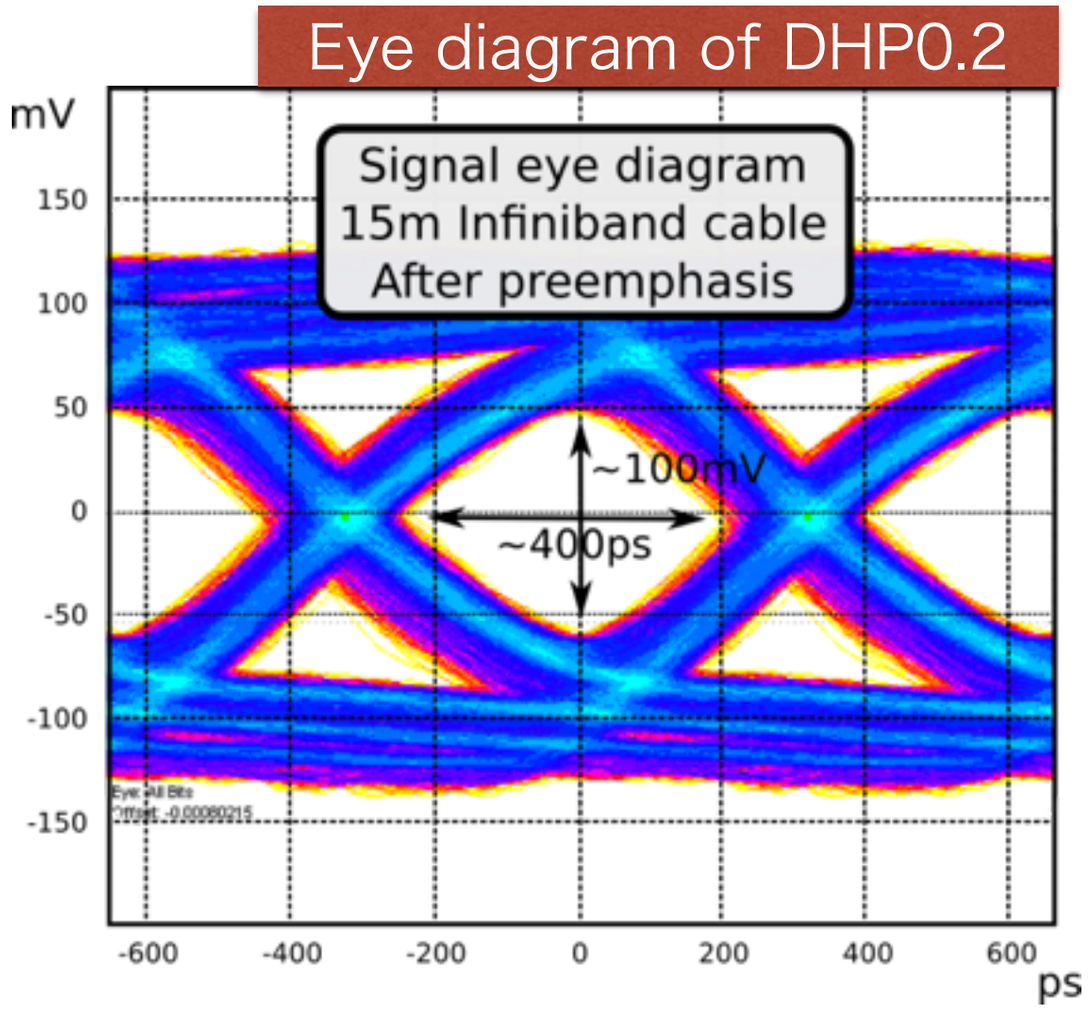
Pre-emphasis technique



CML transmitter

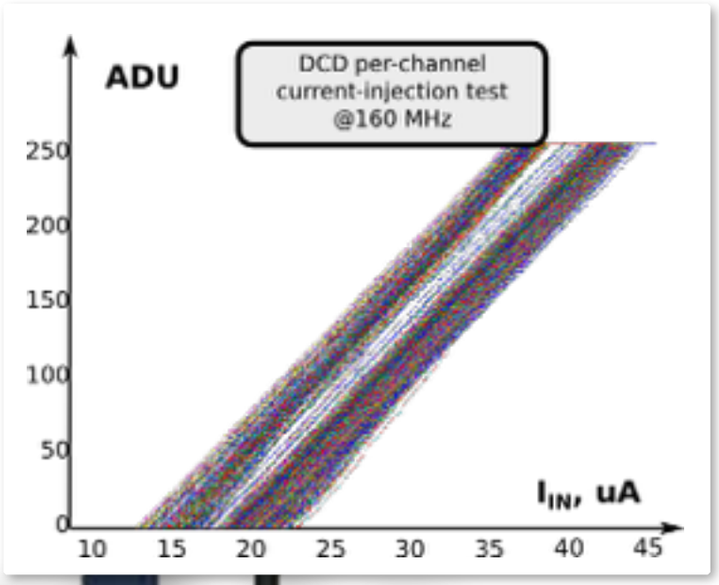


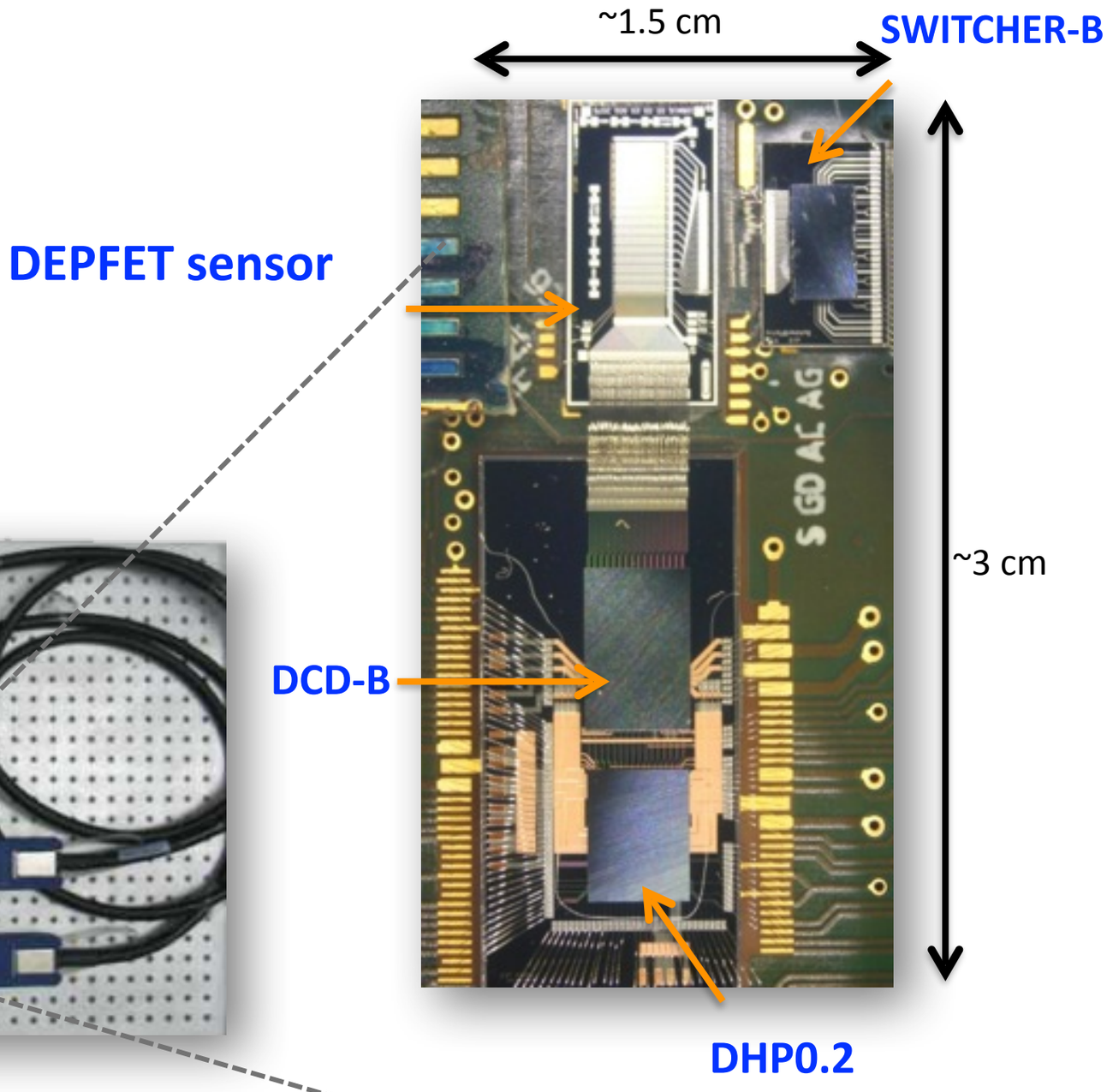
Eye diagram of DHP0.2



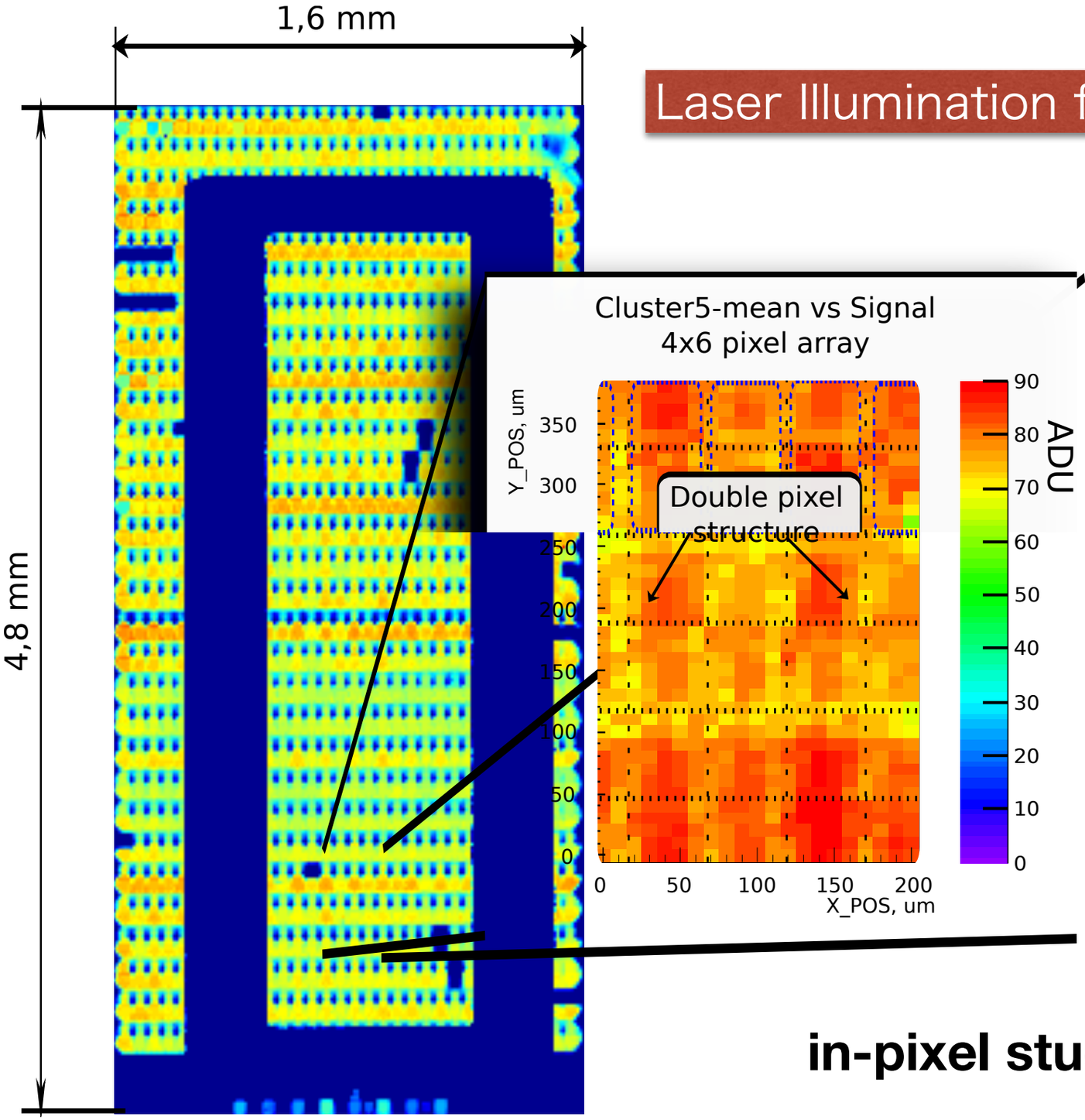
Full Scale Module Prototype

- **Assembly with bump-bonding**
- **Step-by-step ASIC functional checks**





Laser test



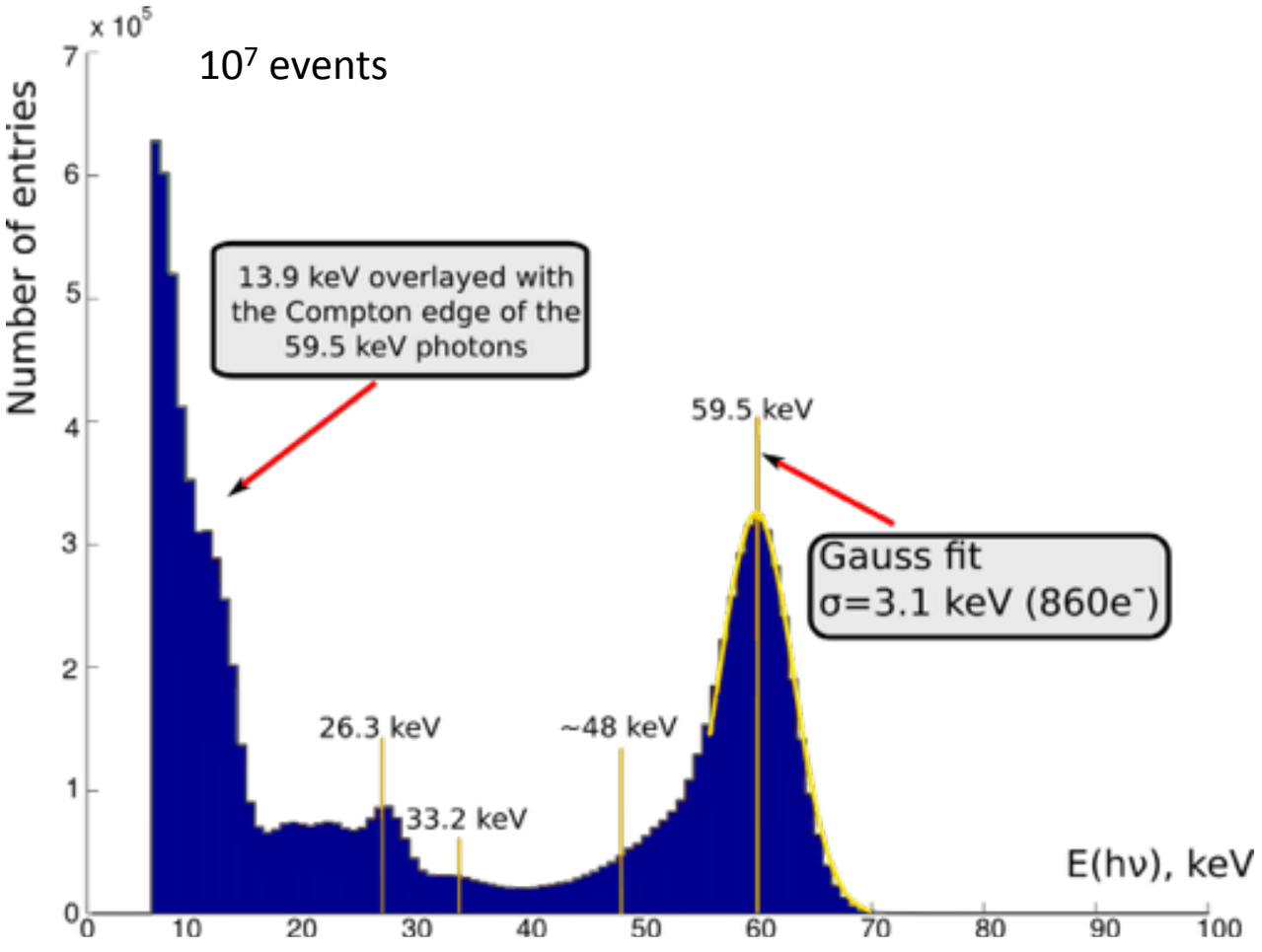
Laser Illumination from the back-side

- **Matrix size of 1.6×4.8 mm²**
- **Pixel size of 50×75 um²**
- **Metallization area shown in blue**
- **Variation of cluster signal: ~10 % position dependent**

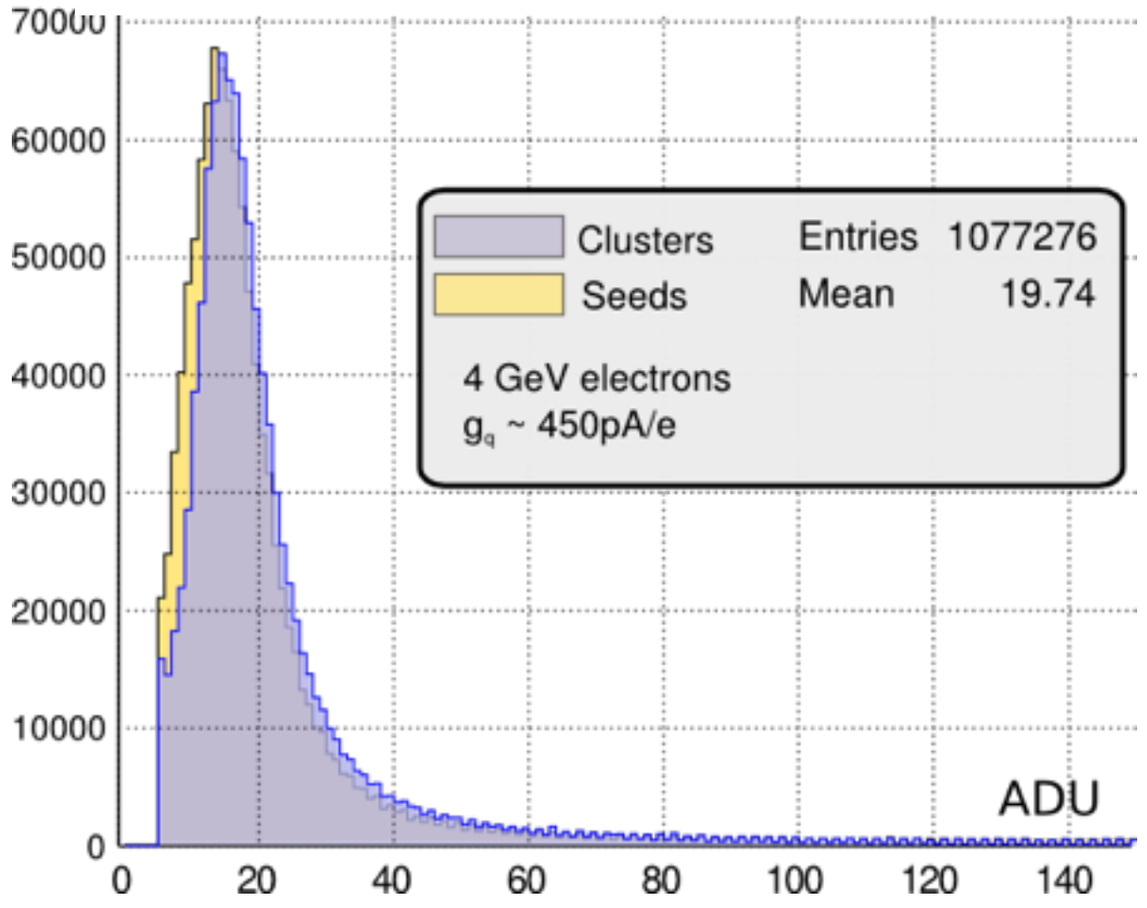
in-pixel study is possible!

IR-Source and Test beam results

Spectrum of Am-241



4 GeV electrons in 50 um DEPFET



All ASICs are working correctly with DEPFET sensor!!

Summary

-The Belle II PXD has been developed based on DEPFET sensors.
-All front-end electronics are almost ready to be integrated into modules.
-Currently three prototype DHPs have been produced with different technology and the first production version designed with a 65-nm CMOS has been delivered.
-The full-scale prototype module shows promising results in IR-source and test beam.

Thank you for your attention.

TIPP 2014, 2-6 June. Amsterdam