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Recent Status of Front-end Electronics for DEPFET pixel detectors for Belle-II

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The Belle II experiment, which will start after 2015 at the Super-KEKB accelerator in Japan, will focus on the precision measurement of the CP-violation mechanism and on the search for physics beyond the Standard Model. To cope with considerably increased background, a pixel vertex detector (PXD) based on DEPFET technology has been developed.
The PXD consists of two layers of DEPFET sensor modules located at 1.8 and 2.2 cm radii. Each module has a sensitive area, which is thinned down to 75 µm and steered with three types of ASICs: Switcher, Drain Current Digitizer (DCD) and Data Handling Processor (DHP). Switcher chips are designed to steer the pixel matrix of the sensitive area. The DCD chips digitize the drain current coming from the pixels. All ASICs will be directly bump-bonded to the balcony of the all-silicon DEPFET module. Its excellent spatial resolution (in the order of several microns) and low material budget was one of the decisive factors determining the choice of this technology for the first time. We report on the current status of the front-end electronics development, including the recent results from the first full-scale module prototype and chip testing.

Summary

The Belle-II pixel detector (PXD) has been developed based on DEPFET technology. The PXD requires three types of steering front-end electronics, and the development of the Data Handling Processor (DHP) is currently imperative. The DHP is designed to steer the readout from the DEPFET matrix by sending the control signals to the other two chips and sending the data off the module to the back-end data handling hybrid over a 15 m long electrical output link with a rate of 1.6 Gbps. Such high performance constraints for the digital data processing make the DHP implementation extremely challenging. Several conceptual solutions for the digital data processing blocks were proposed and implemented. Currently, three prototype DHPs have been produced with different technology and the first production version designed with a 65-nm standard CMOS technology has been delivered. The chip is currently under testing and is expected to be the production chip version, suitable for assembly on PXD modules.

Primary author: KISHISHITA, Tetsuichi (University of Bonn)

Co-authors: Dr MARINAS, Carlos (University of Bonn); Mr LÜTTICKE, Florian (University of Bonn); Dr KRÜGER, Hans (University of Bonn); Mr GERMIC, Leonard (University of Bonn); LEMARENKO, Mikhail (Universitaet Bonn (DE)); WERMES, Norbert (Universitaet Bonn (DE)); HEMPEREK, Tomasz (Universitaet Bonn (DE))

Presenter: KISHISHITA, Tetsuichi (University of Bonn)

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