Design of a Deep Buffer for the 0.13um CMOS PSEC5 Waveform Sampling ASIC

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We present a design for increasing the buffer length from 25.6ns to 3.3us in a prototype of PSEC5, a custom integrated circuit designed for analog-to-digital conversion of fast analog signals at a sampling rate between 5 and 15 Gigasamples/second. The prototype is being designed in the same 0.13um IBM-8RF CMOS process as the PSEC4 ASIC [1]. The major improvements are the increase of the storage buffer from 256 cells to 32,768 cells per channel, allowing a trigger latency of ~3.3us at 10GS/sec, and an increased readout rate. The input signal is continuously sampled into a Primary Array with 256 capacitors which, for a 100ps sampling rate, is rewritten every 25.6ns. The sampling pulses are generated by a Voltage-Controlled Delay Line in 256 stages, run as a Delay-Locked Loop (DLL). The deep Storage Array is organized as two arrays, each 128 capacitors wide by 128 deep. The contents of each half of the Primary Array are transferred into the Storage Array at fixed time intervals in an alternate fashion. The writing and reading of the Storage Array is done with full external control. The design allows uninterrupted writing of the Storage Array after a trigger by selecting a region-of-interest for read-out and temporarily removing it from the recording chain. Depending on the size of the region-of-interest window, the dead time can be greatly reduced or eliminated. The sampled signals are digitized on-chip, and read out serially. The design status and simulation results will be presented.

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The Block Diagram of the Deep Storage Buffer and the Timing Simulation of the PSEC5 Write Addressing Circuit are presented in Figures 1 and 2. The RF Input signal is applied to a set of 256 capacitors, the Primary Array (PA), where it is sampled at fixed intervals. A multi-stage transfer method is employed [2]. While one half of the PA is written, the values stored in the other half are transferred into one of the 256 Storage Arrays (SA).

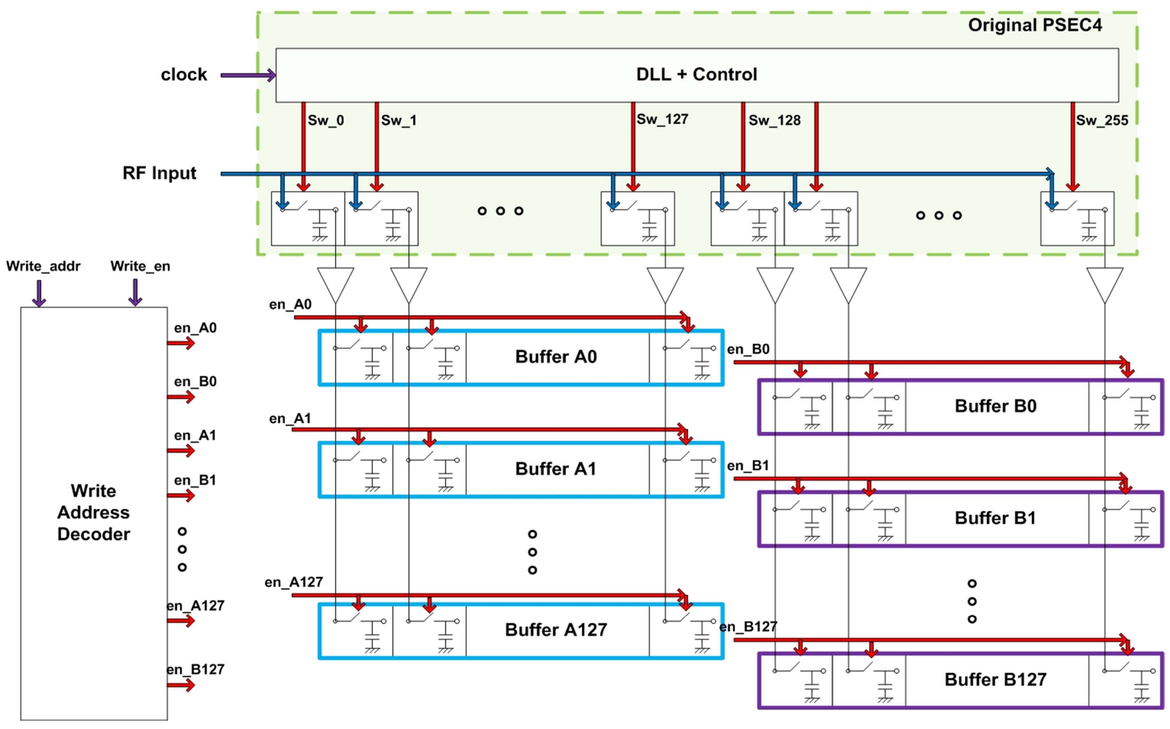

Figure1. Block Diagram of the PSEC5 Buffer. The reference clock is divided into 256 sampling pulses for recording the RF Signal on the Primary Capacitor Array. Voltages are then buffered and transferred to the Storage Arrays.

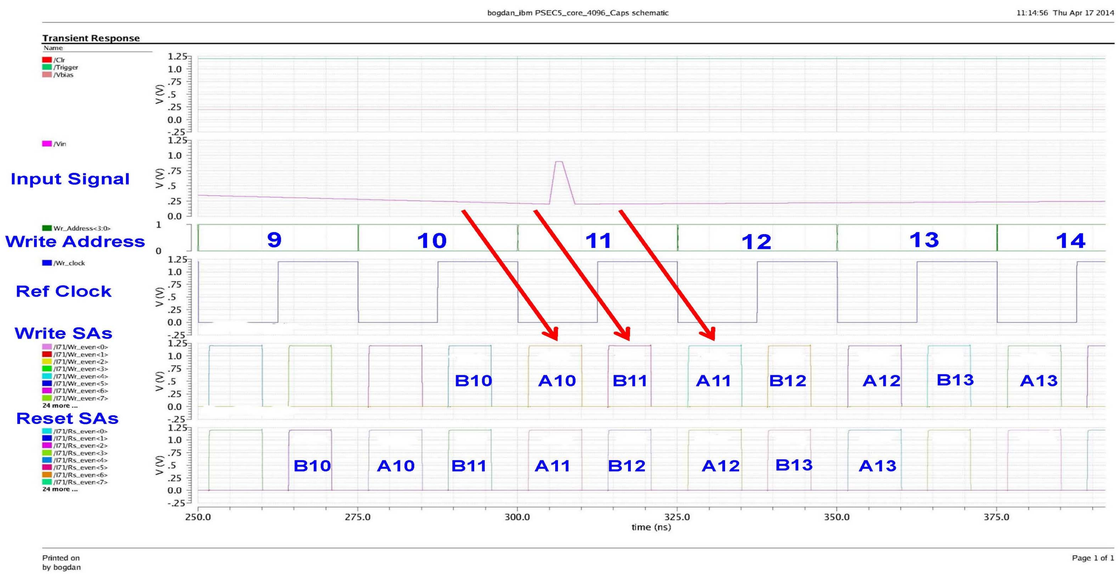

Figure 2. Timing Simulation of the PSEC5 Write-Addressing Circuit. Voltages stored into each half of the Primary Array are successively transferred to a 128-capacitor Storage Array.

The exact timing of the SA Write pulses and their widths are adjusted digitally relative to the reference clock. One clock cycle before each writing, a second set of pulses resets the storage capacitors to a common value. Figure 3 presents a sine input signal, as it passes through the chip and into the storage capacitors.

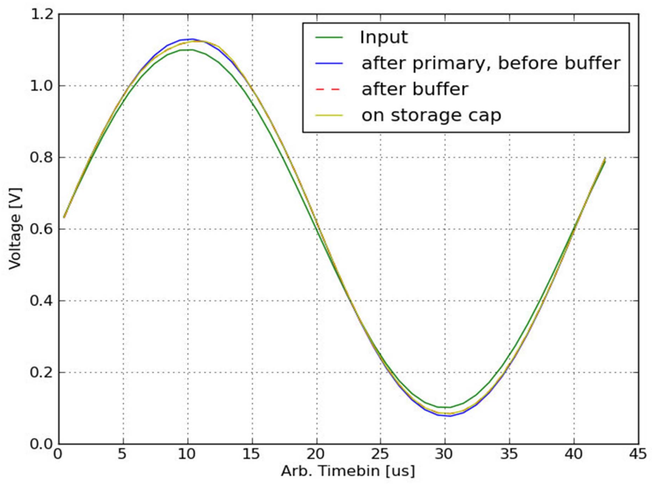

Figure 3. Comparison of a sine input signal, as recorded first on the Primary Array, then buffered, and finally stored on the Storage Array capacitors. Simulations were performed with different reset voltages for the storage caps. Simulation results shown are for Vreset = 1.1V.

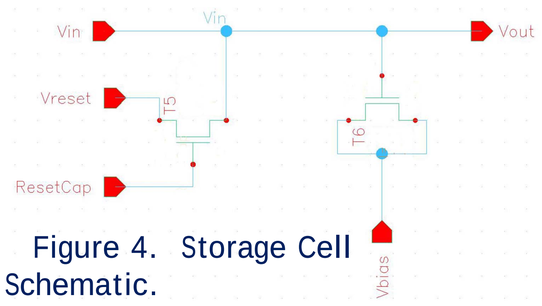

Figure 4. Storage Cell Schematic.

The actual cells for the Storage Array are made with NFET transistors, as shown in Figure 4. The errors caused by leakage currents were simulated with different values for Vin, Vbias, and Vreset, and for time intervals of up to 100us after a trigger. One example is shown in Figure 5.

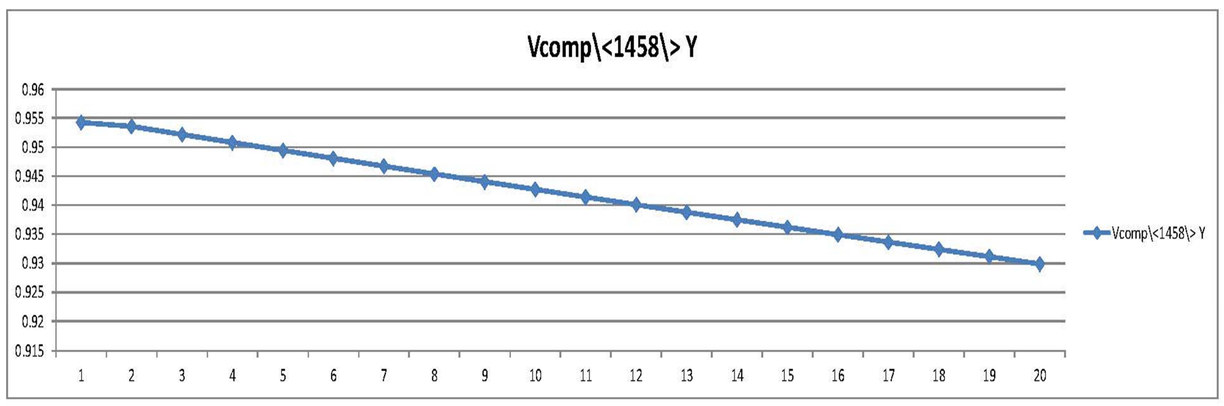

Figure 5. Storage Cell Discharge over a 100us time period. There is a 2.5% Voltage decrease over 100us for a 950mV signal with a 200mV baseline.

Building on the PSEC4 ASIC designed at The University of Chicago, the PSEC5 chip has an increased storage buffer from 256 cells to 32,768 cells per channel, for a trigger latency of over 3us at 10Gsps.

References:
[1] E. Oberla et al., NIM A735, p452; Jan. 2014
[2] L.L. Ruckman, G.S. Varner, NIM A602, p438-445; 2009

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