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CLARO-CMOS: a fast, low power and radiation-hard front-end ASIC for single photon counting in 0.35 micron CMOS technology

Presented by C. Gotti

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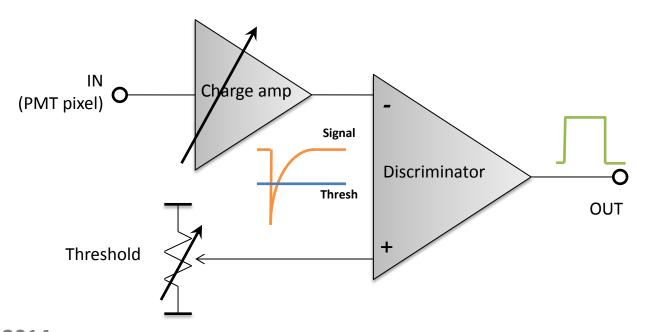
Overview of the CLARO

The CLARO is an integrated circuit designed for **single photon counting** with Ma-PMTs.

Main features:

- 0.35 um CMOS technology from AMS (\rightarrow Low cost, high yield, long lifespan)
- Counts at 40 MHz Recovery time < 25 ns
- Low power consumption ≤ 1 mW/channel
- Settable gain and threshold (8 bits per channel)

Block schematic of one channel:



Timeline

2011:

The 4 channel prototype «CLARO-CMOS» was designed

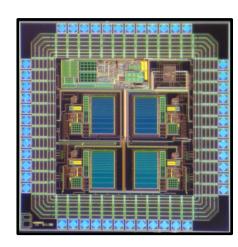
2012:

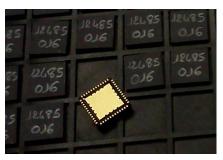
Deep characterization on the test bench First tests with SiPMs and R11265 Ma-PMTs

2013:

Radiation hardness tests with neutrons, X-rays and protons
More tests of the CLARO-CMOS with R11265 Ma-PMTs

Chosen as the baseline front-end ASIC for the LHCb RICH upgrade





2014:

The **8 channels version** with improvements was designed and received last week (it will not be described here)

CLARO-CMOS schematics

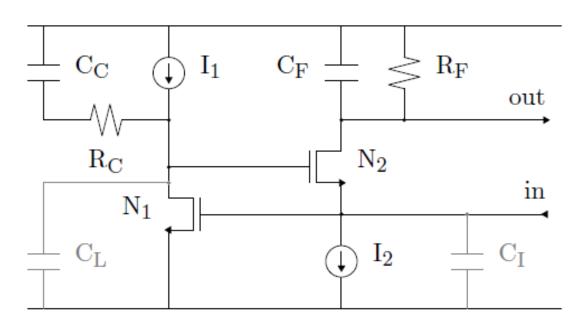
The amplifier is an active cascode, or «super common base», similar to others (such as the MAROC chip designed by the Omega group in Orsay).

 N_1 provides a feedback loop to keep the input impedance of N_2 low (about 100 Ω).

The charge signals are integrated and converted to voltage signals on C_F and R_F .

C_C and R_C are needed to keep the feedback loop stable.

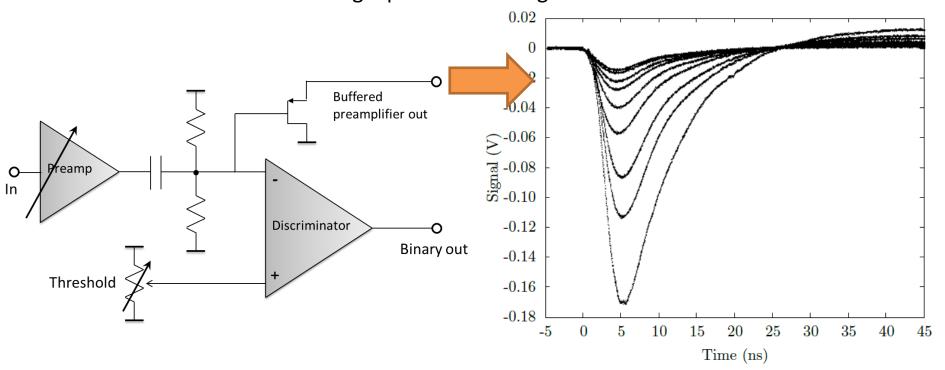
(C_I and C_L are parasitics.)



> The design of the chip is described in detail in JINST 7 P11026

Output signals (1)

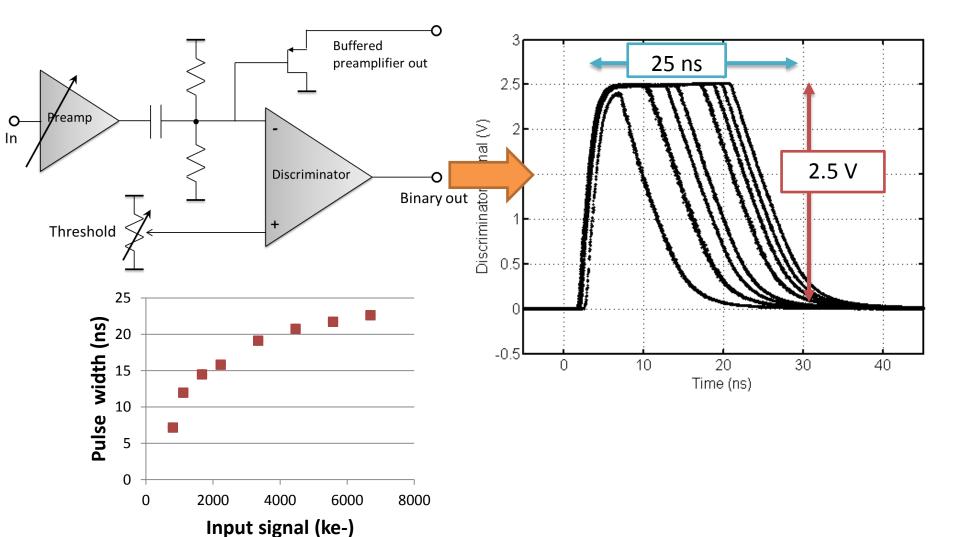
Signals at the analog output, for typical Ma-PMT signals at the input (330 ke- to 3.3 Me-). The analog output is buffered with a PMOS follower, and is mainly used for debugging. It is not meant to be used for single photon counting.



The AC coupling (55 ns) between the preamp and the discriminator causes the undershoot. This can result in a threshold shift at high rate (higher than about 10 MHz). The AC coupling will be removed in the next versions of the chip.

Output signals (2)

Signals at the main (binary) output, for typical Ma-PMT signals at the input (810 ke- to 6.7 Me-, threshold set at about 800 ke-).



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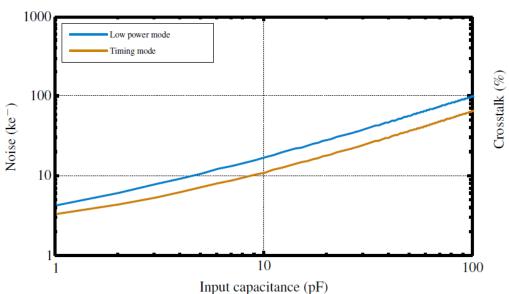
Input capacitance

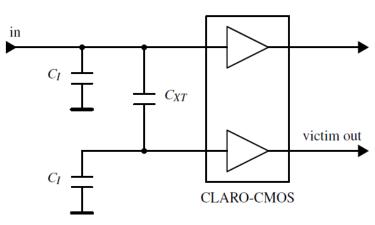
The input capacitance to ground and to neighbouring pixels should be minimized:

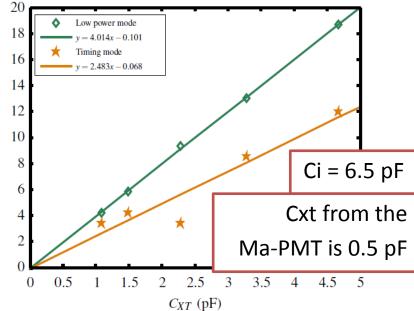
- The input capacitance to ground gives noise
- The input capacitance between pixels gives crosstalk

The minimization of input capacitance guides the layout of the CLARO PCBs.

It is one of the main reasons to keep low the number of channels per chip, so that the length of the traces connecting the pixels to the chip is minimized.



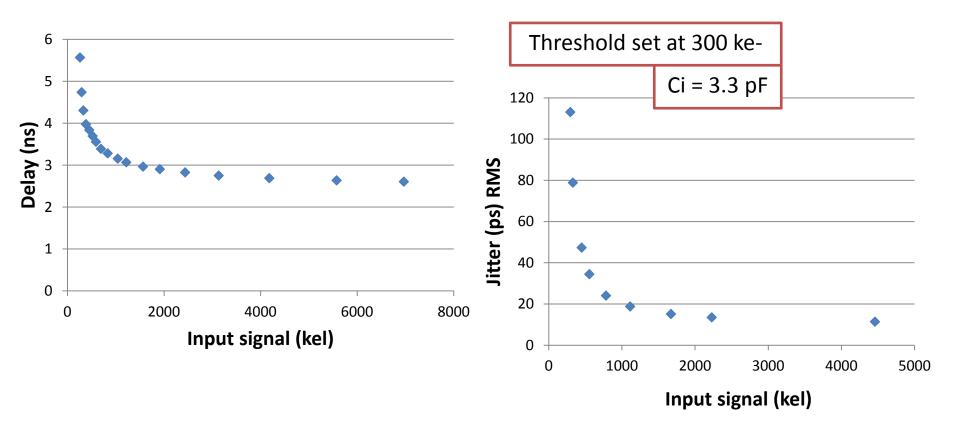




Timing performance

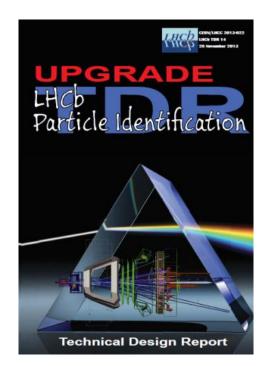
Excellent timing performance at 0.7 mW/channel:

- Time walk < 3 ns
- Leading edge jitter from 110 ps RMS (just above threshold) to 11 ps RMS (large signals)



Even better berformance could be achieved by doubling the power to 1.5 mW/channel.

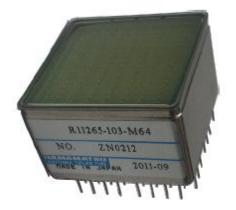
LHCb RICH upgrade

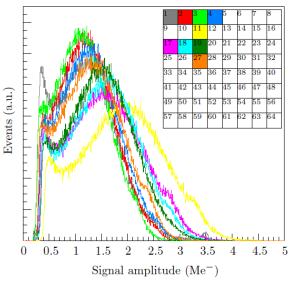


The CLARO was chosen as the baseline front-end ASIC for the upgrade of the LHCb RICH detectors.

The baseline photon sensors are Hamamatsu R11265 Ma-PMTs:

- Single photon peak at about 1 Me-
- Gain spread 1:3 between pixels





In the RICH upgrade electronics review in October 2013, a number of recommendations were raised, that will be implemented in the next design iteration.

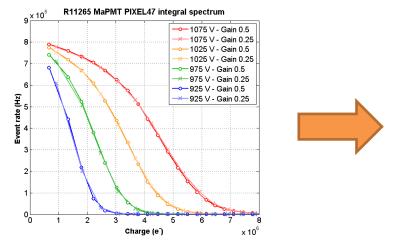
Requirements coming from the LHCb environment:

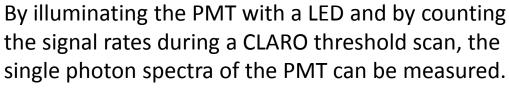
- Single photon counting at 40 MHz (no dead time at 25 ns) with the R11265 Ma-PMT
- Radiation hardness up to 10 kGy (1 Mrad) total dose, hadrons up to 10¹³ (n,p) cm⁻²

Tests with the R11265 Ma-PMT

A set of PCBs to interface the Hamamatsu R11265 Ma-PMT to the CLARO-CMOS prototype were designed and tested.

The design allows to minimize the stray capacitance at the inputs of the chip.

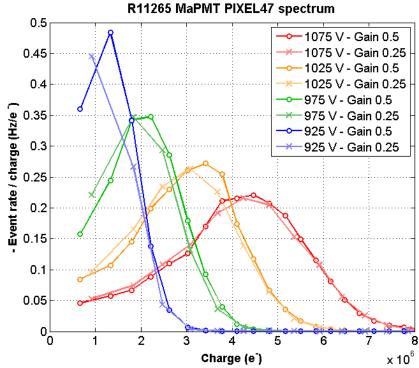




The spectra look good, the S/N ratio is more than adequate.

The next version will have a smaller threshold step, to allow finer scans.



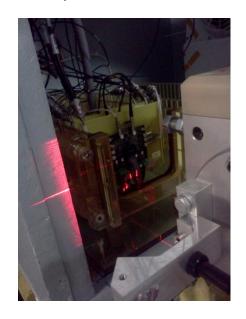


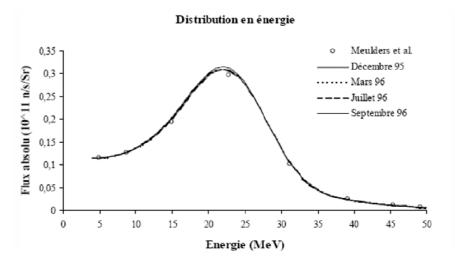
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Neutron irradiation

The neutron irradiation was performed in Louvain-la-neuve (Belgium) in May 2013.

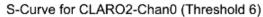


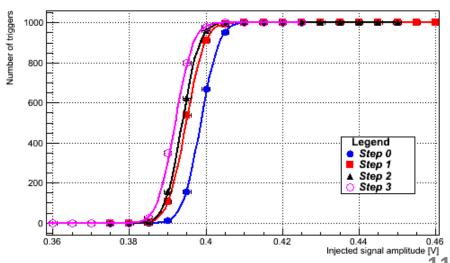




4 samples were powered and irradiated up to 10^{14} 1-Mev n cm⁻² (about 160 years in LHCb) in three steps.

- No SEU / SEL observed
- No variation in supply current
- No significant variation in thresholds and noise



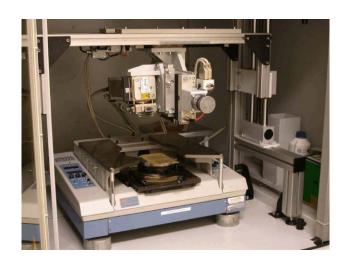


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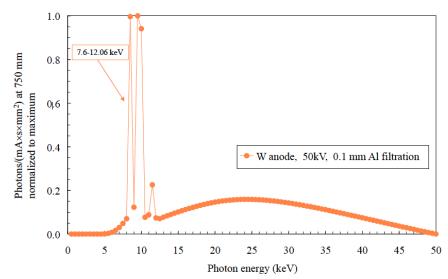
X-ray irradiation

The X-ray irradiation was performed in Legnaro (Italy) in September 2013.

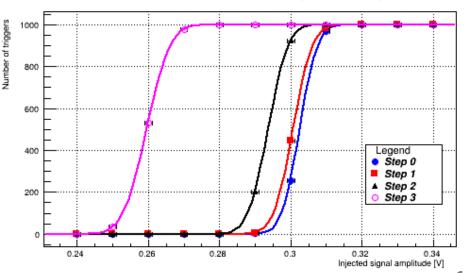


2 samples (with the package lid removed) were powered and irradiated up to 40 kGy (4 Mrad, about 110 years in LHCb) in three steps.

- No SEU / SEL observed
- 10-15% decrease in supply current
- 10-15% variation in channel threshold







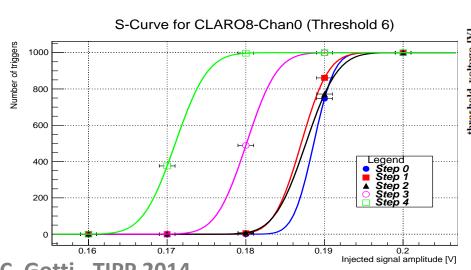
Proton irradiation

The proton irradiation was performed in Krakow (Poland) in February 2014.

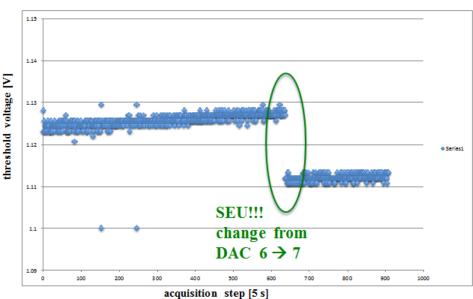
Beam energy: 60 MeV.

3 samples (with the lid removed) were powered and irradiated up to 76 kGy (7.6 Mrad, about 190 years in LHCb) in three steps.

- 1 SEU observed
- No SEL observed
- 10-15% decrease in supply current
- 10-15% variation in channel threshold







Towards the CLARO8

- The 4-channel CLARO-CMOS prototype demonstrated the capability of the chip, even if designed in a relatively old technology (0.35 microns), to count single photons from Ma-PMTs at a 40 MHz rate with a low power consumption (< 1 mW / channel).
- The technology tolerates radiation levels a factor of 10 larger than those foreseen in ten years of operation in the upgraded LHCb (10 kGy or 1 Mrad total dose, hadrons up to 10¹³ (n,p) cm⁻²)
- Moreover, a jitter in the order of tens of ps was demonstrated, enabling the use of the CLARO for precise timing measurements.

The next iteration of the design is the 8-channels CLARO8:

- Amplifier DC-coupled to the discriminator
- Finer threshold steps
- Configuration register protected against SEU by triple modular redundancy
- ...

The CLARO8 was designed earlier in 2014, and the first samples were received last week.



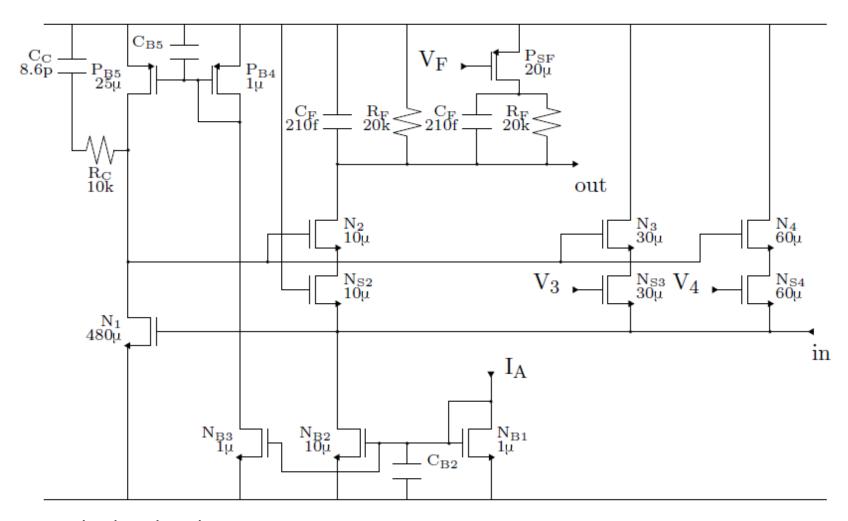
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Thank you

CLARO-CMOS full schematics (1)

Full schematic of the amplifier:

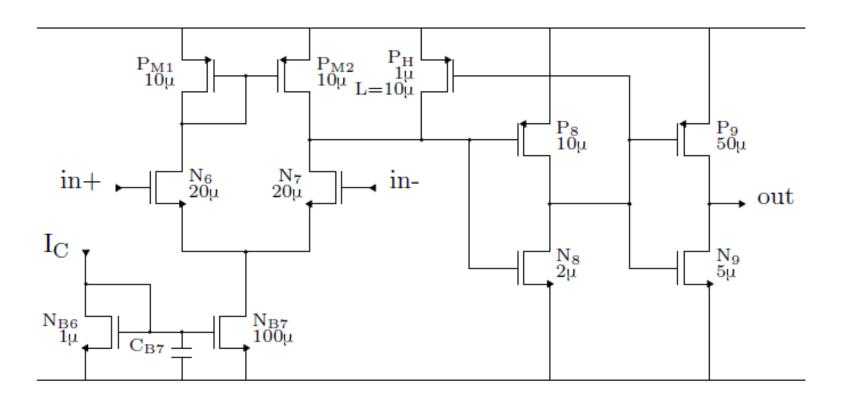


Described in detail in JINST 7 P11026

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CLARO-CMOS full schematics (2)

Full schematic of the discriminator:



Described in detail in JINST 7 P11026

More on timing performance

Test performed with a Agilent 81130° pattern generator and a Agilent DCA-X 86100D 1000 sampling oscilloscope. ---**△**-- Fall --▼-- Fall norm ··•• Overall 100 WWW Jitter (ps) CLARO-CMOS Step generator Sampling scope Trigger line 10 6 Low power mode «Low power»: 0.7 mW/ch y = -0.113x + 5.4875 Timing mode y = -0.055x + 3.7320.5 1000 4 · · • Rise Delay (ns) **…▲…** Fall ··•▼ · Fall norm • · · Overall 100 Jitter (ps) 300 ke (48 fC) 4.5 Me⁻ (720 fC) 10 «Timing» mode: 1.5 mW/ch 2530 5 10 15 20 Pulse width (ns) 0.54.5C. Gotti - TIPP 2014 18

Charge (Me⁻

Tests with SiPMs

Test performed with 1x1 mm² and 3x3 mm² devices.

Signals are slower because of the large input capacitance with respect to the design specification.

Nevertheless, signals corresponding to different numbers of photons can still be resolved.

