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CLARO-CMOS: a fast, low power and radiation-hard front-end ASIC for single-photon counting in 0.35 micron CMOS technology

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The CLARO-CMOS is a prototype ASIC that allows fast photon counting with 5 ns peaking time, a recovery time to baseline smaller than 25 ns, and a power consumption of about 1 mW per channel. This chip is capable of single-photon counting with multi-anode photomultiplier tubes (Ma-PMTs), and finds applications also in the read-out of silicon photomultipliers and microchannel plates. The prototype is realized in AMS 0.35 micron CMOS technology. In the LHCb RICH environment, over ten years of operation at the nominal luminosity expected after the upgrade in Long Shutdown 2, the ASIC must withstand a total fluence of about 6x10^12 1 MeV neq/cm2 and a total ionizing dose of 400 krad. A systematic evaluation of the radiation effects on the CLARO-CMOS performance is therefore crucial to ensure long-term stability of the electronics front-end.
The results of multi-step irradiation tests with neutrons up to the fluence of 10^14 1 MeV neq/cm^2, with protons up to the dose of 8 Mrad and with X-rays up to the dose of 8 Mrad are presented, including measurement of single event effects during irradiation and chip performance evaluation before and after each irradiation step.
In addition, systematic tests have been done on the single-photon counting performance of the CLARO-CMOS coupled to a Hamamatsu R11265 Ma-PMT, that is the baseline solution for the upgraded LHCb RICH photodetectors. Such results are presented as well.

Summary

The CLARO-CMOS is a prototype ASIC primarily designed for single-photon counting with multi-anode photomultipliers (Ma-PMTs). The chip allows fast photon counting up to 40 MHz with power consumption in the order of 1 mW per channel. It was developed in the framework of the LHCb RICH detectors upgrade at CERN, but also found application in the readout of Silicon photomultipliers (SiPMs) and microchannel plates (MCP-PMTs) [1,2].

The prototype has four channels, each made of a charge amplifier with settable gain (3 bits) and a comparator with settable threshold (5 bits) that allow tuning the response of the chip to the gain spread of the PMT pixels. The threshold can be set just above noise to allow an efficient single-photon counting with Ma-PMTs. In the readout of SiPMs, the threshold can be set above the single photon signals, allowing to count events with two or more photoelectrons with high efficiency and good separation of the photoelectron peaks.

The prototype is realized in a 0.35 micron CMOS technology. In the LHCb RICH environment, over ten years of operation at the nominal luminosity for the upgrade, the ASIC must withstand a total fluence of about 6x10^12 1 MeV neq/cm^2 and a total ionizing dose of 400 krad.

We present results of multi-step irradiation tests with neutrons up to the fluence of 10^14 1 MeV neq/cm^2, with protons up to the dose of 8 Mrad and with X-rays up to the dose of 8 Mrad. During irradiation, cumulative effects on the performance of the analog parts of the chip and single event effects (SEE) were evaluated. The chips were biased continuously and the chip threshold voltages were measured regularly, in order to detect possible single event upsets (SEUs) affecting the threshold DAC settings. Power consumption was

also monitored online, and an additional circuit provided protection against Single Event Latchup (SEL). A picture of one of the irradiation setups can be seen in Figure 1. S-curves were measured before and after each irradiation step, to follow the evolution of counting efficiency, threshold shifts and noise during the irradiation.

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Figure 1. Picture of the setup used to irradiate three CLARO-CMOS chips at the neutron irradiation line of the Université Catholique de Louvain Cyclotron Facility (Louvain-la-Neuve, Belgium). The visible cables are used for powering and configuring the chips, monitoring single event effects on-line and measuring chips performance.

The electrical performances of the CLARO-CMOS chip coupled to the Hamamatsu R11265 Ma-PMT are presented as well. For these tests a dedicated PCB was designed to connect the chips to the Ma-PMT with minimal contribution of parasitic capacitances at the input, and allowed to obtain very low noise and crosstalk. This readout scheme simulates the baseline read-out solution for the upgraded RICH detectors of the LHCb experiment. To mimic the conditions expected in the upgraded LHCb RICH environment, single photons in the blue range were generated using LED and diode laser. The speed of the CLARO signals and the low power consumption were demonstrated. Single-photon spectra from the Ma-PMT pixels were nicely reconstructed with a threshold scan, showing that the binary outputs allow precise characterization of the Ma-PMT. Also, crosstalk between neighboring pixels was shown to be negligible.

References:

1 P. Carniti et al., “CLARO-CMOS, a very low power ASIC for fast photon counting with pixellated photodetectors”, Journal of Instrumentation 7 (2012) P11026

[2] P. Carniti et al., “CLARO-CMOS, an ASIC for single photon counting with Ma-PMTs, MCPs and SiPMs”, Journal of Instrumentation 8 (2013) C01029

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