Total Ionization Damage Compensations in Double Silicon-on-Insulator(SOI) Pixel Sensors

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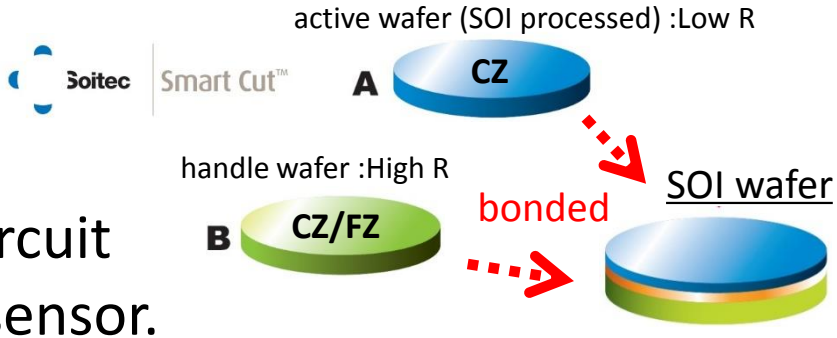
✓ **related presentations**:
T. Miyoshi et al. : Monolithic pixel detectors fabricated with single and double SOI wafers
A. Takeda et al. : Development and Evaluation of Event-Driven SOI Pixel Detector for X-ray Astronomy
H. Matsumura et al. : Development of X-ray SOI Pixel Sensors: Investigation of Charge-Collection Efficiency
K. Kasahara et al. : Development of Superconducting Tunnel Junction Photon Detector on SOI Preamplifier Board to Search for Radiative decays of Cosmic Background Neutrino

SOI Pixel Sensors

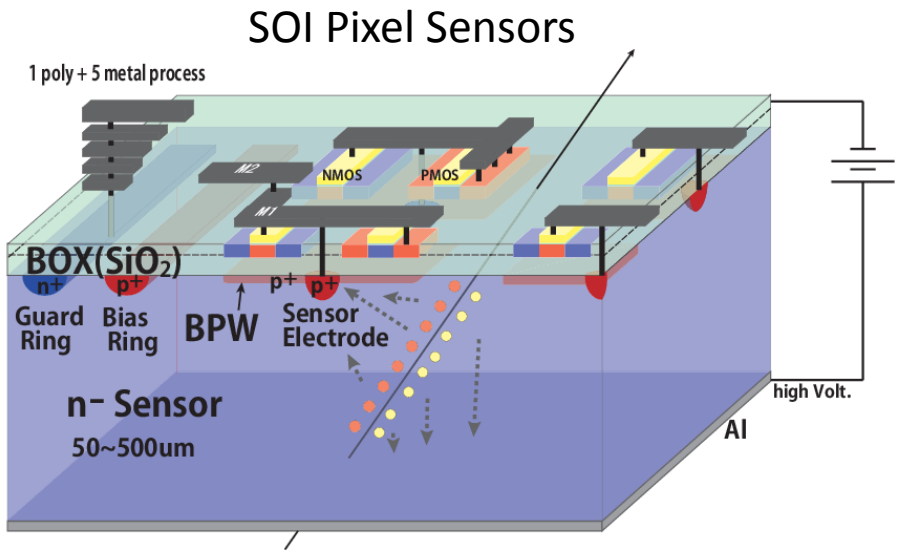
Technology characteristics:



- ✓ Bonded SOI wafers by SOITEC Co. with low resistive “active wafer” for circuit and high resistive “handle wafer” for sensor.
- ✓ Commercial Fully-Depleted(FD) SOI process (0.20μm) by Lapis Semiconductor Ltd.

Pros:

- **bonded wafer**
  thick X-ray, thin HEP :fully depleted
- **FD-SOI features**
  low-power, hi-speed, no latch-up,
  <1K-300C operational
- **monolithic (no metal-bonding)**
  fab. cost, small material, high density pixels



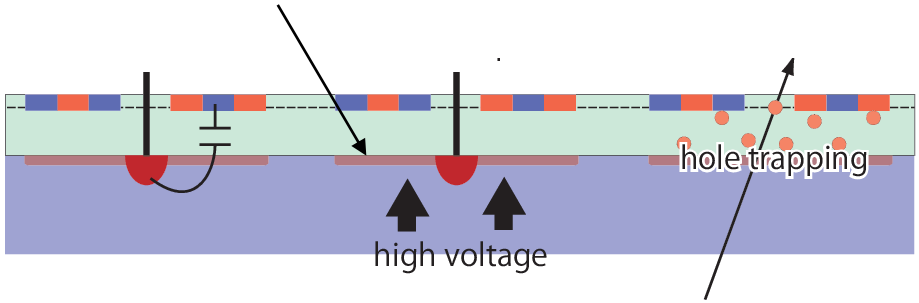
SOI Pixel Sensors

Cons:

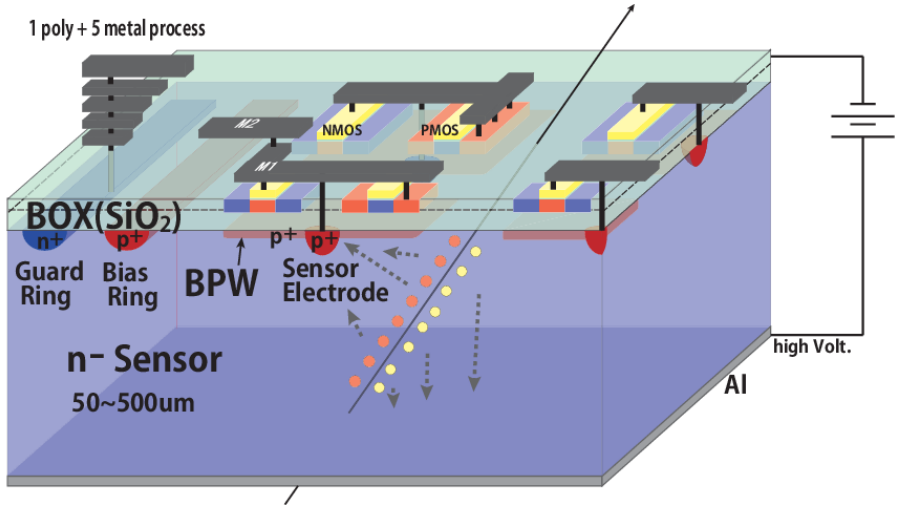
- **cross-talk between the sensor and the circuit**
  because of very thin BOX layer: 200nm
- **back-gate effect**
  readout affected by bias voltage to the back
- **radiation effect - TID effect**
  readout affected by holes trapped in BOX layer

BPW(Buried P-Well) is effective to reduce the back-gate effect

- increase capacitance……



SOI Pixel Sensors



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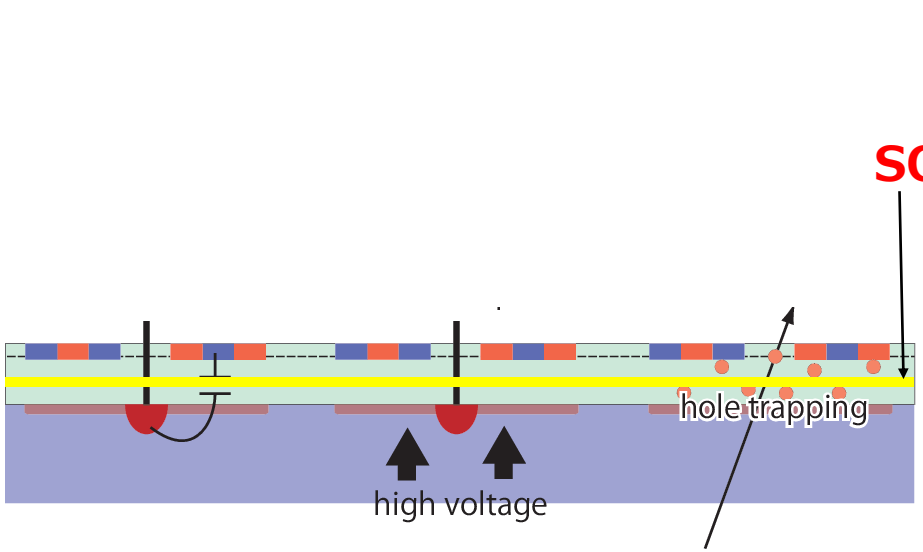
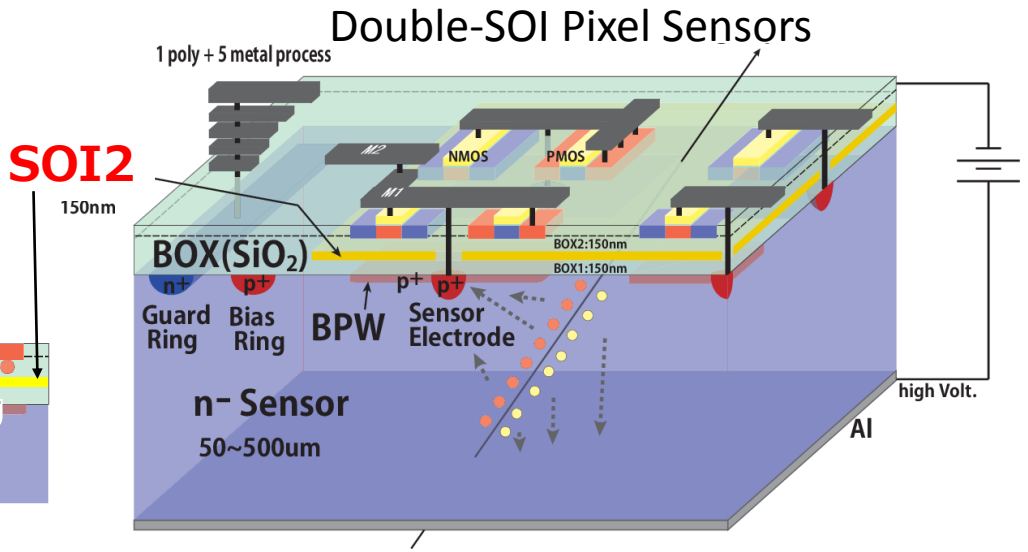
- **radiation effect - TID effect**
  readout affected by holes trapped in BOX layer

To solve these cons, **Innovative Double-SOI (SOI2 layer) is introduced!!**

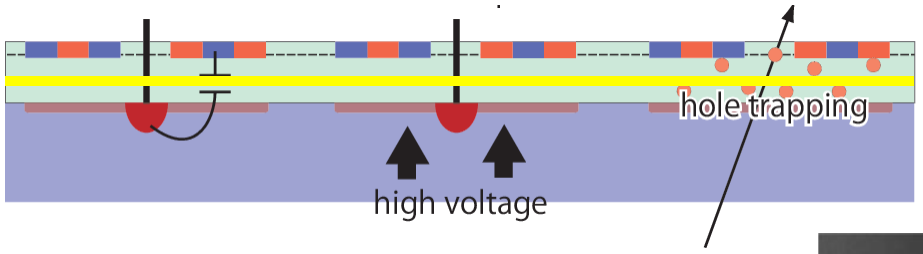




Double-SOI process

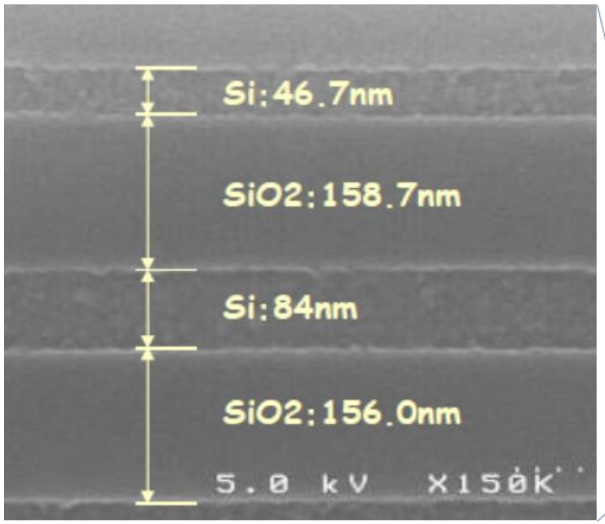
2nd Si layer (SOI2) made by SOI-process twice

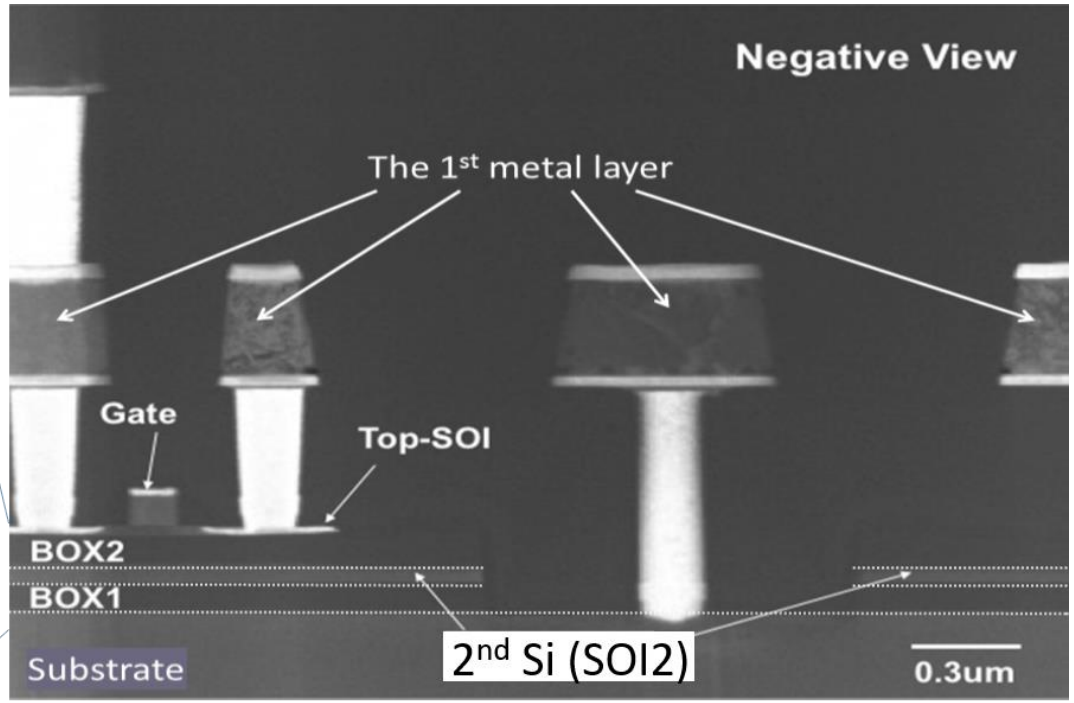
- ✓ shield against cross-talk & back-gate effect : **NOW IN PROGRESS**
- ✓ V control to compensate trapped hole charge : **TODAY'S TALK**



SOI2

ρ_{SOI2}~10Ωcm with CoSi2: ~170kΩ/sq
w/o CoSi2: ~1MΩ/sq

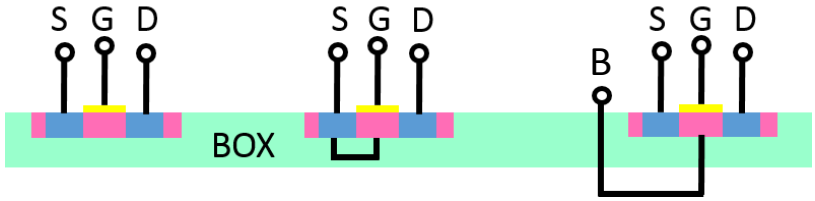




Transistor Test Elements Groups (TrTEG)

TrTEG6 : 3kGy – 2MGy (200Mrad)

18 species each for NMOS/PMOS
-- several L, W (Weff=Wxm).
-- low, normal, high threshold volt.
-- 3 kinds of body connections.

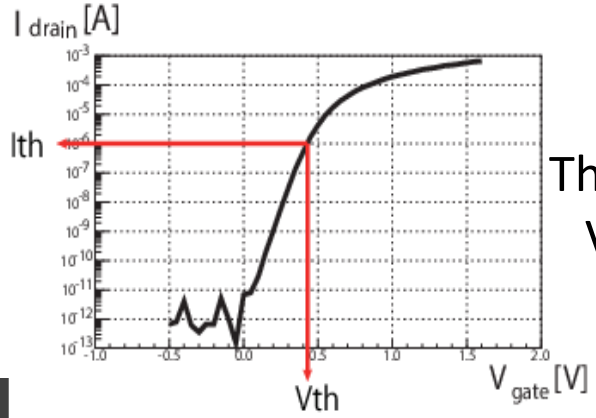


body floating	source-tie	multi-body-tie
(bf)	- type1(s-tie) - type2(s-tie2)	can be applied a variable volt. (multib-tie)

Total dose in high energy physics experiments
LHC(HL-LHC) ATLAS - Inner Pixel Detector
:**158 kGy/yr (1.6 MGy/yr)**
ILC ILD - Vertex Detector
:**1 kGy/yr**

L[um]	W[um]	m	Comment
0.20	5	4	nvt_bf
0.50	5	10	nvt_bf
1.00	5	20	nvt_bf
0.20	5	4	lvt_bf
0.50	5	10	lvt_bf
1.00	5	20	lvt_bf
0.35	5	7	iohvt_bf
0.35	5	7	iohvt_bf
0.20	5	4	lvt_s-tie
0.50	5	10	lvt_s-tie
1.00	5	20	lvt_s-tie
0.40	10	4	nvt_s-tie2
0.60	6	10	nvt_s-tie2
1.00	5	20	nvt_s-tie2
0.20	5	4	nvt_multib-tie
0.50	5	10	nvt_multib-tie
1.00	5	20	nvt_multib-tie
1.00	5	20	ios-tie

Measure Id-Vg curve before/after irradiations.



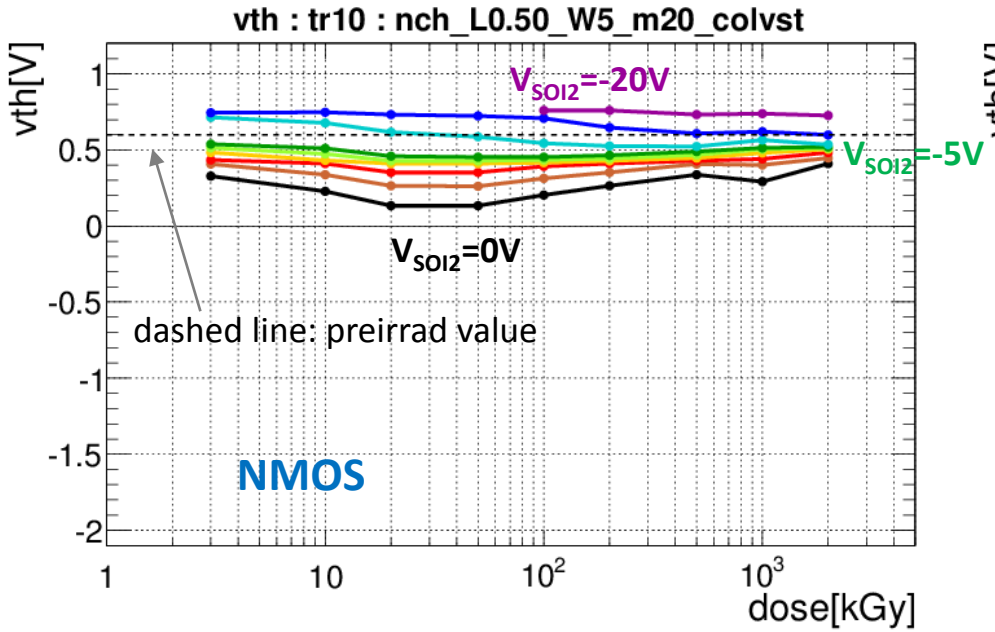
Threshold (Vth):
Vg@Id=(100nA)x(Weff/L)

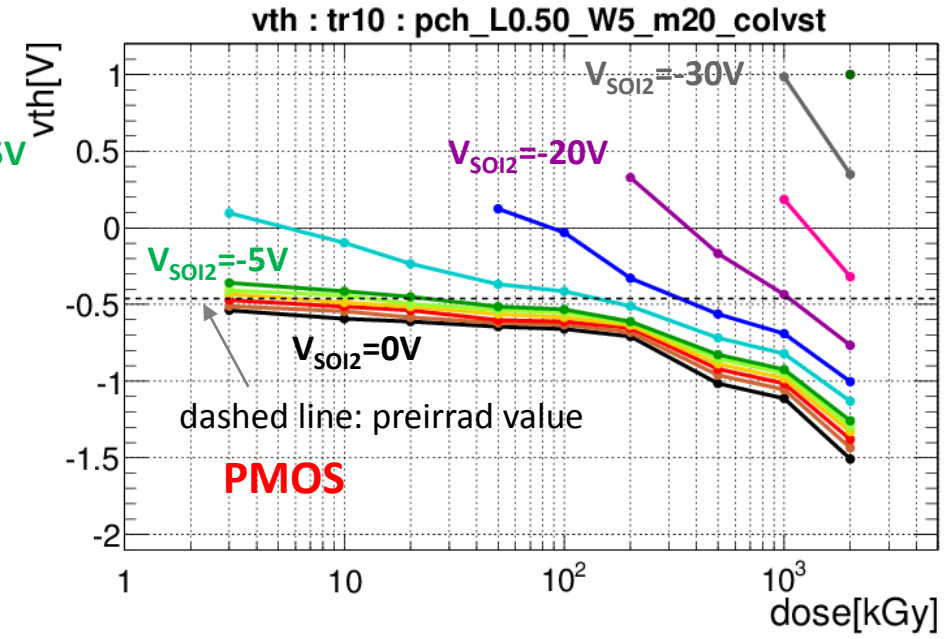
TrTEG6
Vth Shifts – typical TR

tr10 : L0.5_W5_m20_colvst

Thresholds shift negatively due to holes by irradiation.

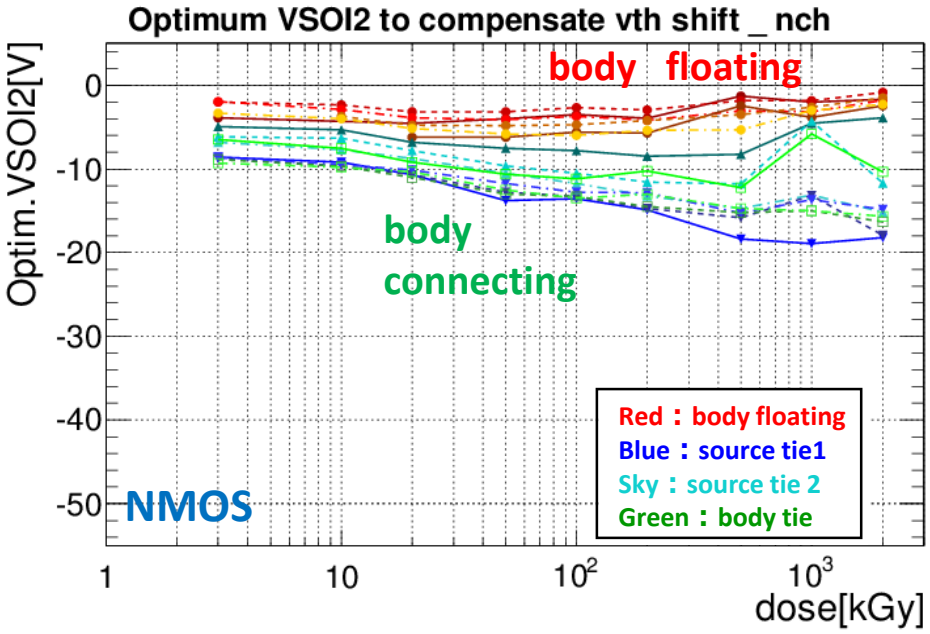
By applying V_{SOI2} properly,
the threshold can be recovered to the pre-irrad value.

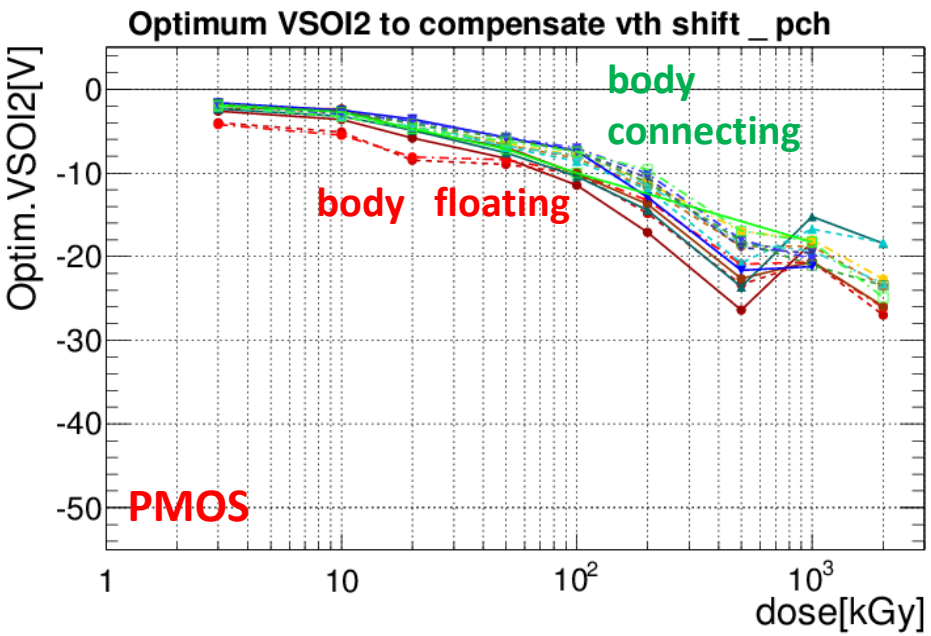




TrTEG6
Vth Shifts – all TR types

Optimum V_{SOI2}: V_{SOI2} per dose to recover the transistor thresholds to the pre-irrad values measured at VSOI2=0



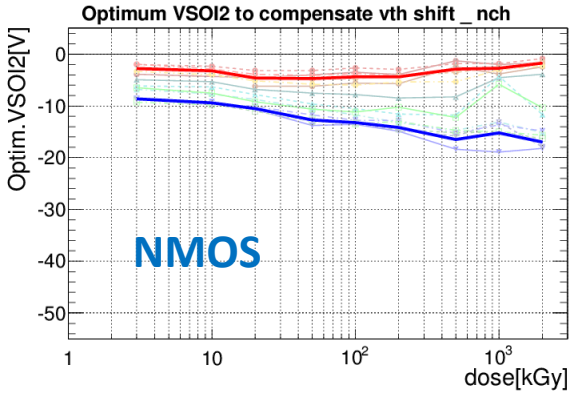


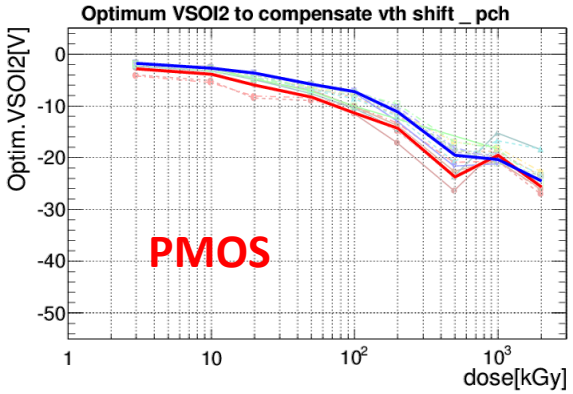
Noticeable differences are observed between NMOS & PMOS TRs, among body connections notably in NMOS.

Separate V_{SOI2} settings may be optimum to compensate TID.

-example case: 4-voltages for NMOS/PMOS, bf/s-tie2. (s-tie1,b-tie are not considered)

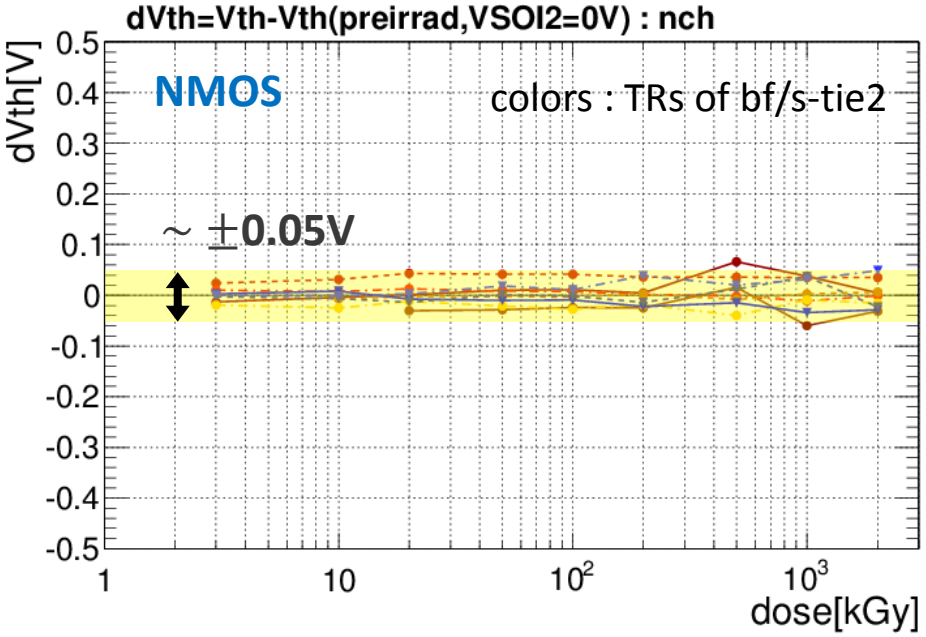
TrTEG6
Vth Compensation-example case

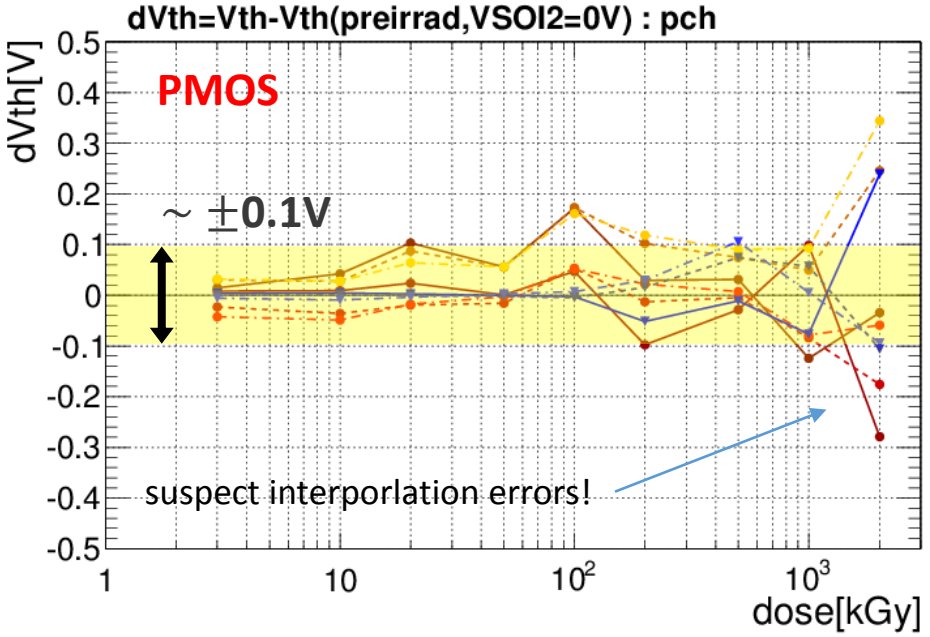




Red : average of body floating TRs
Blue : average of source tie2 TRs

Applying the 4 average curves for each V_{SOI2} type,
transistors are recovered in the range of ±0.05V for NMOS, ±0.1V for PMOS





Pixel Sensor (INTPIX)

INTPIXh2:10kGy-100kGy (10Mrad)

Integrated-type pixel sensor
-Pixel Size: 18um x 18um
-Handle: Cz(n,0.7kΩcm)
-SOI2(common to all TRs): Cz(p,10Ωcm)
-BPW(for shield back-bias effects) : GNDed

Total dose in high energy physics experiments
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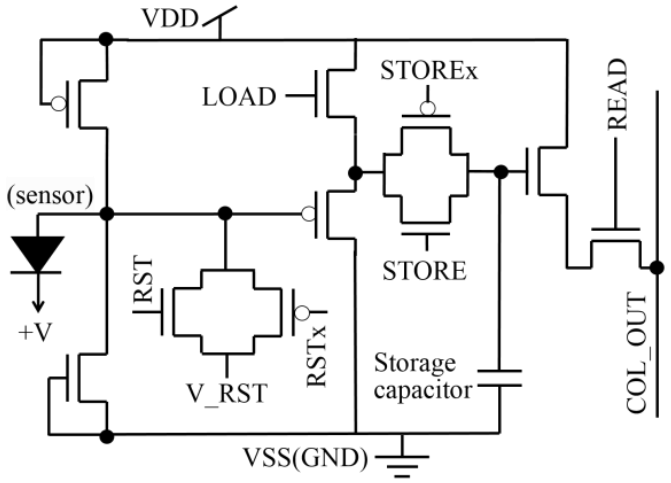
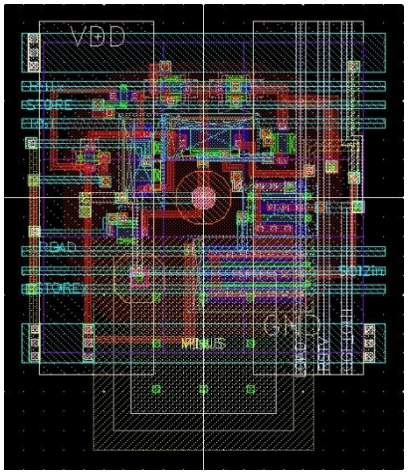
:**1 kGy/yr**



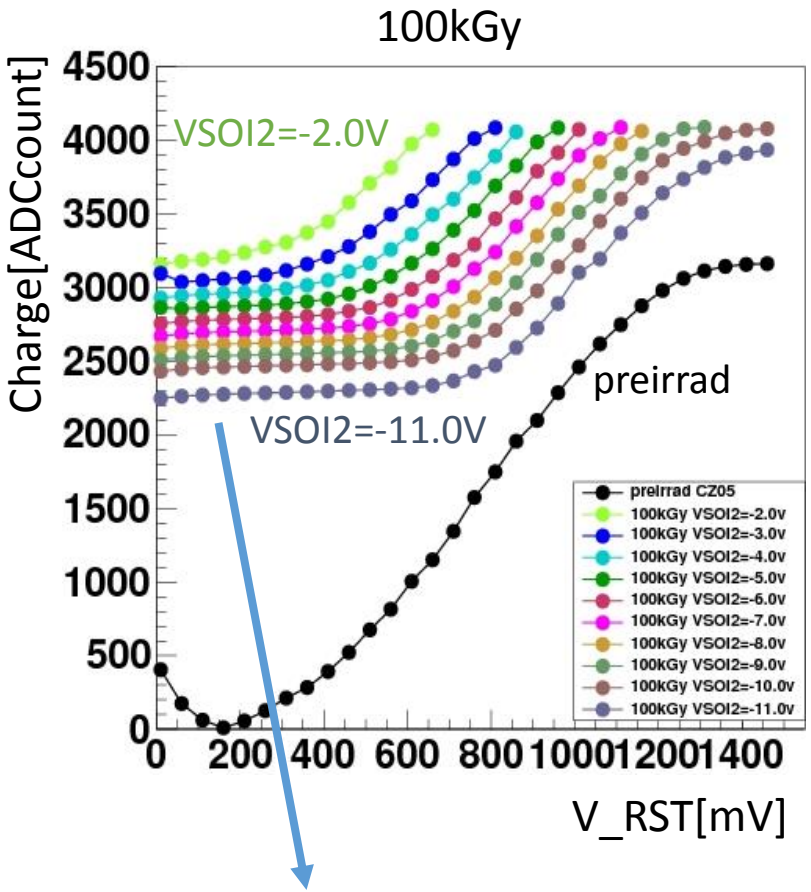
on-pixel circuit

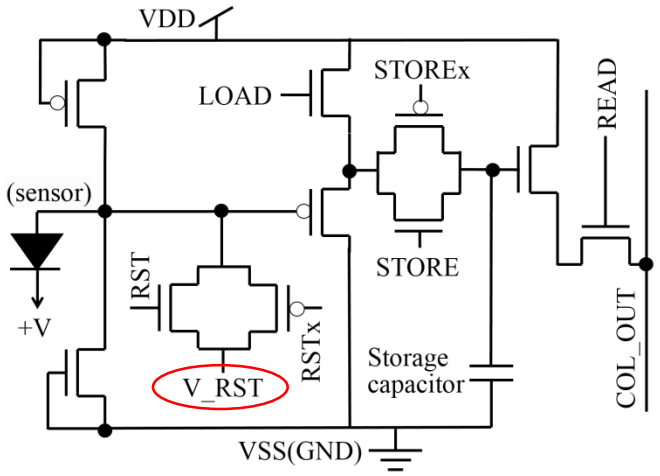


Evaluate the functionality of electronics & response to IR-laser.

INTPIXh2
Reset Voltage Response

The functionality of electronics by "injecting" RESET voltage(V_RST).





The sensor irradiated to 100kGy is recovered its functionality by V_{SOI2}.

But continuous calibrations per dose are required…

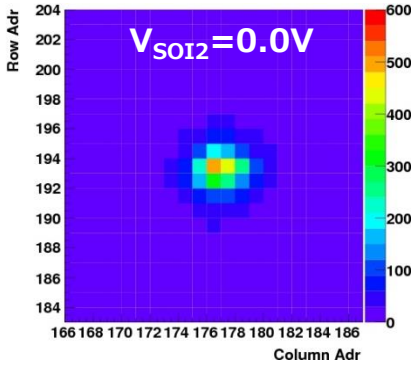
Dynamic range is not fully recovered : single V_{SOI2} is employed.

V_{SOI2} depending on transistor type is preferred.

INTPIXh2
IR-Laser Response

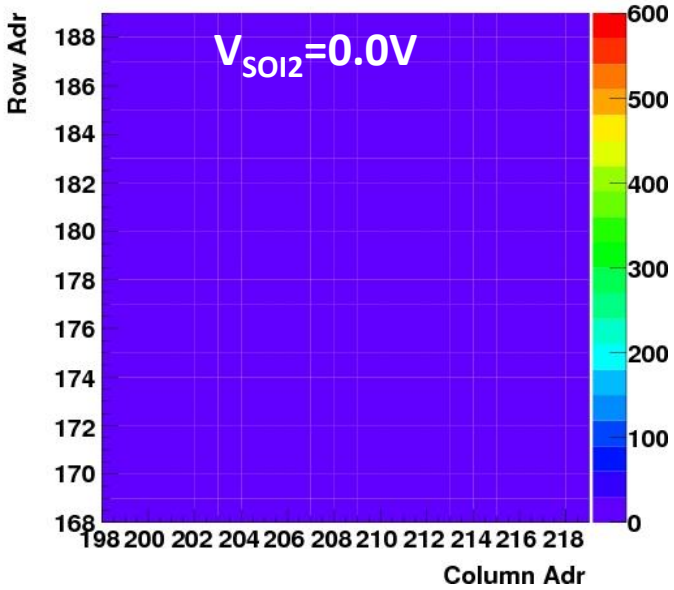
IR-Laser : 1064nm, 10ns pulse

pre-irrad sample

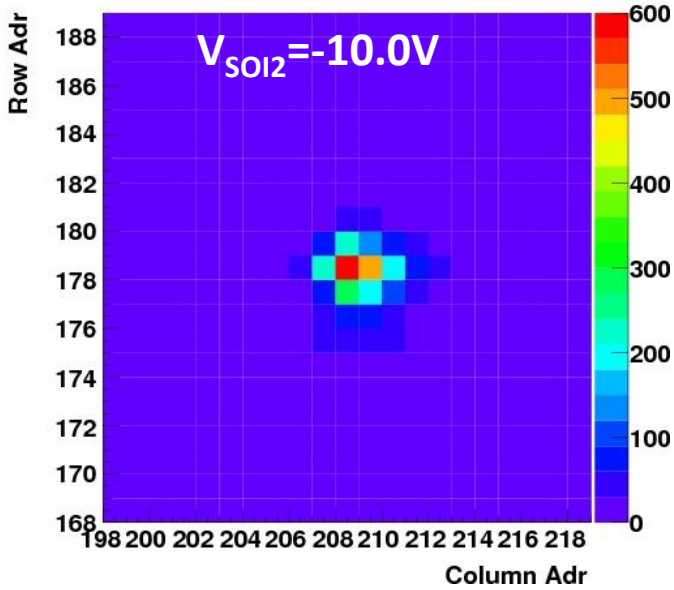


Light Image = ADC(light) – ADC(pedestal)
- Int. time : 120ns
- back bias voltage : 100V
- reset voltage: 0.85V

100kGy sample



The response is almost saturated…

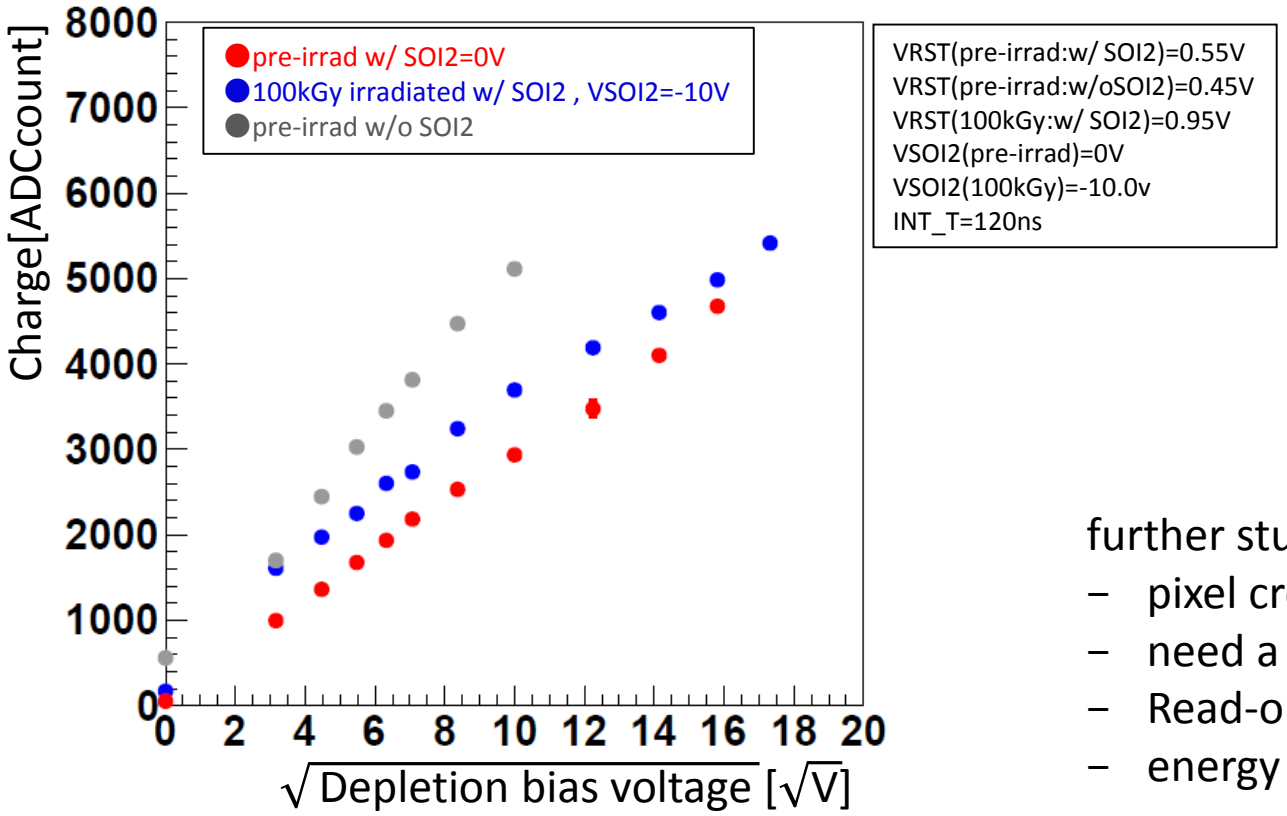


The image is obtained !

INTPIXh2
IR-Laser Response: ADC curve

Even after irradiated up to 100kGy,
obtained the same linearity and sensitivity as pre-irrad one.

Single-wafer sensor(w/o SOI2) has a higher gain than double-SOI-wafer one.
(due to smaller SOI2-sensor capacitance)



further studies are now in progress on
- pixel cross talk
- need a higher gain ?
- Read-out buffer response w/ SOI2
- energy peak of γ-ray sources ……

Summary

We are developing SOI pixel sensors for high energy physics.

Double-SOI can compensate the TID.

- Threshold voltage of transistors is recoverable.
- Sensor response is also recoverable.

(Data with higher doses will come soon!)

- The optimum V_{SOI2} are different among NMOS/PMOS, body-connections ….
- Design based on the obtained information is next step to further minimize TID effects.
- Other SOI2 properties are being evaluated.

By employing innovative double SOI technology, the radiation tolerance (TID) has been enhanced substantially.

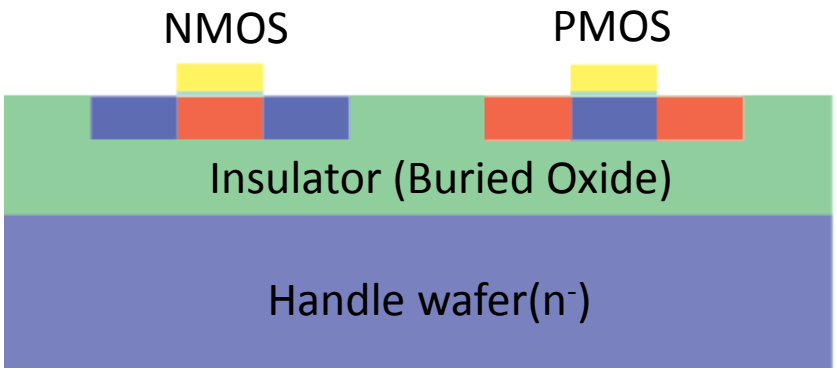
Designing pixel sensors for future collider experiments is set forward

BACK UP >>>

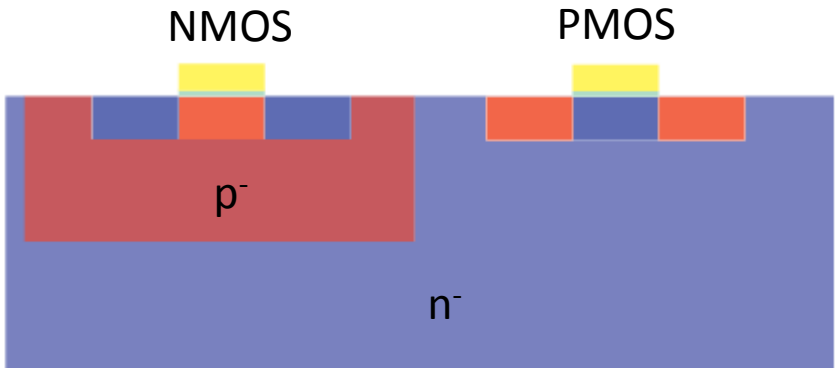
Fully-Depleted Silicon-on-Insulator(SOI) Technology

SOI – Transistors are isolated by the insulator.

FD – No parasitic capacitance.

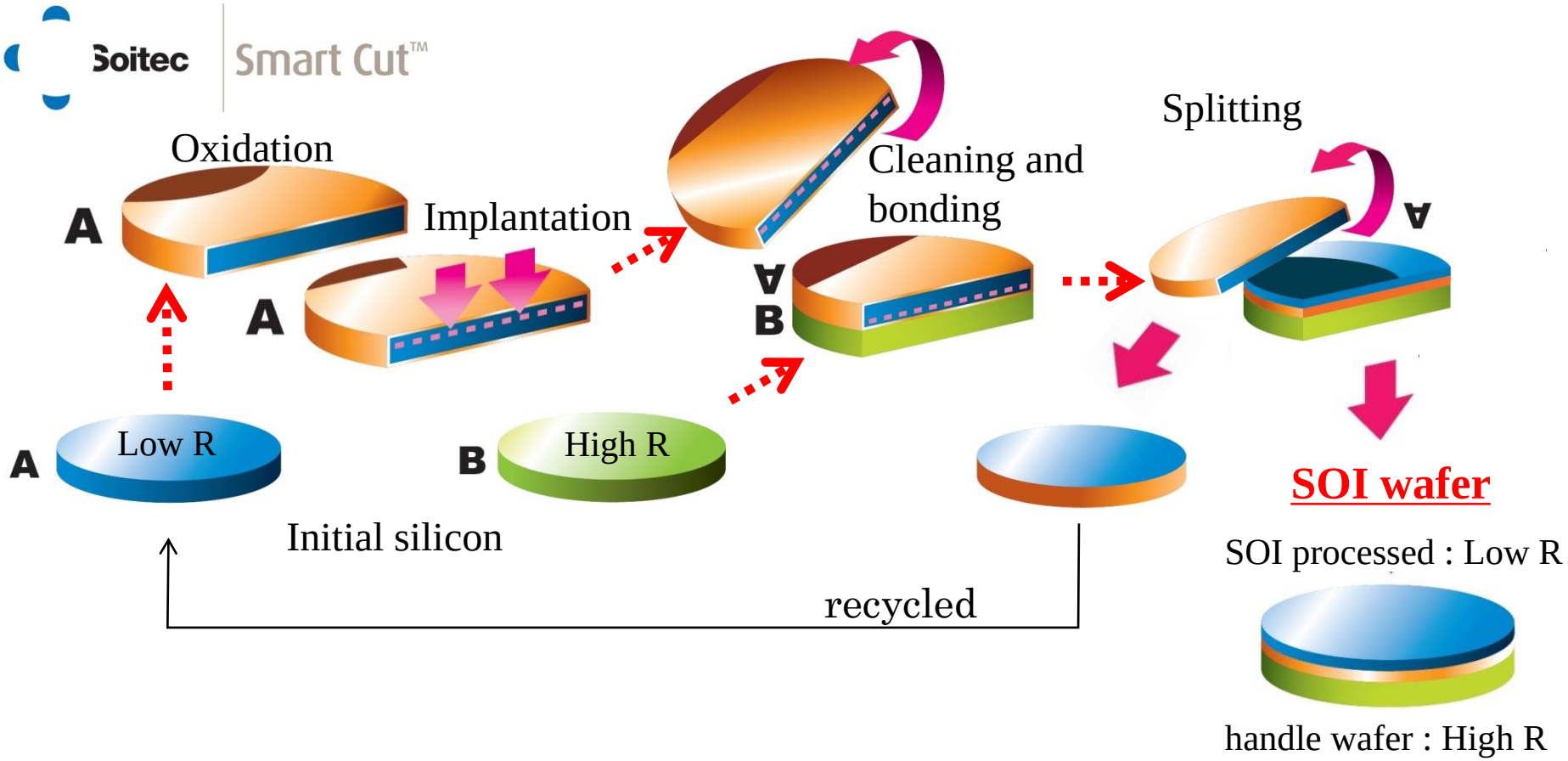


SOI-CMOS



Bulk-CMOS

SOI Wafer Production



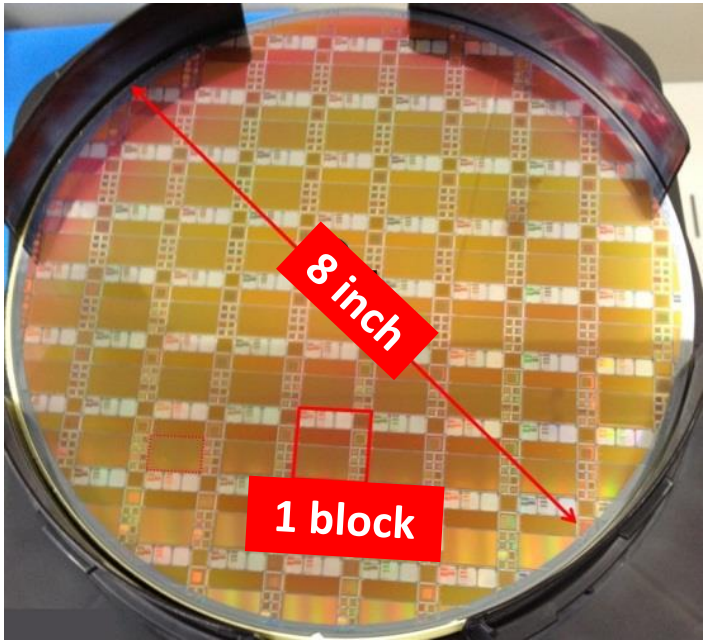
Main process parameters (Lapis Semiconductor Co. Ltd.):

Process	0.2µm Low-leakage Fully-Depleted SOI CMOS 1poly+5Metal layers, MIM cap(1.5fF/mm^2), DMOS Core (I/O) voltage=1.8 (3.3)V
SOI wafer	200mmf, 720µmthick top Si: Cz 18Ωcm p, 40nm thick, Buried Oxide(BOX): 200nm thick Handle wafer: Cz(n;0.7kΩcm), FZ(n;7k), FZ(p,25k) **Double SOI available**
Backside process	Mechanical grind, chemical etching, Implant, Laser annealing, Al plating (thin to 50mm possible)

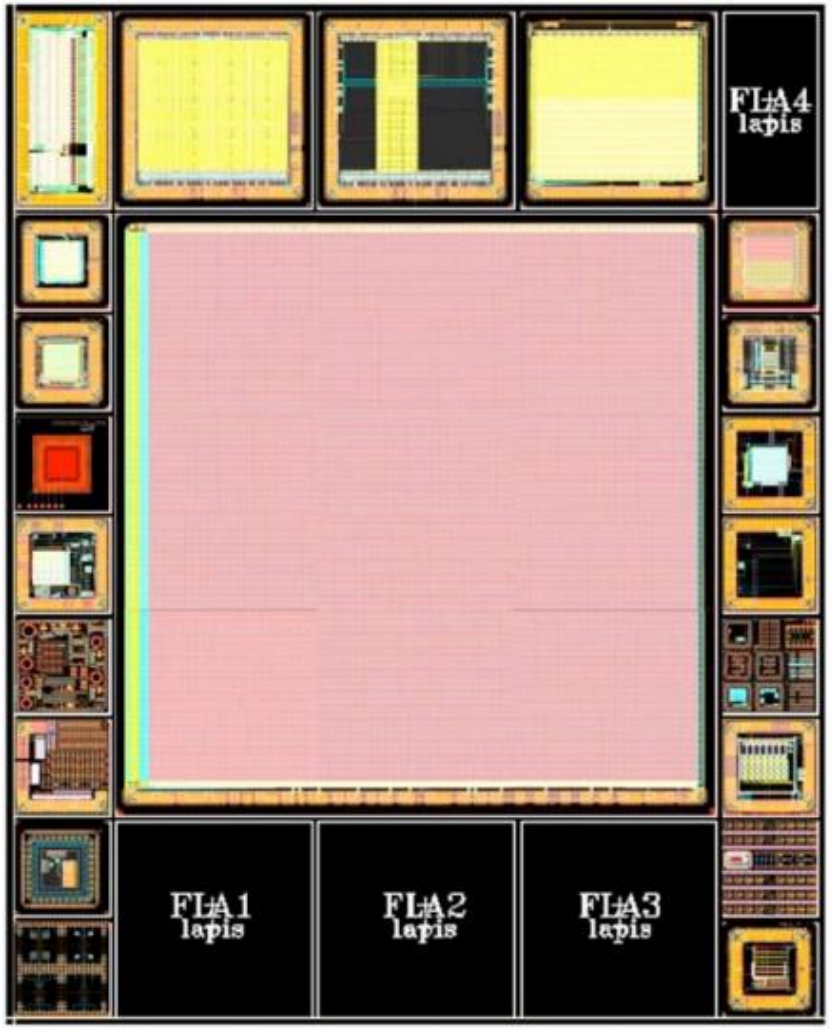
Multi Project Wafer(MPW)

- KEK organizes MPW runs twice a year
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip
  - University & institution

KEK, FNAL, LBNL, AIST, CNS, Kyoto Univ., Tohoku Univ., Univ. Tsukuba, RIKEN-XFEL, JAXA, Krakow, Hawaii, IHEP, and more…

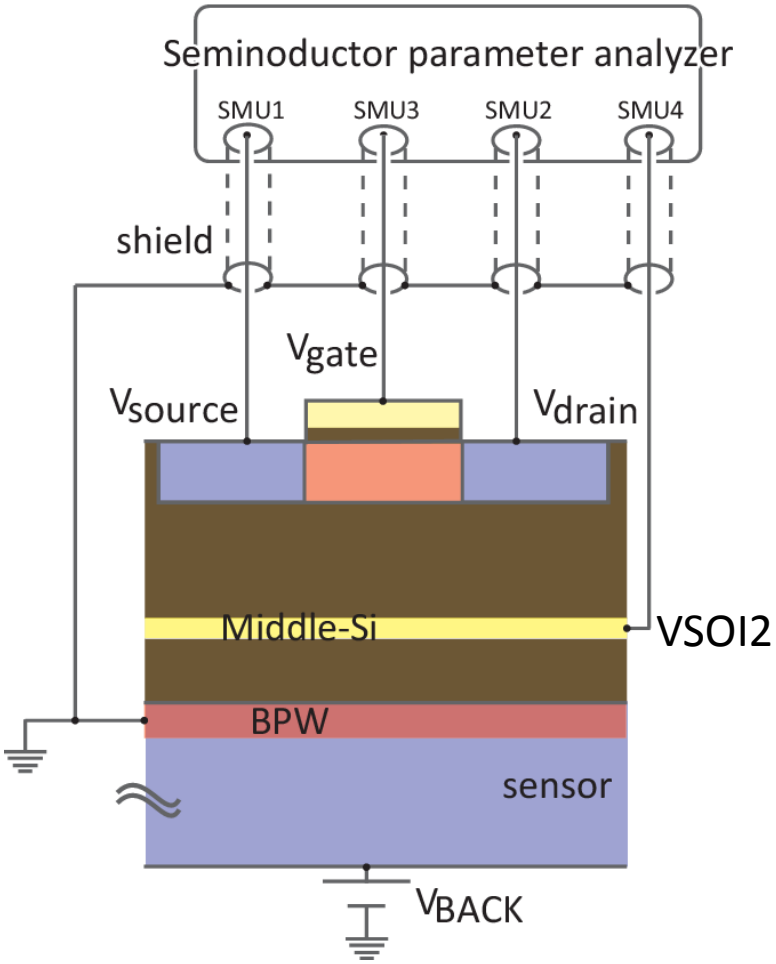


SOI-wafer

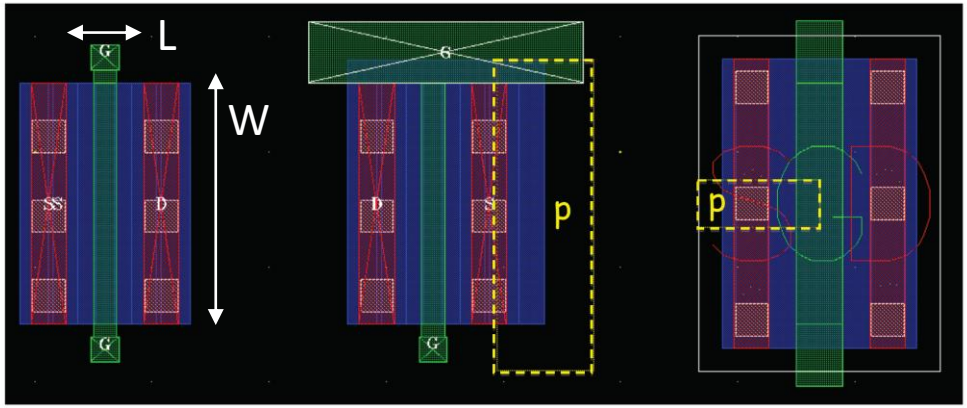


Examples of Mask layouts. : 20.6mm x 20.6mm

TRTEG6 body connections



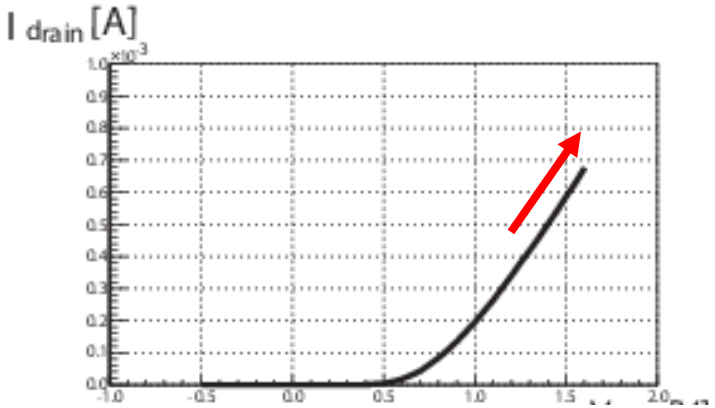
Body Floating Source-tie Source-tie2



NMOS
Vsource=0V
Vdrain= 1.8V
Vgate=-1.0～1.7V
VBPW=GND
VSOI2=0V～-20V

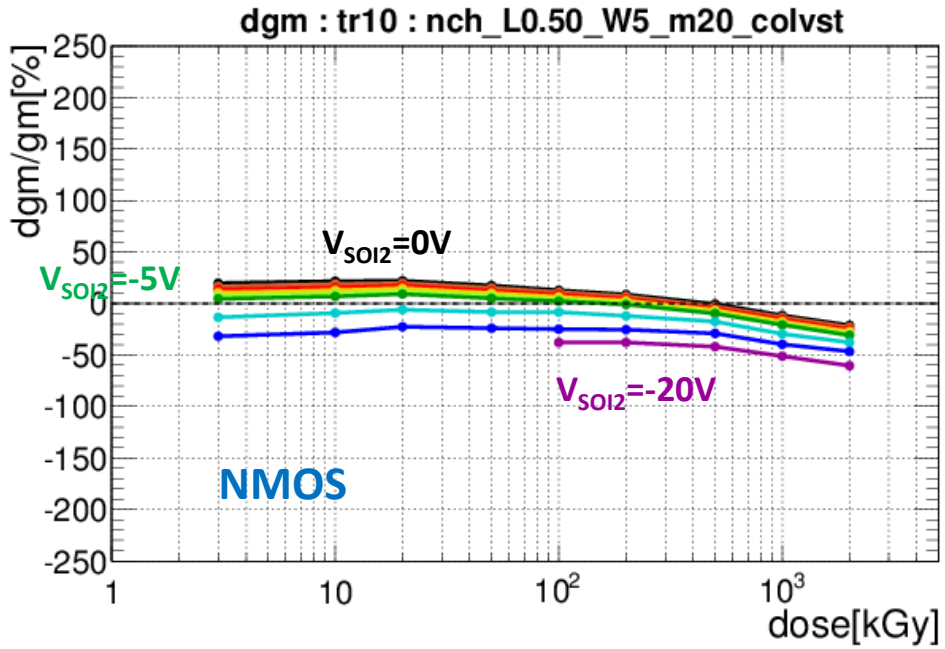
PMOS
Vsource=1.8V
Vdrain= 0V
Vgate=2.8～0.1V
VBPW=GND
VSOI2=0V～-40V

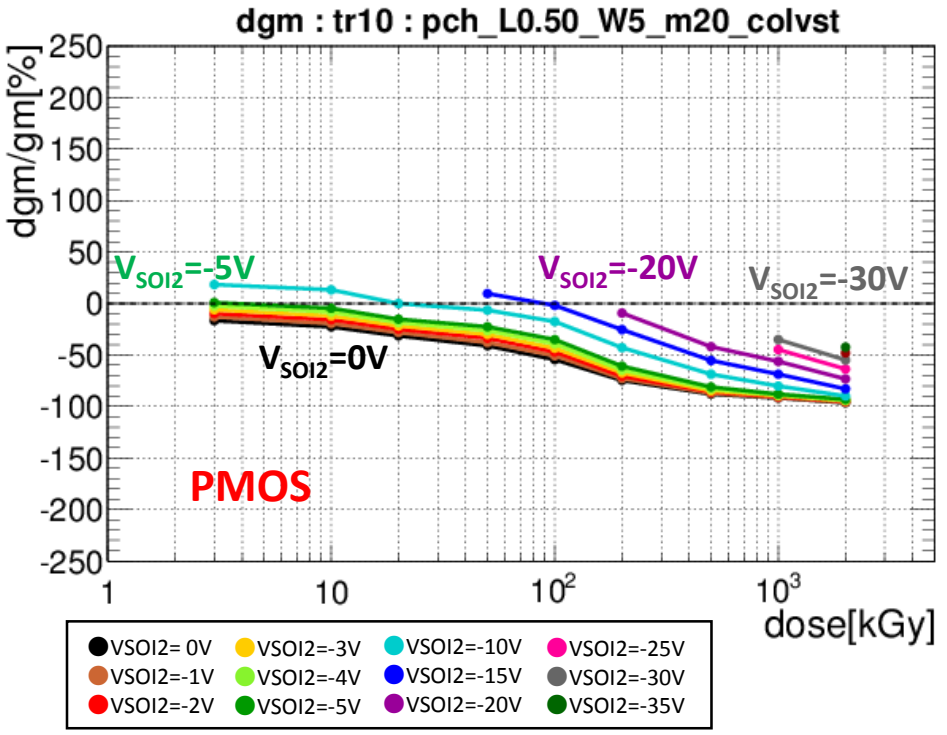
TrTEG6
gm shifts - typical TR



Trans conductance(gm)
= (Id/Vg) @linear region

The gm shift are more complicated than vth.
The gm can be recovered to some extent.





Pixel Readout - FPGA