Development of CMOS Pixel Sensor Featuring Pixel-Level Discrimination for the ALICE-ITS Upgrade

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(on behalf of the PICSEL group of IPHC-Strasbourg)

Outline

- ***CMOS pixel sensor: from the STAR-PXL to the ALICE-ITS upgrade***
- ***The R&D road map towards the ASTRAL sensor***
  - ***AROM-0: feasibility study***
  - ***AROM-1: further optimization***
  - ***FSBB-A0: first prototype of full scale building block for ASTRAL***
- ***Summary and conclusions***

From STAR-PXL to ALICE-ITS upgrade

- ***ULTIMATE (MIMOSA 28) for the STAR-PXL detector***
  - *Fabricated in 0.35µm CMOS process*
  - *Active area as large as ~ 3.8cm^2 (with 20.7µm square pixels)*
  - *Rolling shutter readout analogue pixels + column level discriminators + zero suppressed output*
  - *t_{int} ~ 200µs & power dissipation ~ 150mW/cm^2*
  - *The STAR-PXL detector is taking physics data since early March 2014*
  - *The first vertex detector equipped with CMOS pixel sensor (CPS)*
- ***ALICE-ITS upgrade has called for more demanding sensor performances***

Expt-System	σ_t	σ_{sp}	TID	Fluence	T_{op}
STAR-PXL	≤ 200µs	~5µm	150kRad	$3 \cdot 10^{12} n_{eq}/cm^2$	30°C
ALICE-ITS	***10~30µs***	~5µm	***700kRad***	***$10^{13} n_{eq}/cm^2$***	30°C

=> Moving to the TowerJazz 0,18µm CIS quadruple well process

✓ *Radiation tolerance*
- *High resistivity sensitive volume*
- *Thinner gate oxide*
- *Validated for ALICE-ITS upgrade*

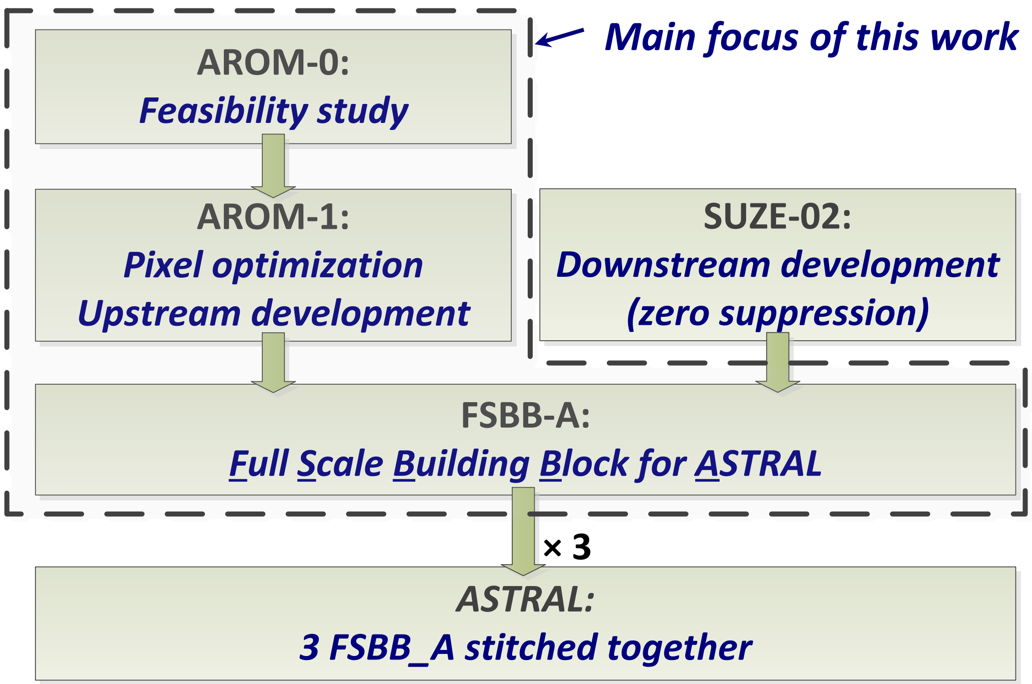
✓ *Speed*
- *More parallelized readout (multiple-row readout)*
- *Elongated pixels (less rows to be readout)*
- *Finding new pixel structures*

  => High µ-circuits integration

  => Deep-Pwell: full CMOS integration in pixel

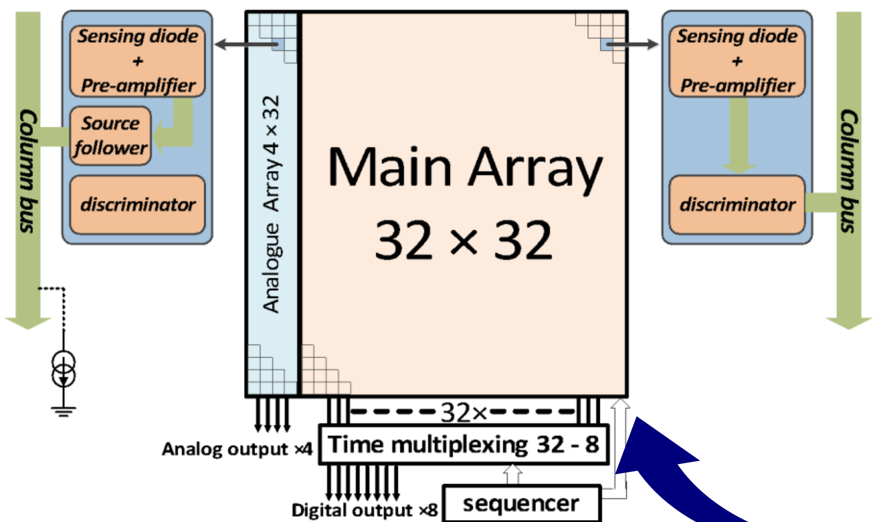
From STAR-PXL to ALICE-ITS upgrade

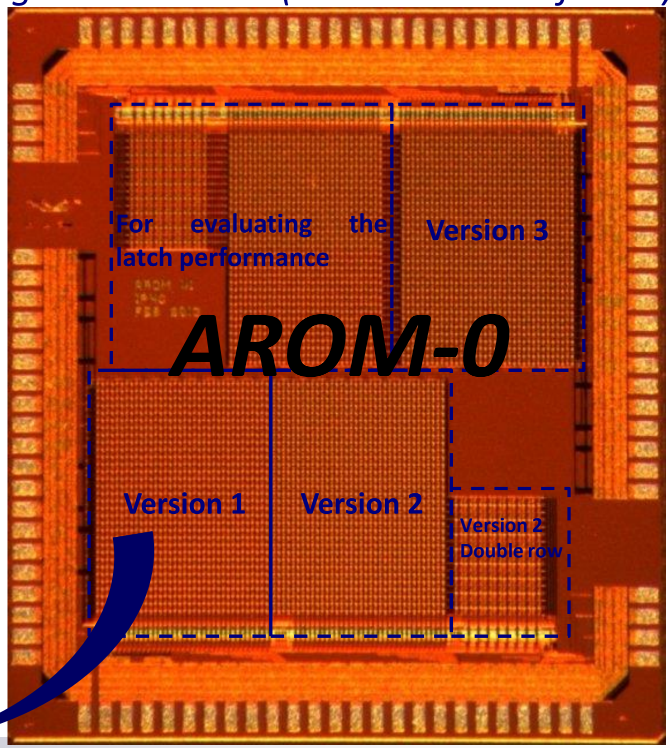
- AROM (Accelerated Read-Out Mimosa) sensor with pixel-level discrimination
  - *Analogue buffer driving the long distance column line is no longer needed*
    - *Static current consumption reduced from ~120 μA (in column-level discrimination) to ~14 μA per pixel*
  - *A-D conversion time can be halved down to 100ns due to small local parasitic*
- R&D roadmap based on the AROM sensor for the ALICE-ITS upgrade
  - *Our final goal: ASTRAL (AROM Sensor for the inner TRacker of ALICE)*
  - *One of the proposals for this application*



Description of AROM-0 (1/2)

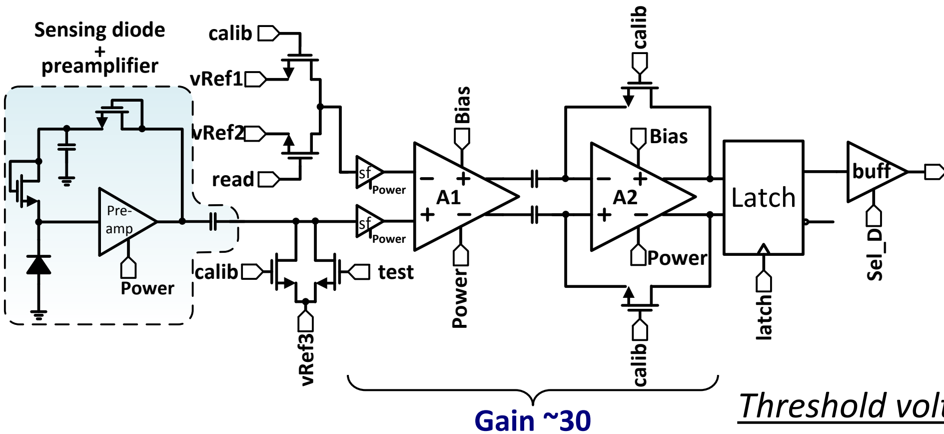
- ***Chip overview***
  - *6 sub-matrices*
  - *Pixel pitch: 22x33 μm² = > driven by the requirement of the ALICE-ITS upgrade*
  - *Each pixel contains a sensing diode, a pre-amplifier and a discriminator*
  - *Validated sensing and pre-amplifying components (MIMOSA 32, MIMOSA 32TER)*
  - *Three different topologies of discriminators*
  - *Both single row (matrix of 32×32) and double row readout (matrix of 16×16) are implemented*
  - *4 extra columns alongside the 32×32 matrices for analogue calibration (C-V conversion factor)*
  - *Compared to the column level discrimination*
    - *Twice as fast*
    - *Less than half of the pixel static current consumption*

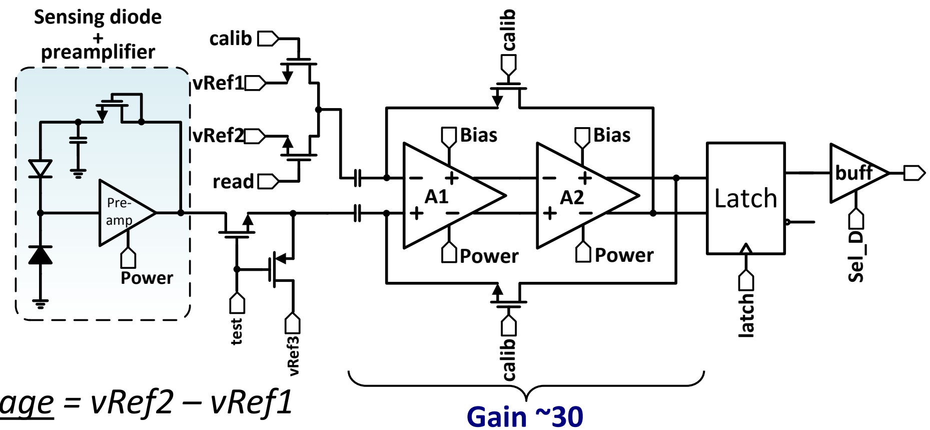




Description of AROM-0 (2/2)

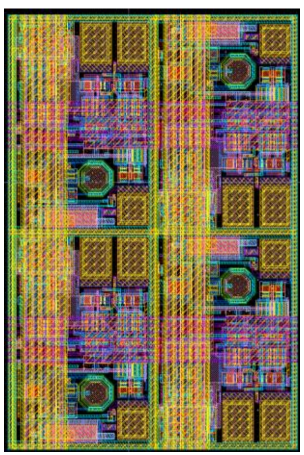
- **Version 1**
  - ✓ *More stable* ☺
  - ✓ *But including more components* ☹
- **Version 2**
  - ✓ *Less components included* ☺
  - ✓ *But less stable* ☹





Threshold voltage = *vRef2 – vRef1*

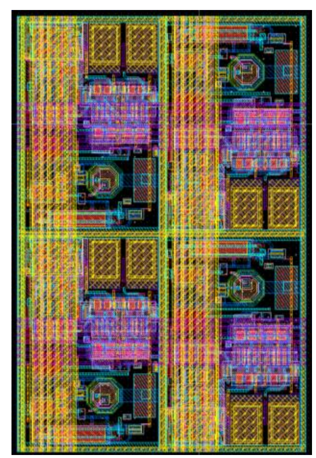
32×32 single row readout



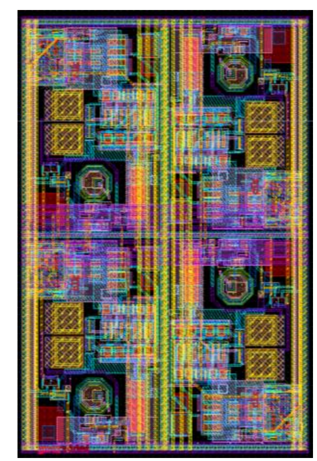
Cf. between AROM-0 and ULTIMATE

CHIP	Static bias current	Row processing time
AROM-0	*48µA@V1* *33µA@V2*	*100ns*
ULTIMATE	*~120µA*	*200ns*

32×32 single row readout

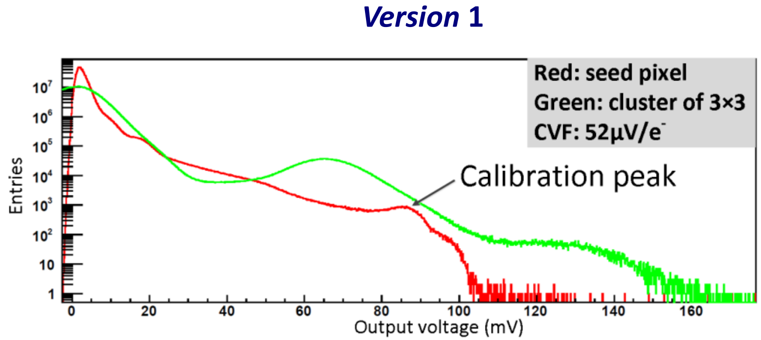


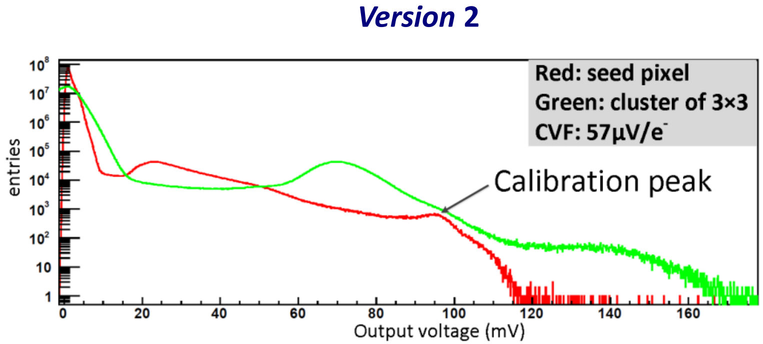
16×16 double row readout



Test Results of AROM-0

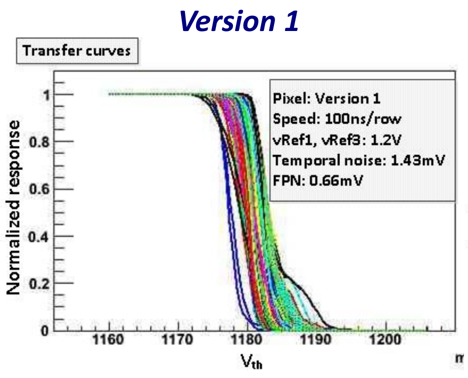
- ***Analogue calibration: Fe^{55} X-ray source***

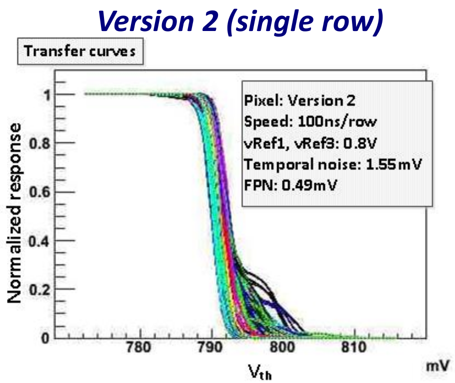




- *CVF: ~55μV/e⁻ => Correspond well to previous measurements with analog output pixels*

- ***Full in-pixel circuitry test***





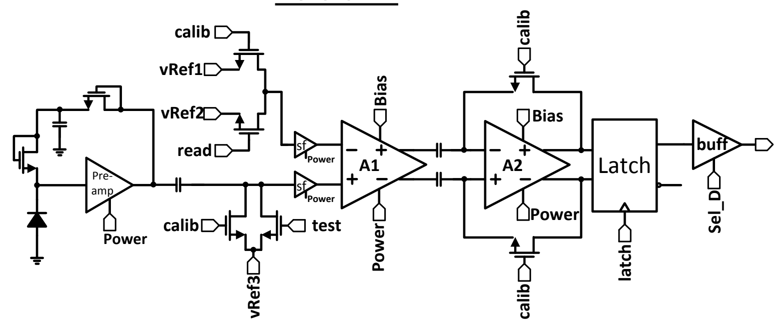
Sub-array	Temporal noise (mV)	FPN (mV)	ENC (e⁻)
V1	*1.43*	*0.66*	*30.2*
V2	*1.55*	*0.49*	*28.4*
V2 (double row)	*1.57*	*0.72*	*30,4*

- *Total ENC ~30e⁻ @ 100ns/row or 100ns/2rows*
- *The discriminator contributes ~ 20e⁻*
  - *Noise sources have been studied and noise performance can be improved*
- *Results are encouraging but further optimization is still needed => guiding the design of AROM-1*

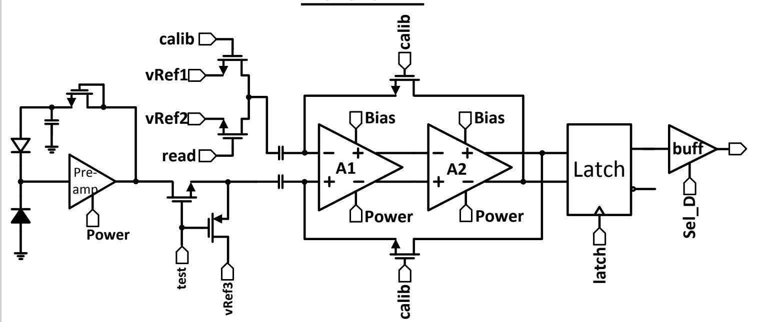
From AROM-0 to AROM-1

AROM-0 submission Feb. 2013

Version 1

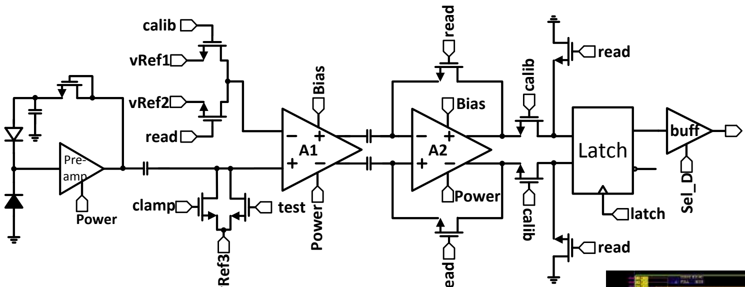


Version 2

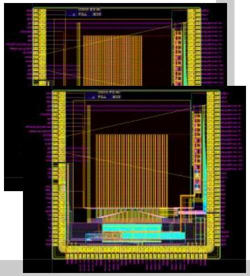


AROM-1 series

AROM-1 E/F submission Nov. 2013

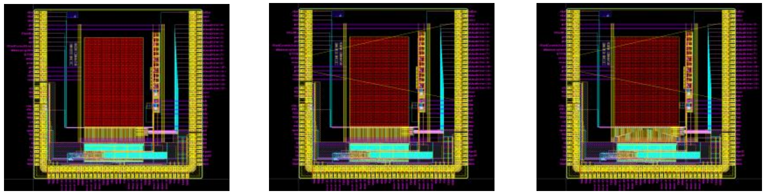


- 64 x64 pixels Double row readout
  - E: 22x33 µm²
  - F: 27x27 µm²
- Noise and power consumption optimized
- Expected to have the best performance



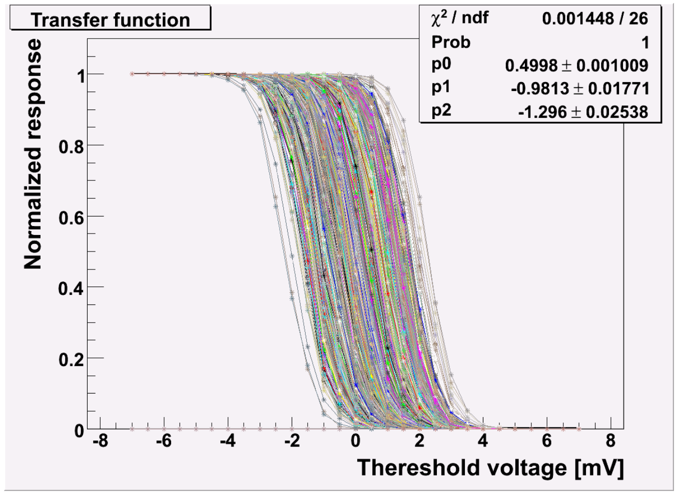
AROM-1 A/B/C submission Aug. 2013

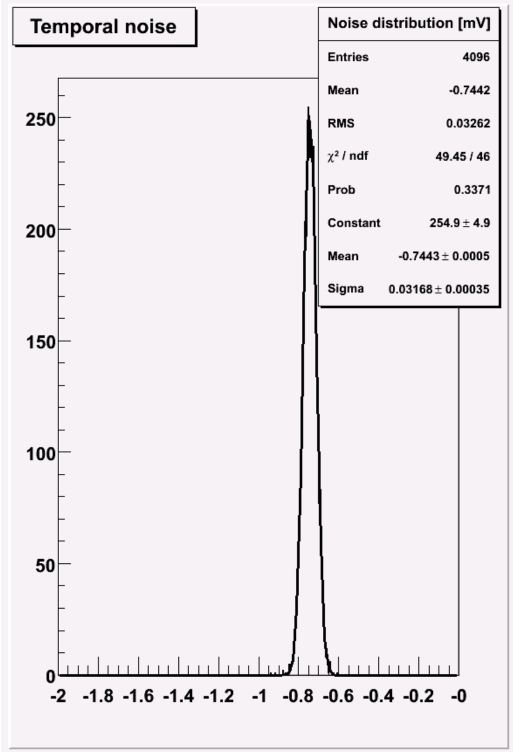
- 64 x64 pixels Double row readout
  - A: 22x33 µm² similar layout as AROM-0 V2
  - B: 22x33 µm² optimized layout => less cross talk
  - C: 24x33 µm² study impact of pixel pitch
- RTS noise mitigated by optimizing the pre-amplifier
- Thermal noise from switches optimized
- JTAG programmable reference and sequence control

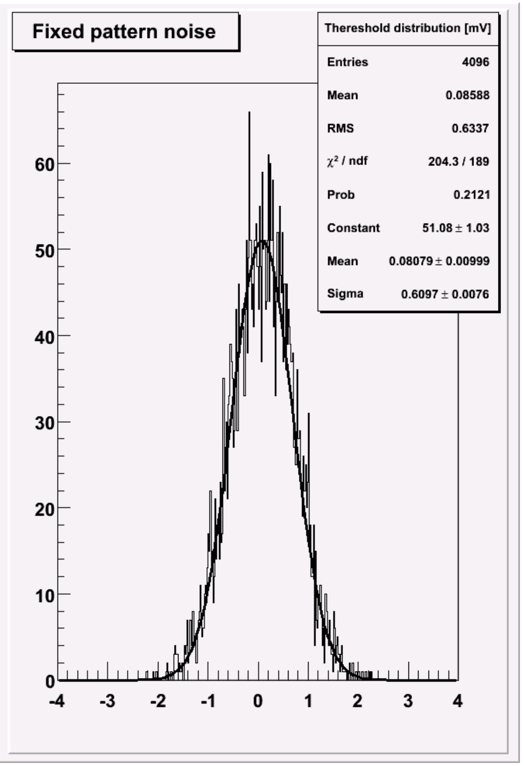


Test Results of AROM-1 B (1/2)

- ***In-pixel discriminator test***
  - *TN ~ 0,75mV, FPN ~ 0,63mV @ 100MHz clock (instead of 160MHz)*
    - *Readout speed: 160ns/2rows*
    - *Current acquisition board limitation*
  - *Noise improved by ~ 20% compared with AROM-0 V2 (double row readout)*
  - *Results are likely to allow for satisfactory signal-to-noise ratio (SNR)*
    - *It seems to be very difficult to further improve the noise performance in this circuit configuration*

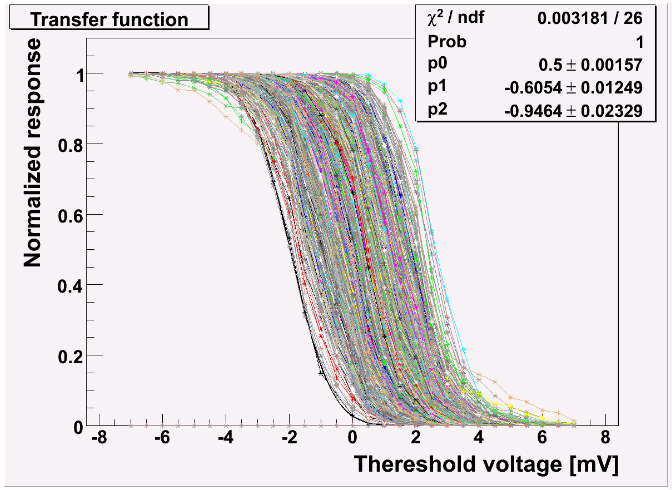


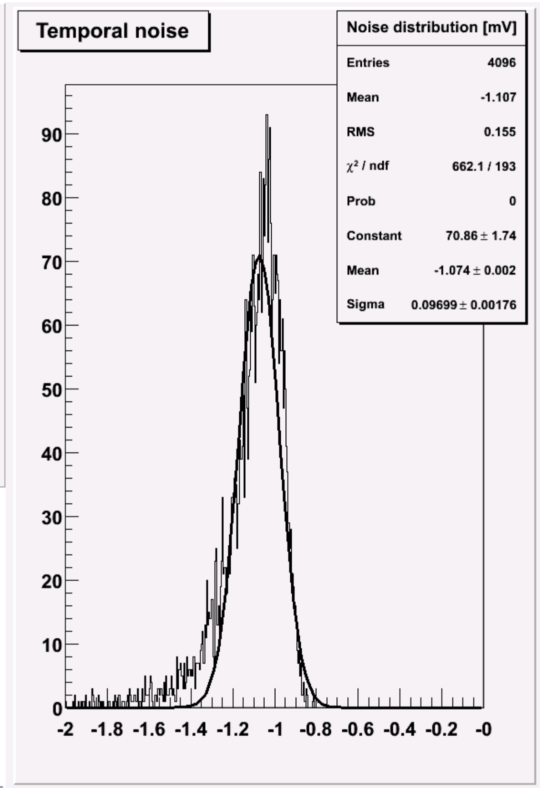


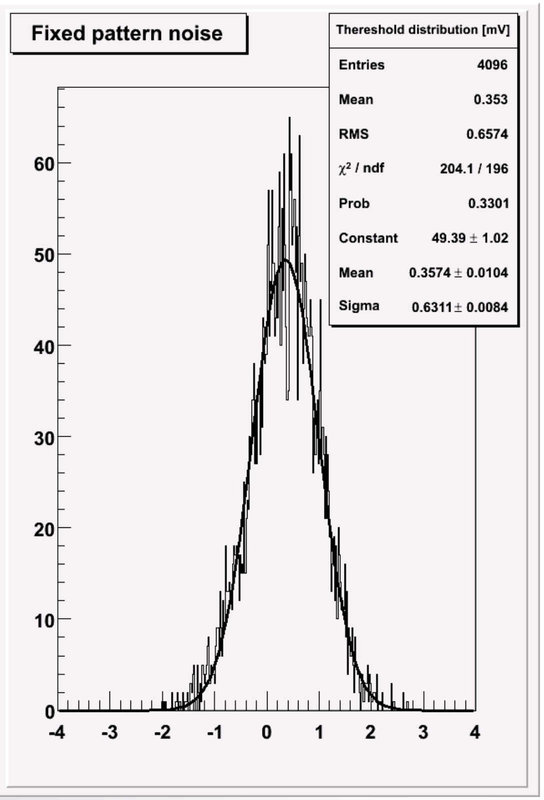


Test Results of AROM-1 B (2/2)

- ***Full in-pixel circuitry test results***
  - *TN ~ 1,1mV, FPN ~ 0,66mV @ 100MHz clock*
  - *Conversion factor before discriminator: 55µV/e⁻ ~ 70µV/e⁻*
  - *The discriminator still contributes larger noise than the sensing and pre-amplifying components*
    - *The dimension of the input transistor in the pre-amplifier is increased in AROM-1*
      => RTS noise mitigation BUT lower CVF
    - *It would be beneficial if a higher C-V conversion gain is achieved*

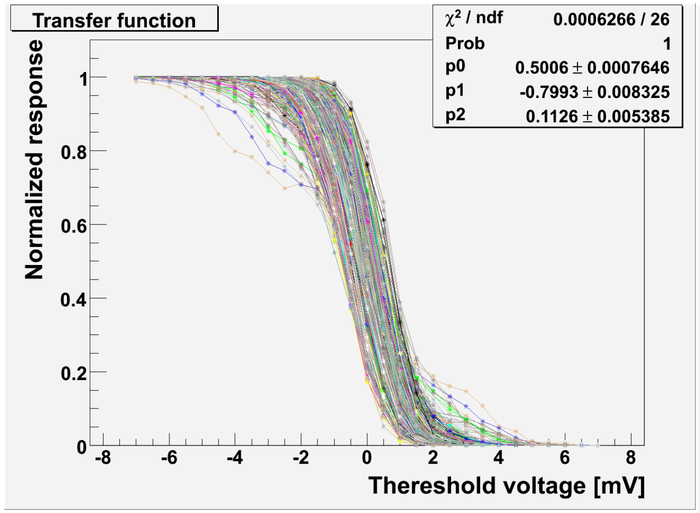


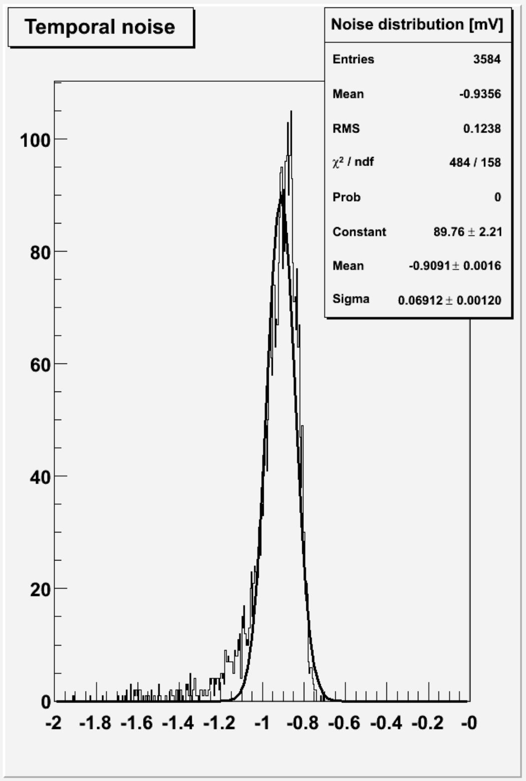


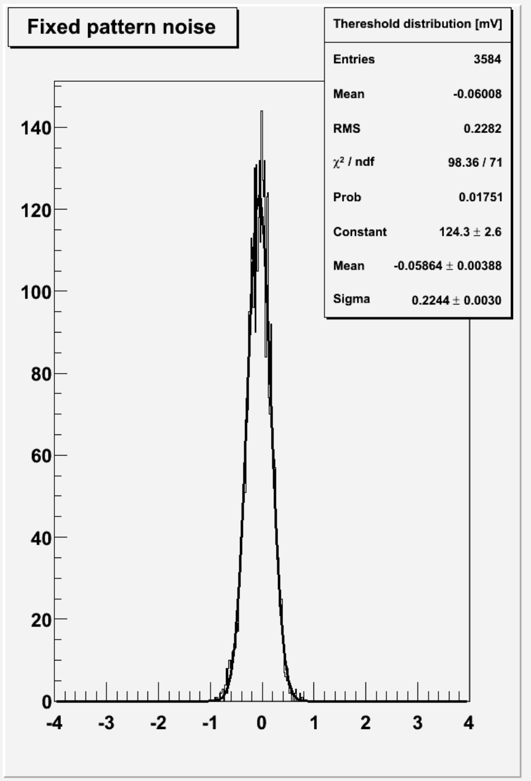


Test Results of AROM-1 E

- ***Full in-pixel circuitry test results (preliminary results, test still in progress)***
  - *TN ~ 0,94mV, FPN ~ 0,23mV @ 100MHz clock*
  - *Discriminator noise: TN ~ 0,29mV, FPN ~ 0,19mV @ 100MHz clock*
    - *TN and FPN largely decreased compared with AROM-1 B*
    - *very promising (also as expected)*
  - *The power consumption is also optimized => static current consumption ~ 15µA/pixel*
  - *Baseline pixel for FSBB_A development*

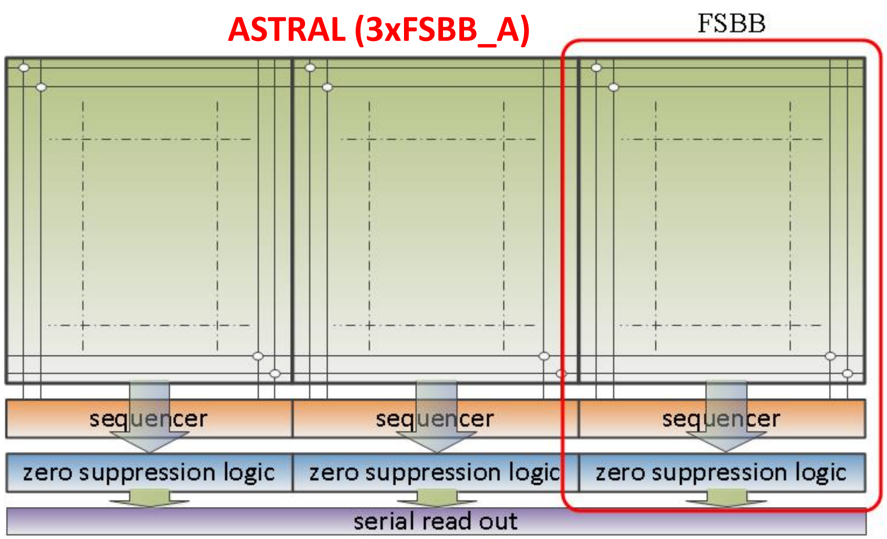






FSBB-A0 Overview

- ***Main characteristics***
  - *pixels of 22×33 µm² with staggered sensing diodes => AROM-1 E*
  - *Double-row rolling shutter readout*
  - *416 columns of 416 rows*
  - *13.7×9.2 mm² active area*
  - *New zero-suppression logic=> SUZE-02*
  - *4 output buffers of 512×32 bits each*
  - *2 output nodes at 320 Mbits/s (160 MHz clock)*
  - *Integrated JTAG, regulators, ...*
  - *$t_{r.o.}$ ~ 20 µs*



Summaries and Conclusions

- *The CMOS pixel sensor is under a transition of upgrading from the 0.35µm technology to the 0.18µm technology in order to meet the requirements of the ALICE-ITS upgrade*
  - *Radiation tolerance validated*
  - *New pixel architecture is explored => pixel level discrimination (fast & power efficient)*
- *AROM-0: feasibility study*
  - *Two different topologies of discriminator with promising performance*
  - *Some coupling issues found and high temporal noise => optimized in the AROM-1*
- *AROM-1: pixel optimization and upstream architecture verification*
  - *Including 5 different chip versions (AROM-1 A/B/C/E/F)*
  - *The best pixel is AROM-1 E derived from AROM-0 V1*
    - *Preliminary results have shown excellent noise performance*
    - *Power consumption also optimized => pixel static current consumption <15 µA*
- *FSBB_A0: verify the full chain and full functionalities of the ASTRAL sensor*
  - *Utilizing similar pixel as in AROM-1 E*
  - *To be tested this summer*
- *The final sensor called ASTRAL will combine 3 FSBB_As*

THANK YOU!