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Development of CMOS Pixel Sensor Featuring Pixel-Level Discrimination for the ALICE-ITS Upgrade

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The CMOS pixel sensor (CPS) based on the TowerJazz 180nm CIS process can provide qualified radiation hardness for the ALICE-ITS upgrade. Meanwhile, full CMOS integration in the pixel is achievable due to the availability of deep P-well. Therefore, a novel concept of pixel with integrated discriminator was realized to develop a fast and power efficient rolling shutter CPS architecture for the ALICE-ITS upgrade. Compared with the conventional CPS using column-level discrimination, the in-pixel discrimination sets the analog processing within the pixel. Thus the analog buffer driving the long distance column bus is no longer needed and the static current consumption per pixel can be largely reduced from 120 μ A down to 15 μ A. Besides, the row processing time can be halved down to 100ns thanks to small local parasitic. As a proof of concept, the prototype chip called AROM0 was fabricated in April 2013. Full functionality and the noise performance of the chip have been validated in laboratory test. Based on the experience of AROM0, the improved pixel designs have been implemented in the chip called AROM1 which is an intermediate prototype chip anticipating the final sensor architecture proposed for the ALICE-ITS upgrade. It features the pixel array of 64 \times 64 with double-row readout while integrating the on-chip biasing/reference control and JTAG programmable sequence management circuitry.

This paper will present the design and test results of AROM0. It'll also discuss the improvement in AROM1 and present the test results of this sensor which is expected in early 2014.

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