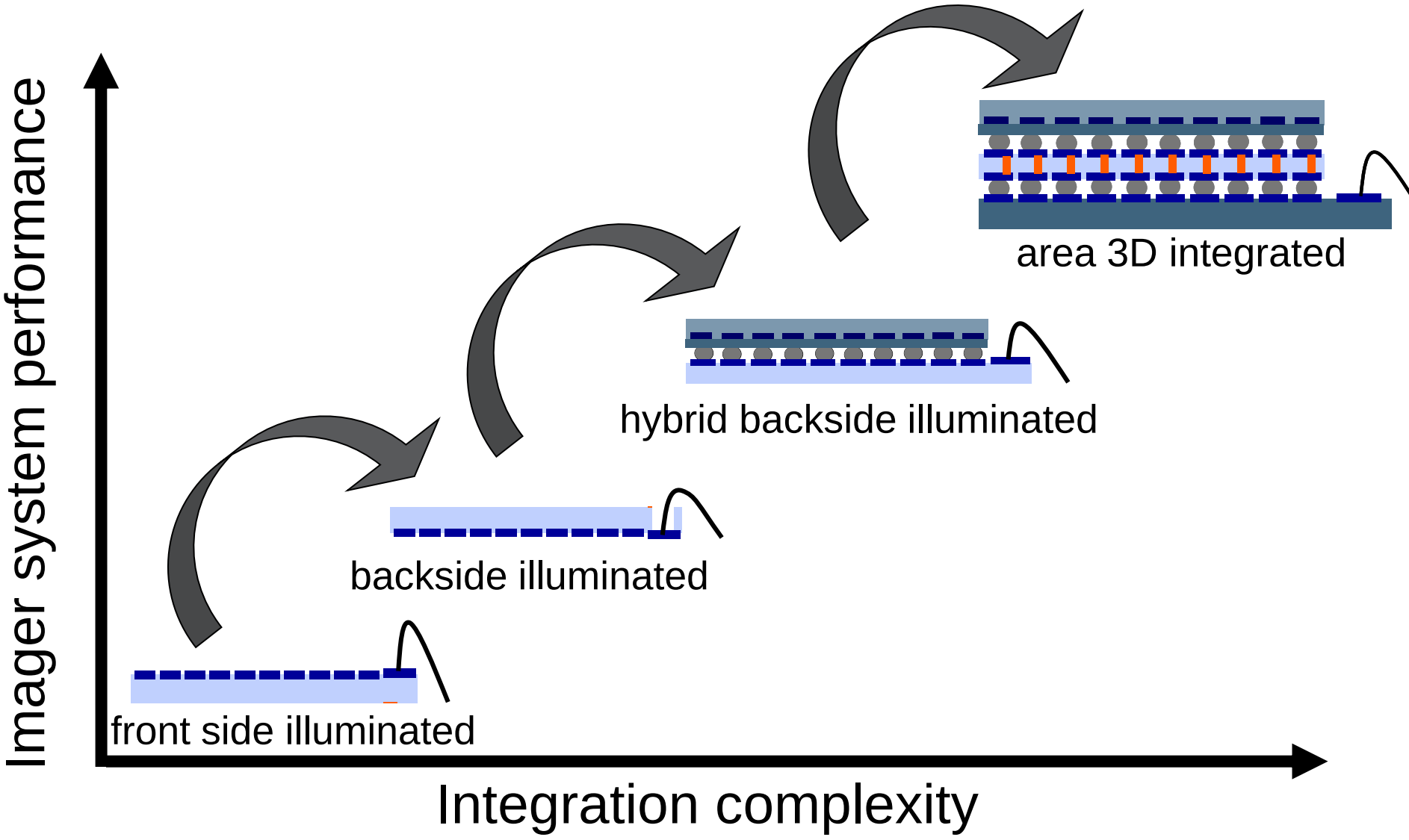
3D INTEGRATION OF IMAGERS

PIET DE MOOR

imec

IMEC'S IMAGER INTEGRATION ROADMAP



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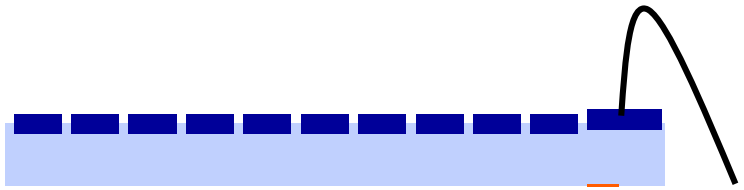
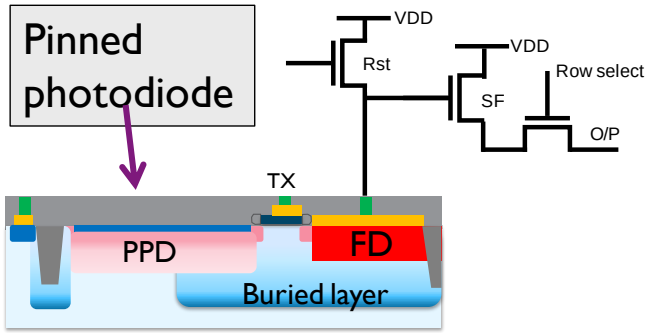
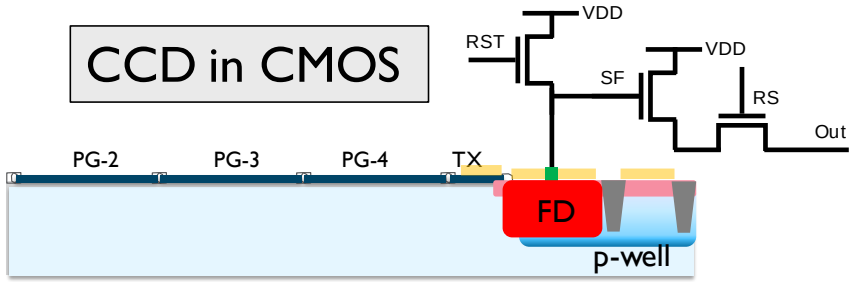
FRONTSIDE ILLUMINATED IMAGERS (FSI)



MONOLITHIC FRONT SIDE ILLUMINATED IMAGERS + EXTRA MODULES

- **Imec solution**: CMOS based imager technology:
  - 0.13 um CMOS platform
  - + CIS (CMOS imager sensor) module: 4T pixel
  - + high end add-on's and custom process development:
    - Backside illumination
    - Embedded CCD
    - Hyperspectral filters





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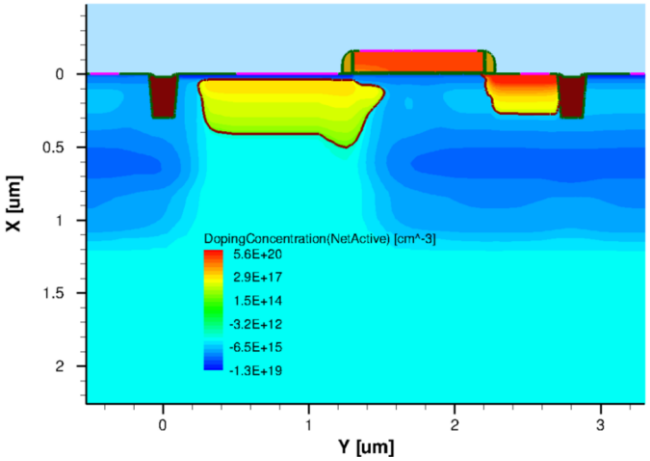
PIXEL DESIGN

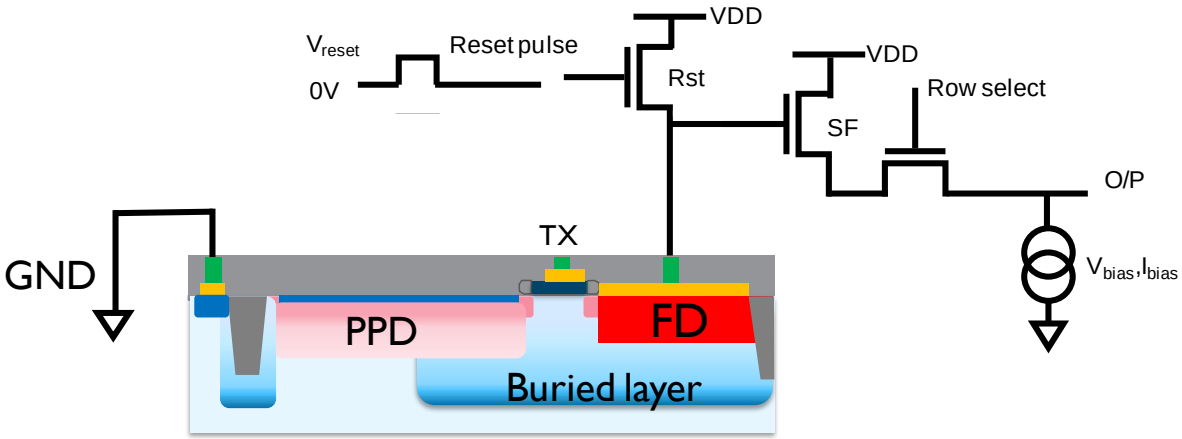
4 Transistor pixel with pinned photodiode:

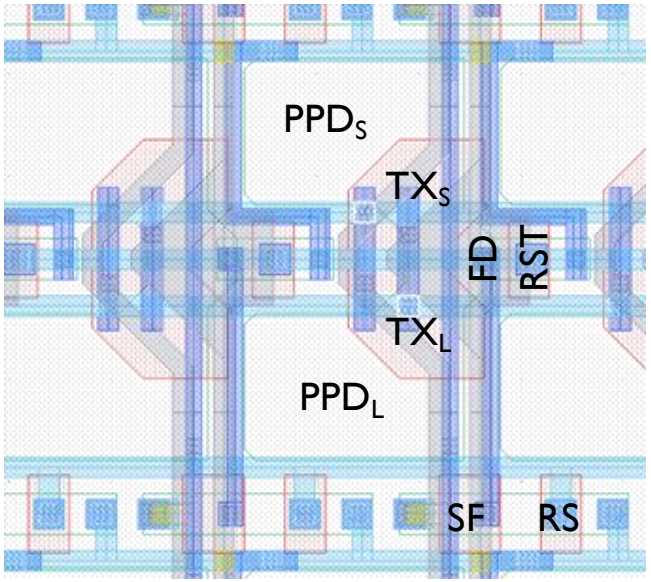
- ✓ low noise
- ✓ low dark current
- ✓ correlated double sampling compatible
- ✓ shared floating diffusion node

Key technology:

- ✓ custom design and process for:
  - photodiode
  - transfer gate
  - reset and source follower transistors







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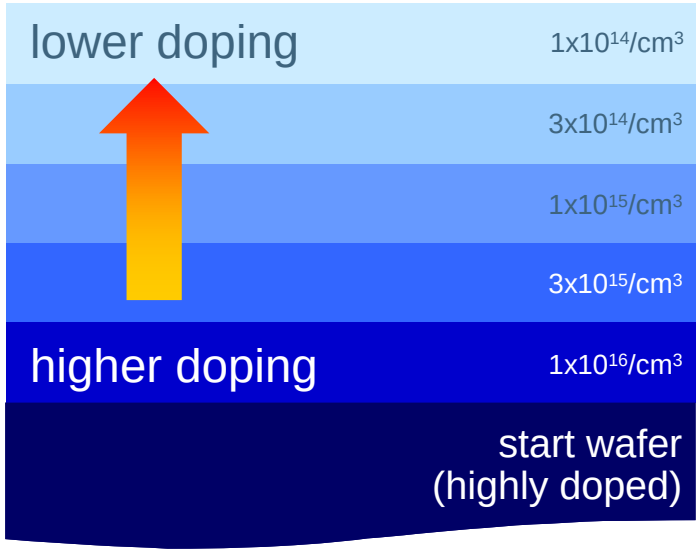
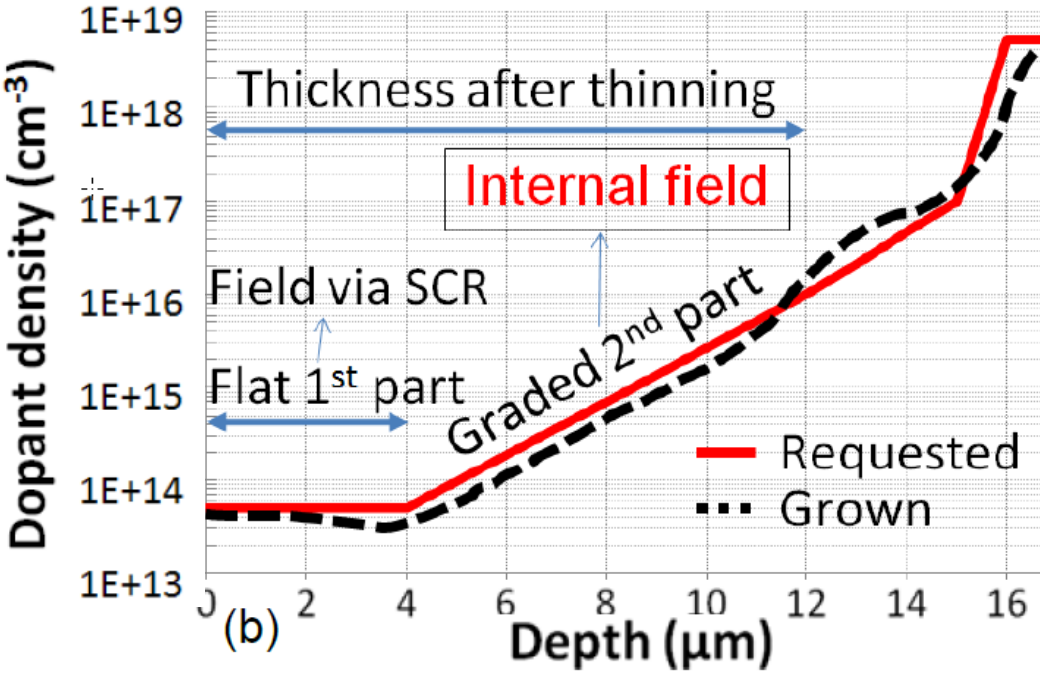
SPECIAL SUBSTRATES

- Epitaxial layers:
  - Thick:
    - Up to 50 um demonstrated
    - For enhanced red response
  - Graded dopant concentration
    - For directional carrier transport

    = lower cross-talk
- High resistivity substrates:
  - Both n and p-type
  - Resistivity > 1kOhm.cm
  - Solution for chucking in imec fab
- Application: fully depleted imagers for particles and X-ray (direct detection)





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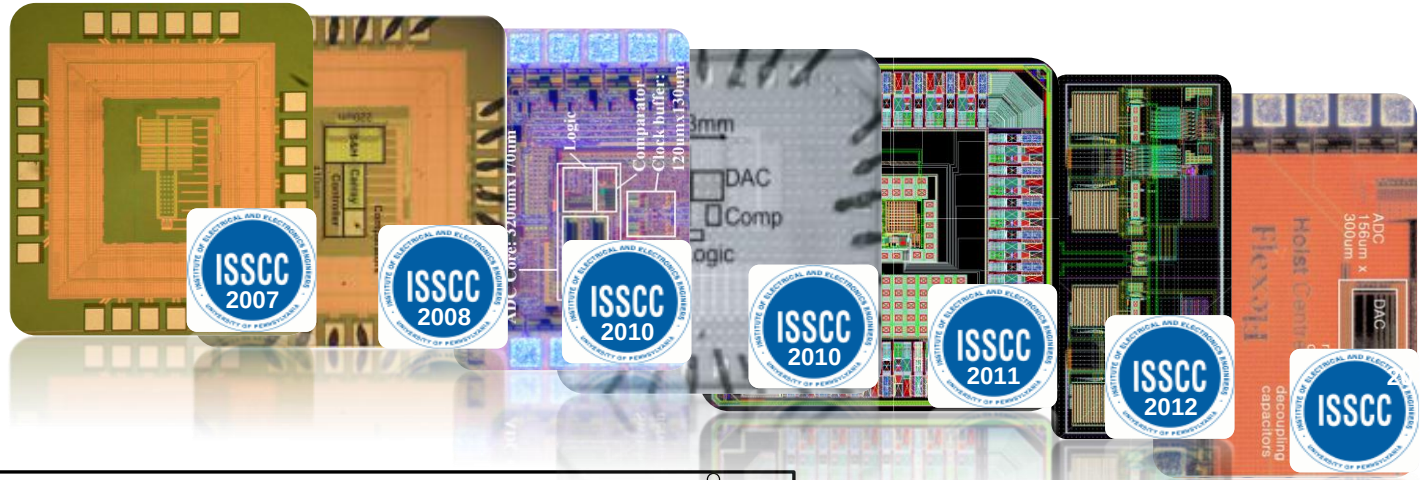
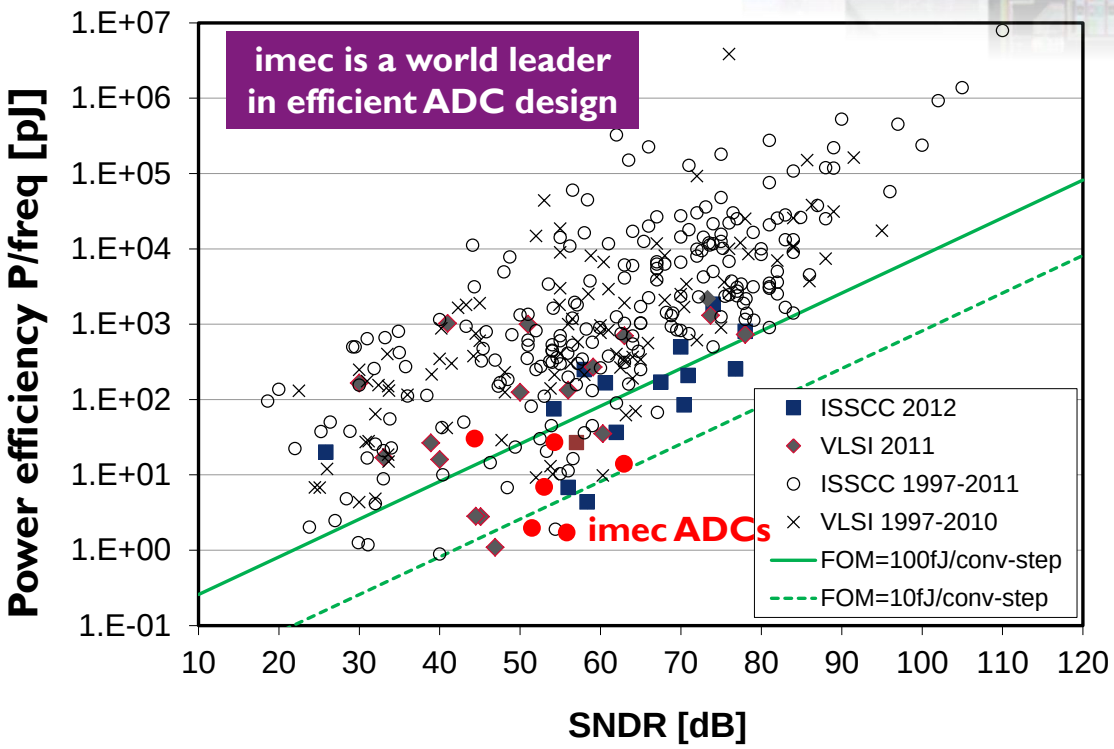
IMAGER SOC CIRCUIT DESIGN

8-12b
4-250MS/s
ADCs





- ADC typical specifications:
  - Low power consumption
  - High speed
  - Low noise/high resolution

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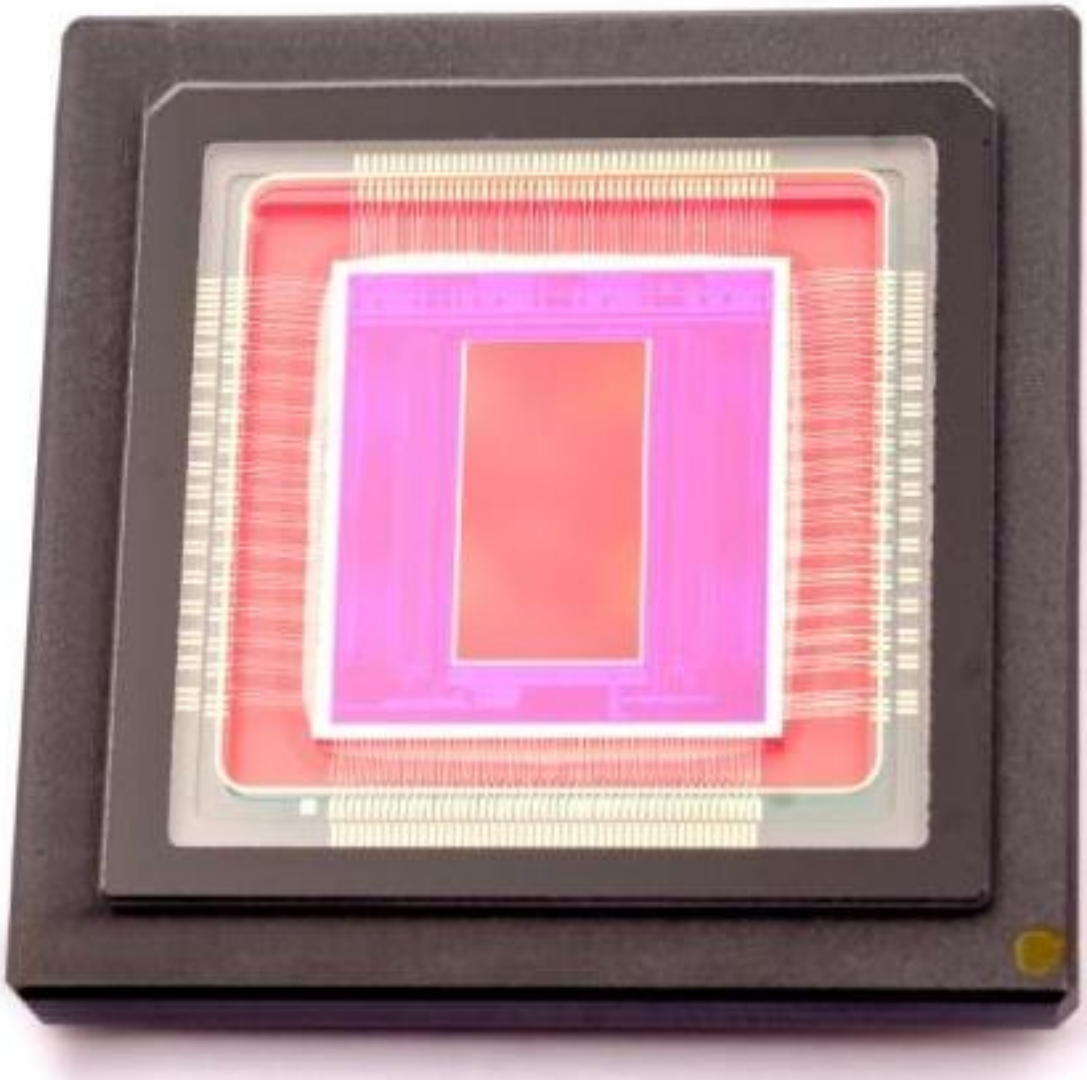
PROTOTYPE OF 4K X 2K CIS



- Imec 130nm CMOS
- 4kx2k pixels
- 2.5µm pitch
- 60fps
- 12bit ΔΣ column ADCs
- <1.5W
- LVDS digital interface

Designed & manufactured by imec for **Panasonic**

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RADIATION HARD DESIGN @ IMEC

- DARE: Radiation-hardened-by-design libraries in standard commercial CMOS technology:
  - Developed & enhanced in ESA projects
  - Library of mixed signal & digital design blocks:
    - DARE180 well supported (UMC 0.18 um CMOS)
    - XFAB .18 XH started
    - **Planned creation of a TSMC 65nm** DARE library

esa

Design Against Radiation Effects

EUROPRACTICE IC SERVICE

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IMEC ICLINK OFFERING

UMC

ON Semiconductor

EUROPRACTICE IC SERVICE

tsmc

TSMC

VCA Partner

Aerospace services

imecDARE

Backend
Design
Services

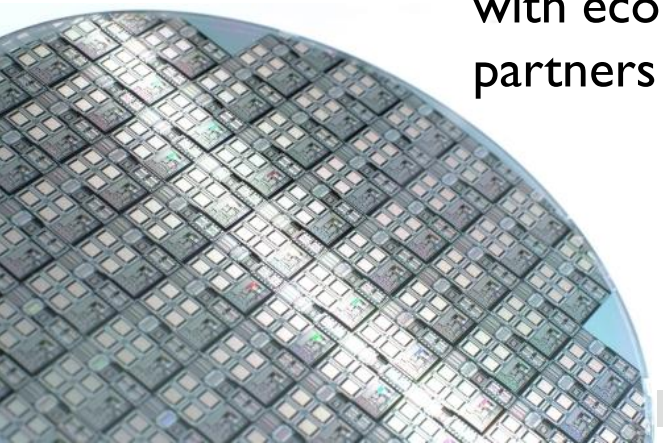
imec ICLink

PCB/PBA Services

EDM Electronics Design & Manufacturing

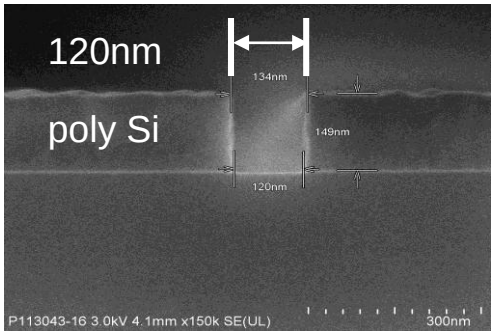
ASIC design with eco system partners

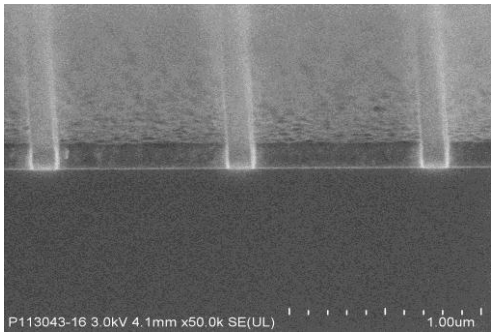
Technology
Targeting
Service

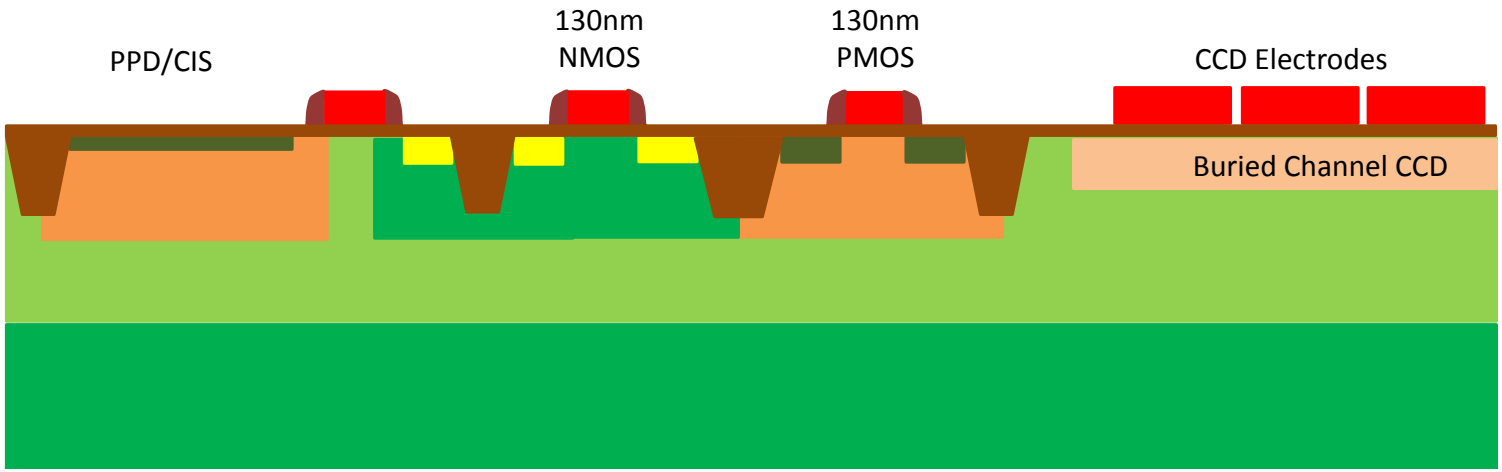


EMBEDDED CCD IN CMOS TECHNOLOGY

- Extra module added into Imec 130nm CMOS/CIS technology
- Narrow gap, single poly electrodes
- Customizable, BSI compatible CCD device
- Fully CMOS-CIS compatible







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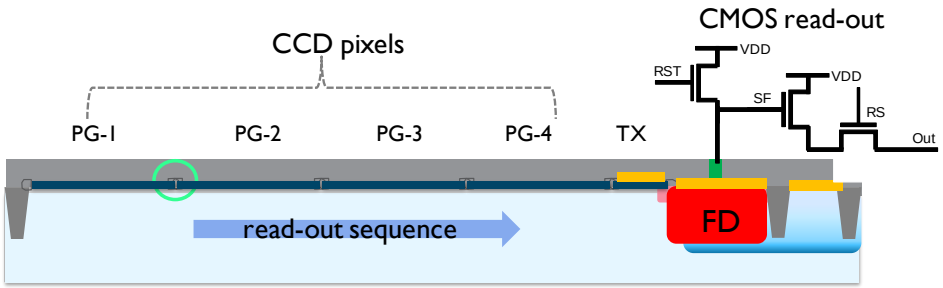
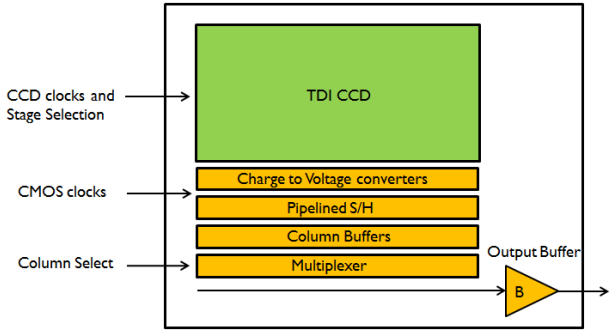
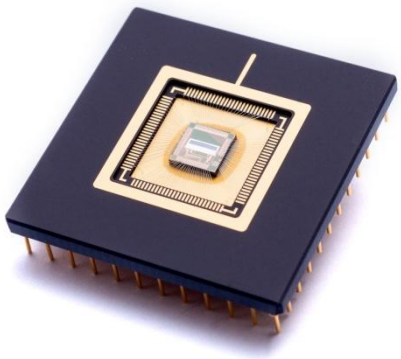
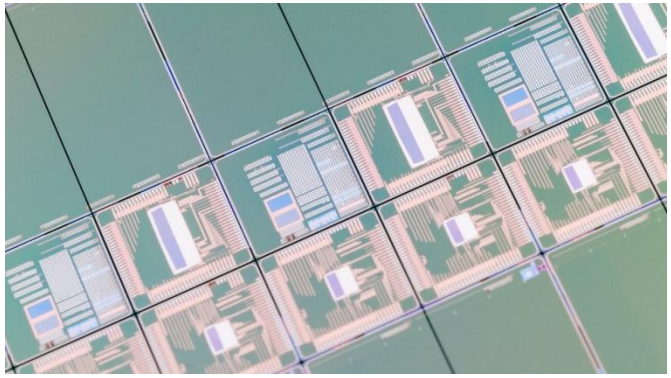
EMBBEDDED CCD TDI TEST IMAGER

- eCCD technology validated, devices processed
- excellent charge transfer efficiency (CTE) measured: > 99.9987 %









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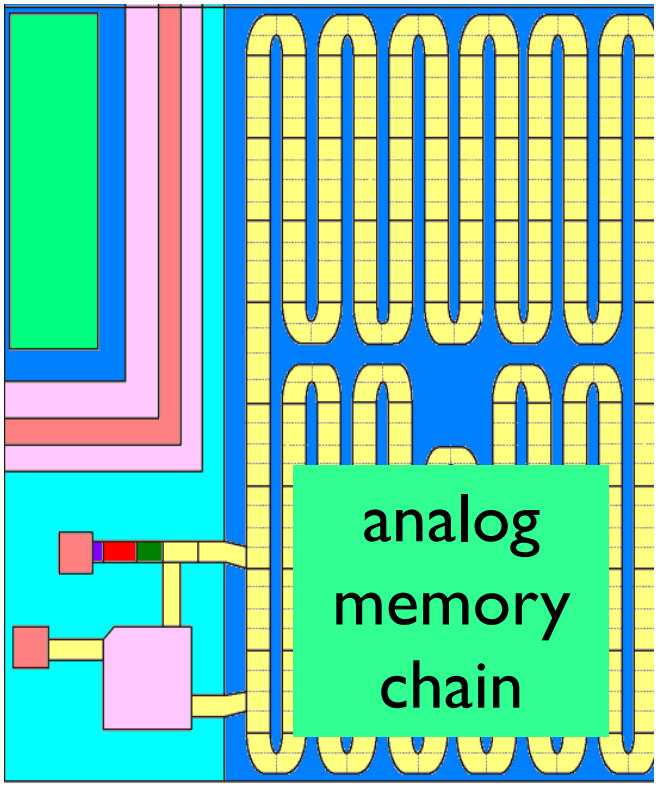
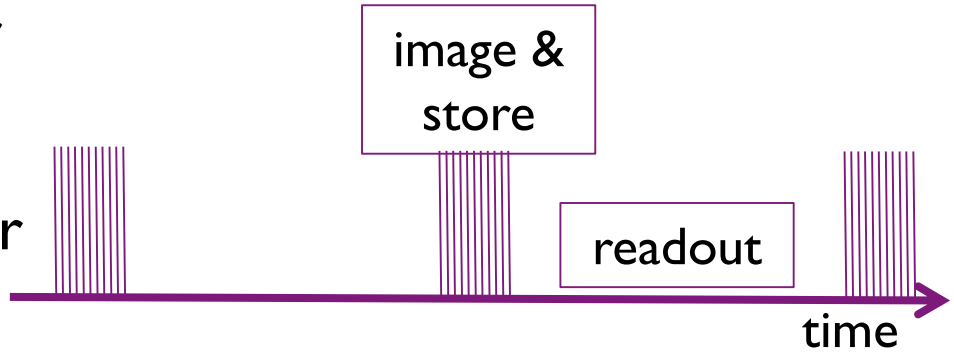
ULTRA FAST IMAGING USING ECCD

- design solution:
  - in pixel memories
  - = store a (limited) number of frames inside pixel
  - readout at lower speed
  - allows burst mode of imaging
- embedded CCD:
  - noiseless storage and transfer
- CMOS:
  - fast & low power data transfer off-chip, ADC's, ...



Source: G. Etoh



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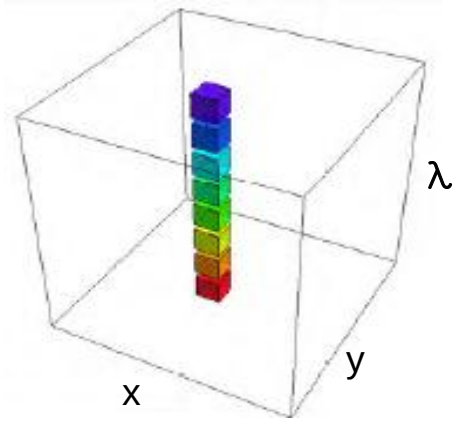
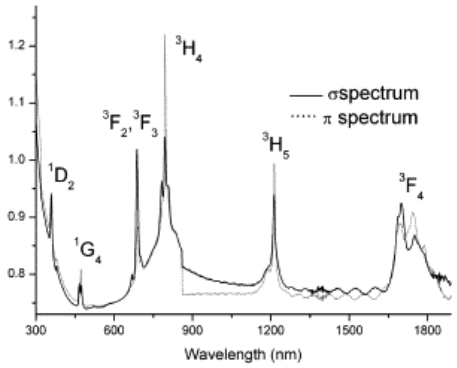
HYPERSPECTRAL IMAGING PRINCIPLE

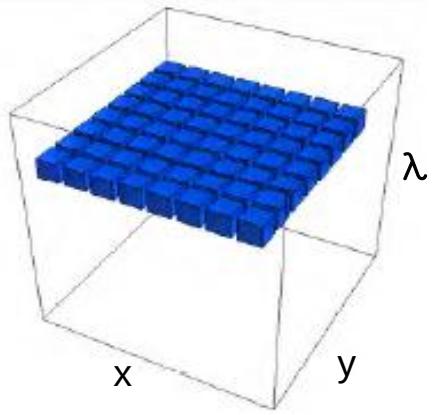
Spectrometer





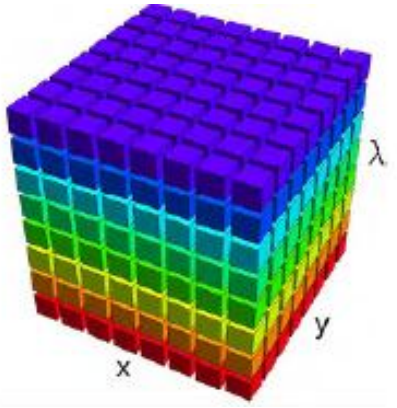
→ **Spectral information** in **one spatial pixel** only

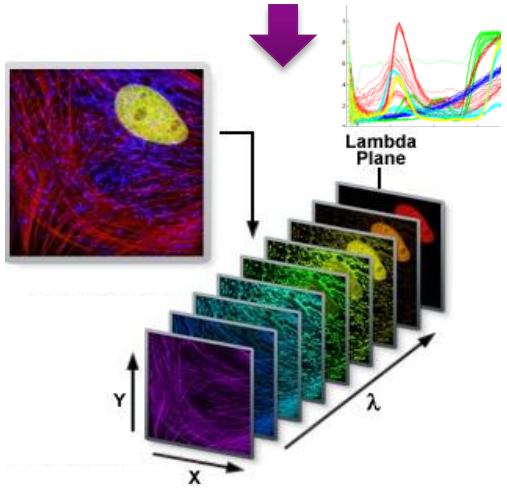
Color camera



→ **RGB colors** of **one image** only

Hyperspectral camera





→ Image-cube: both **spectral** and **2D information**

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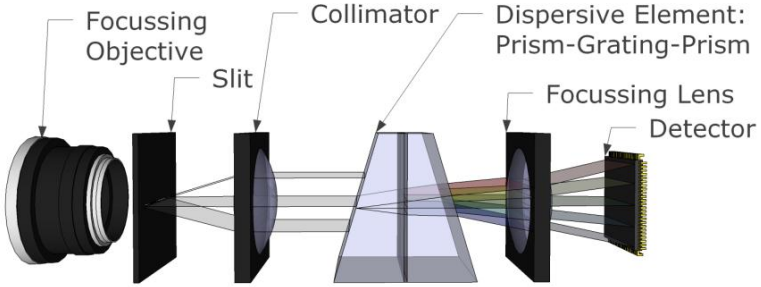
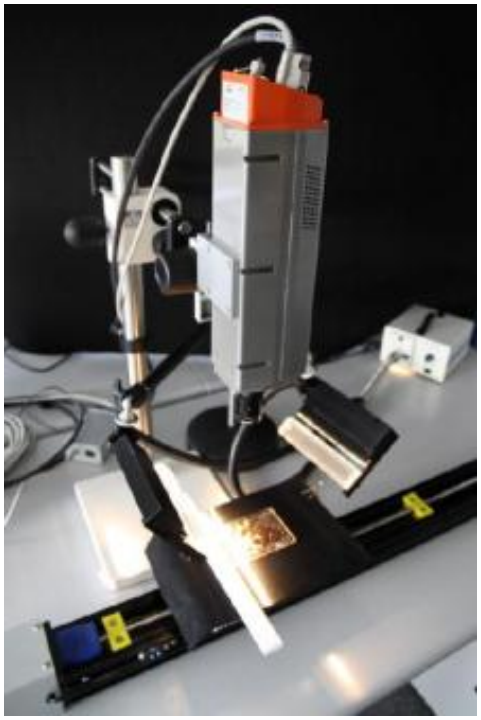
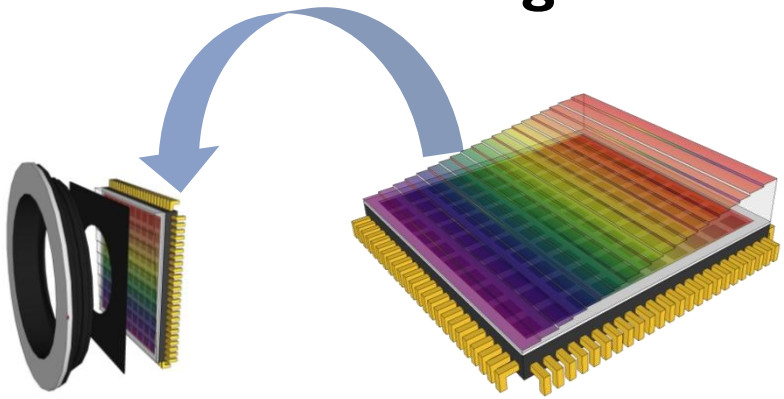
HYPERSPECTRAL IMAGERS: PRINCIPLE

- State-of-the-art:
  - Imager + grating/prism





- Imec solution:
  - **Wafer level filter integration**



Advantage:

- Extreme miniaturization

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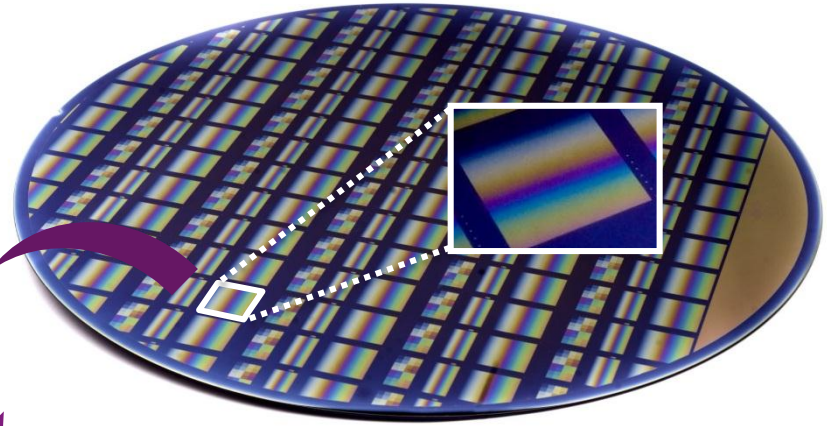
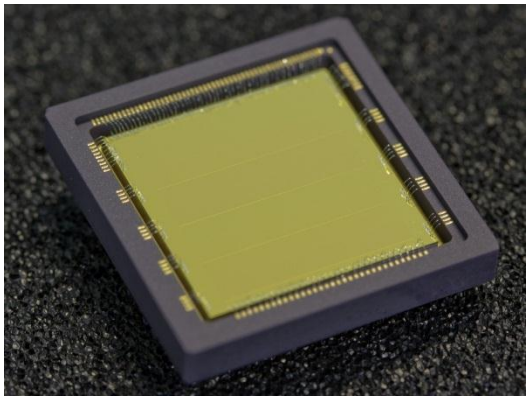
HYPERSPECTRAL IMAGERS: STATUS

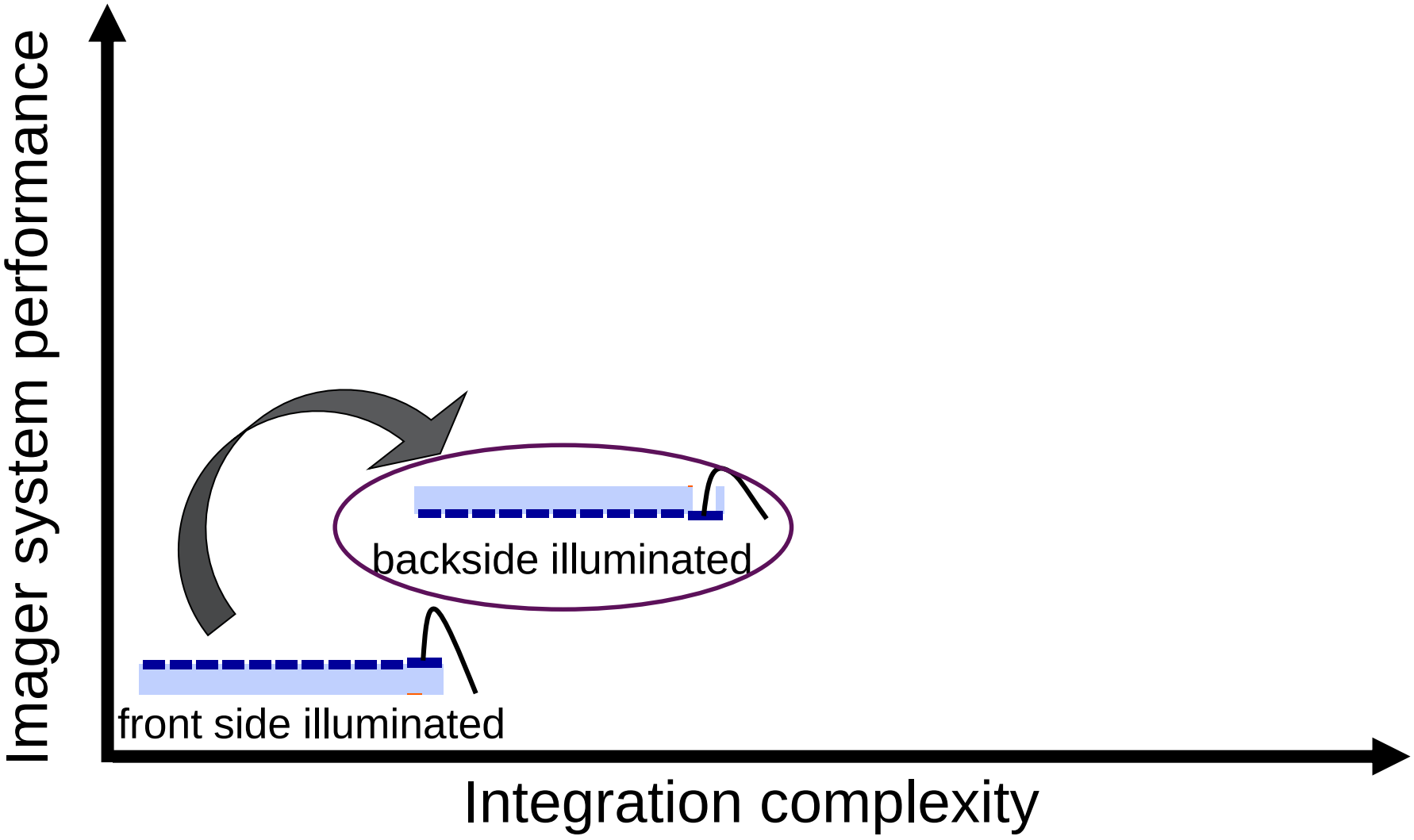
- technology established for 600 -900 nm
- technology development ongoing:
  - 470 – 900 nm
  - combination with panchromatic
- post-processed on top of CMOSIS's CMV2000 & CMV4000 sensors
- 6 different camera implementations
- evaluation kits available





BACKSIDE ILLUMINATED IMAGERS (BSI)

ADVANCED IMAGER INTEGRATION



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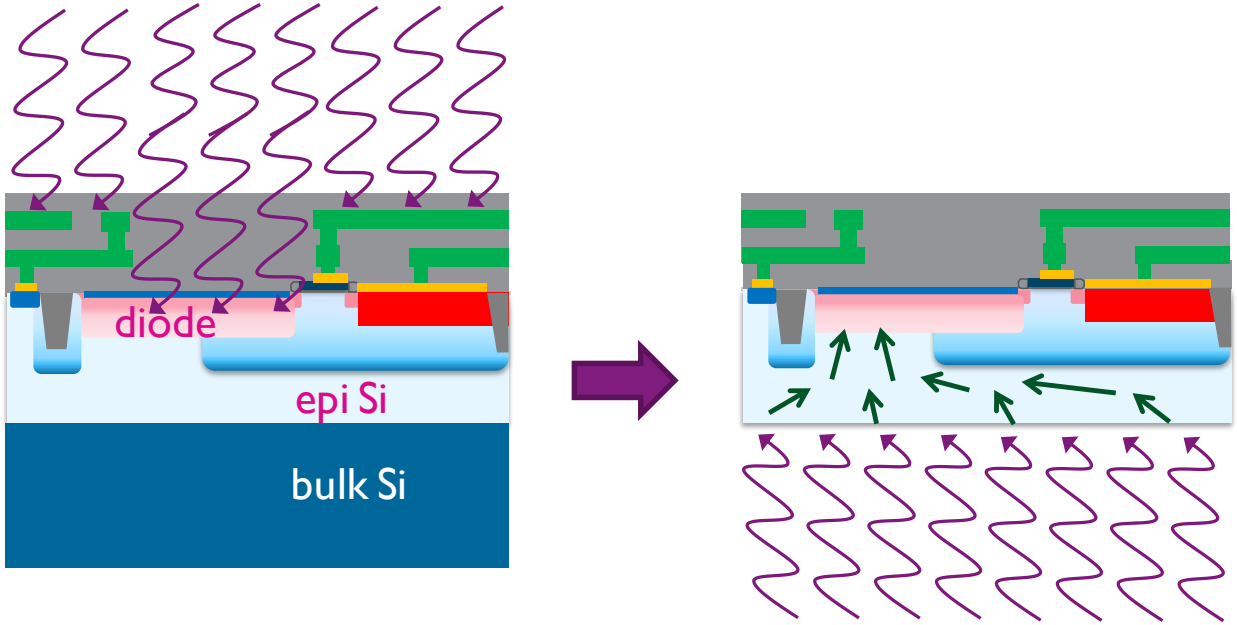
BACKSIDE VS. FRONTSIDE ILLUMINATION

- **Front side illumination:**
  - Absorption in BEOL dielectrics
- **Backside illumination :**
  - Direct absorption in Si



Front side illuminated

Backside illuminated

- imec provides backside illuminated imager platform including **very shallow surface passivation**

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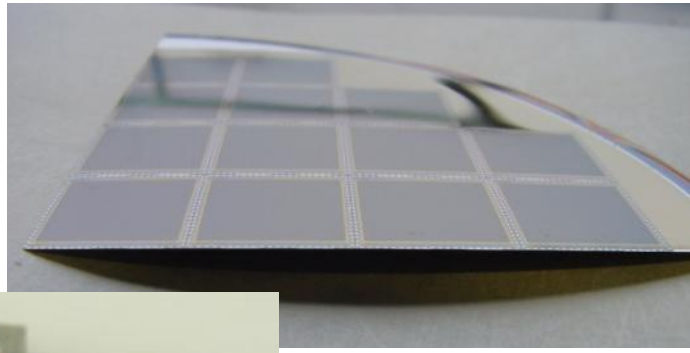
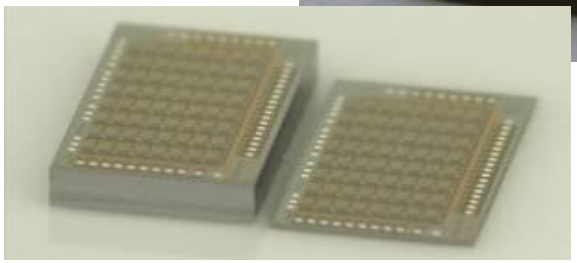
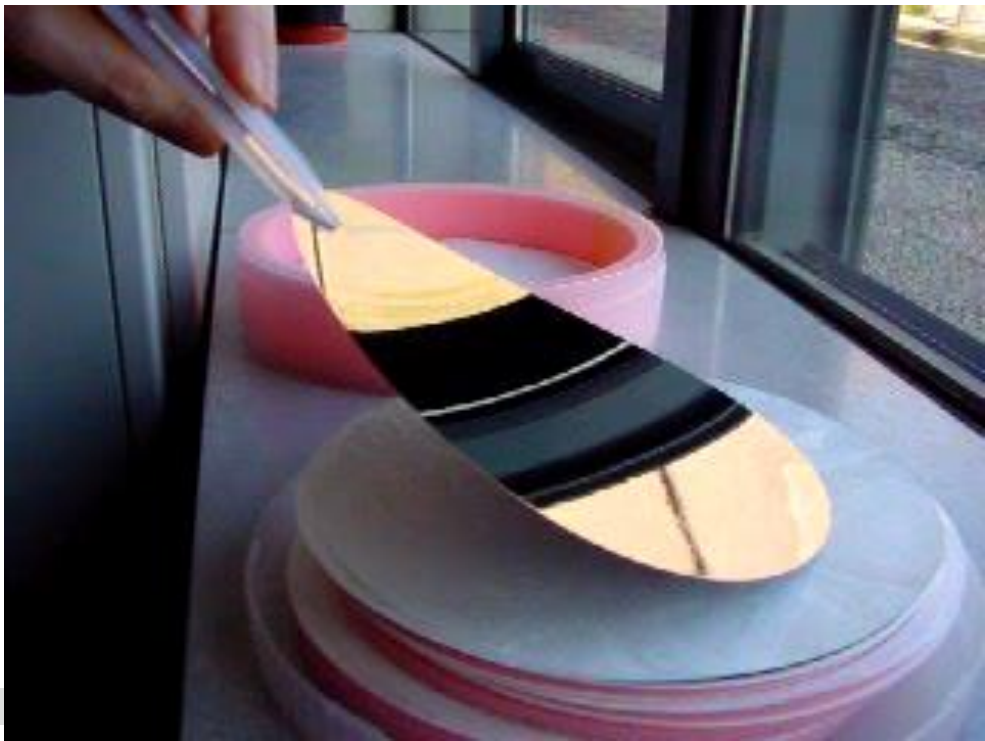
TECHNOLOGY ENABLER: THINNING

- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers wafer bonding technology
- IMEC results:
  - Thinning down to a few um
  - Total thickness variation < 1 um on 200 mm wafer







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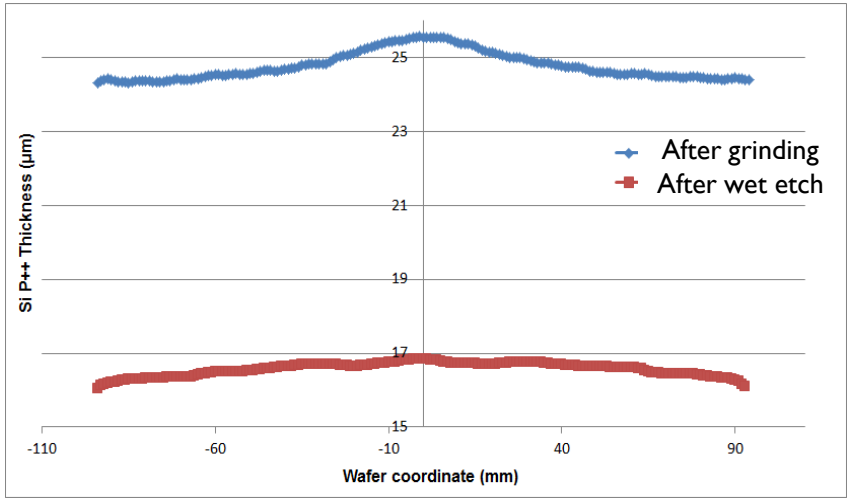
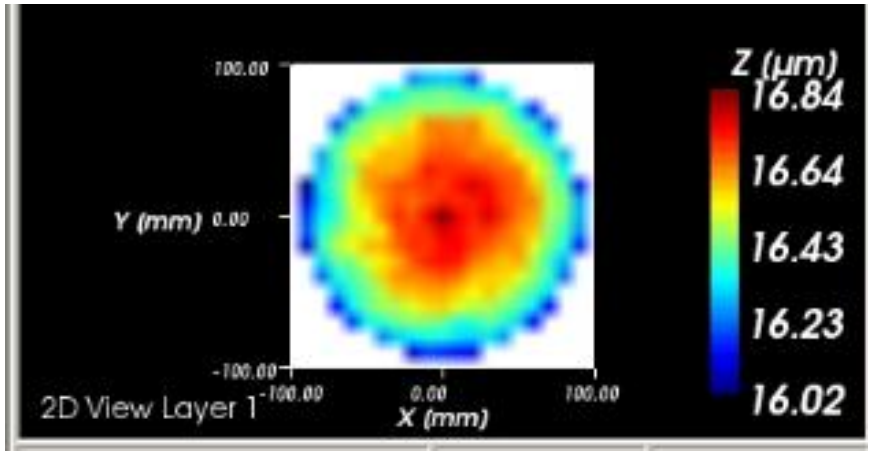
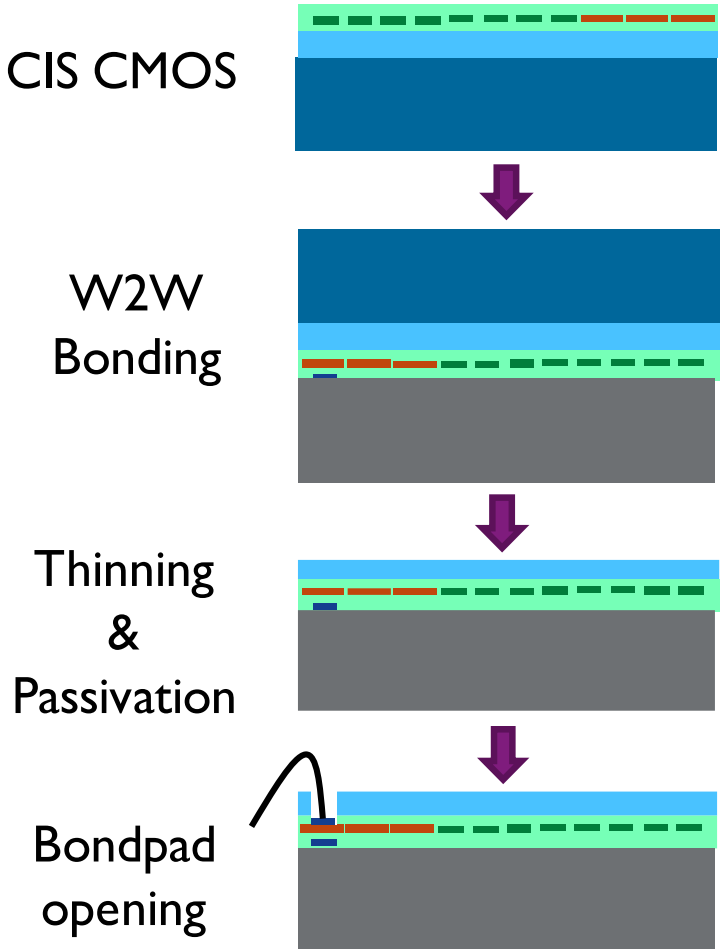
THINNING PROCESS

- Progressive **bulk** thinning approach:
  - Grinding + Selective and Non-selective wet etch final thickness with < 1um TTV (on 200 mm wafer)
- important parameters:
  - Final thickness: determines the QE in the (infra)red
  - Thickness uniformity: total thickness variation (TTV)

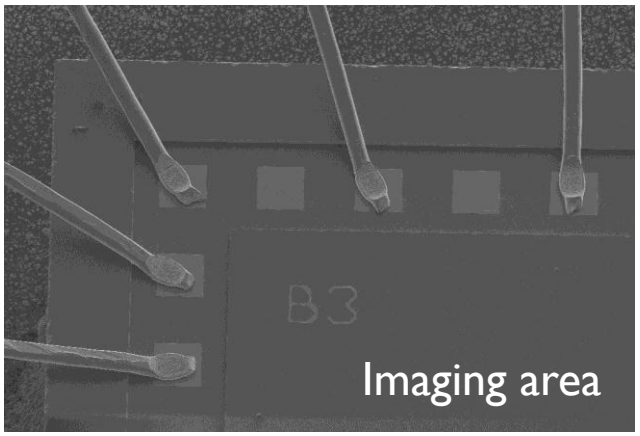




IMEC BACKSIDE ILLUMINATION MODULE



- Extension of 0.13 micron CMOS/CIS process
- Process module including:
  - Wafer-to-wafer bonding
  - (bulk) Wafer thinning
  - Backside passivation
  - Anti-reflection coating
  - Bondpad opening



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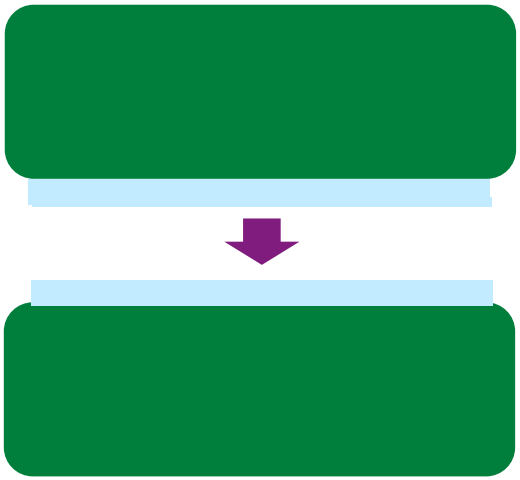
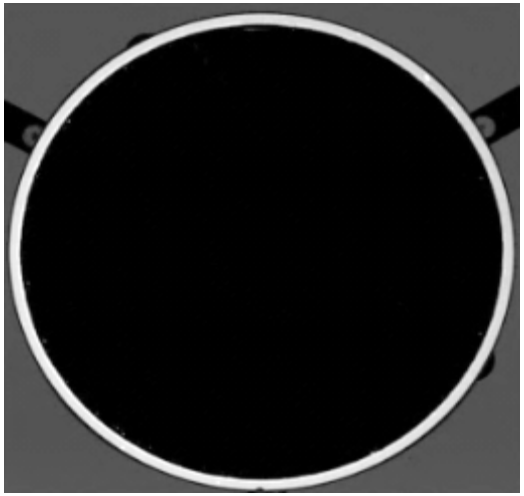
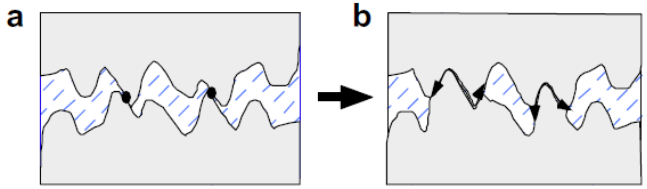
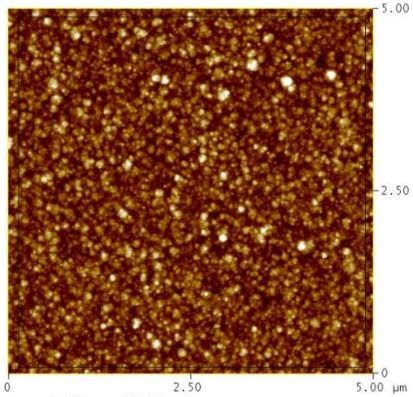
DIRECT LOW TEMPERATURE OXIDE-OXIDE BONDING

- successful optimization of process
- important parameters:
  - topology
  - flatness
  - micro-roughness
  - surface particles
  - controlled surface chemistry









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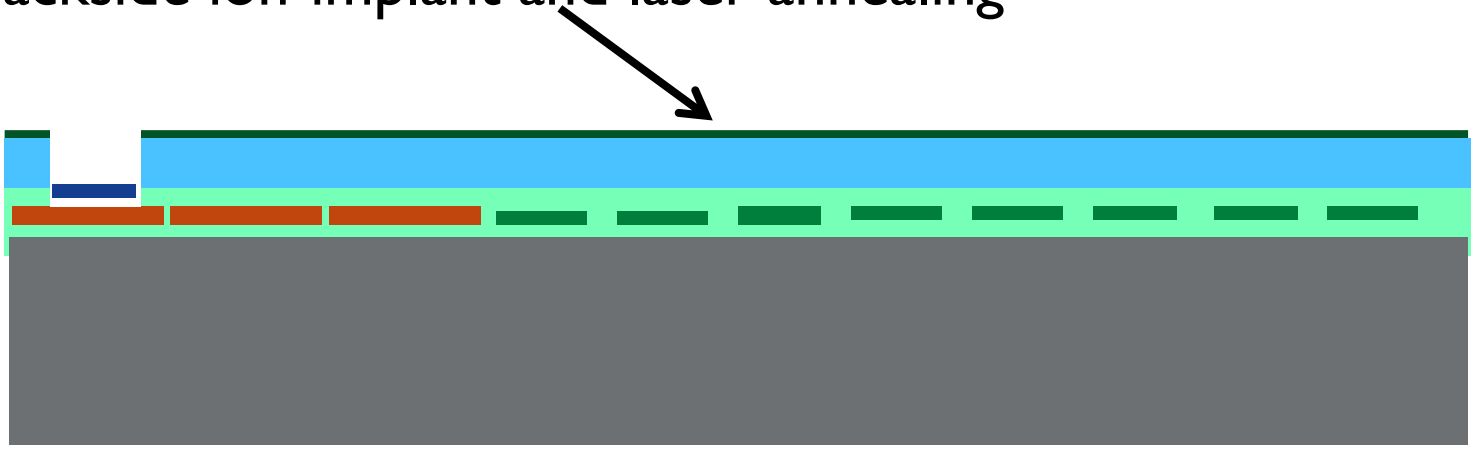
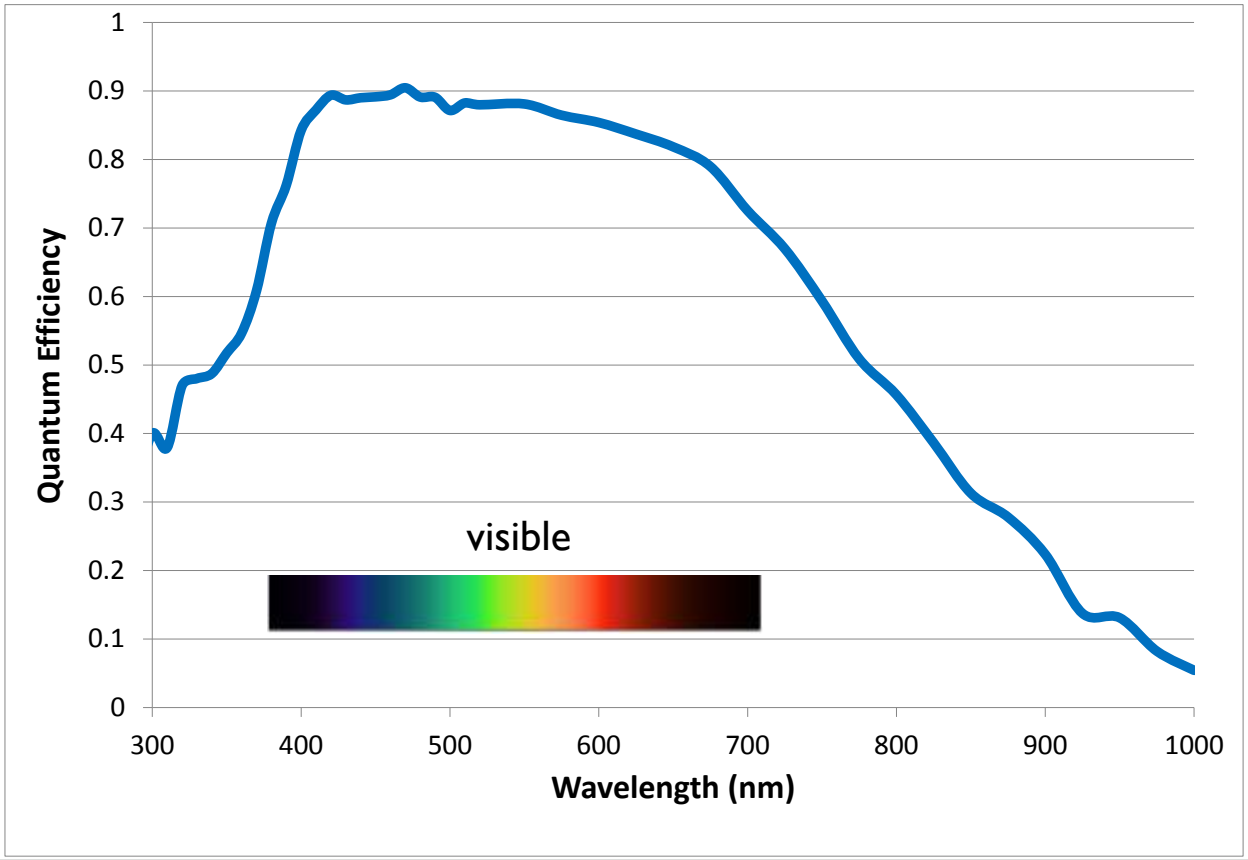
BACKSIDE SURFACE PASSIVATION: PROBLEM AND SOLUTION

- Problem:
  - Backside interface is low quality: high trap density, potential pockets
  - Impact on imager performance:
    - Reduced quantum efficiency (esp. blue/green)
    - Increased dark current
- Solution: backside surface field:
  - Backside ion-implant and laser annealing



BACKSIDE ILLUMINATION RESULTS: VISIBLE

- including ARC
- QE_{max} ~ 90 %, QE > 70% in visible



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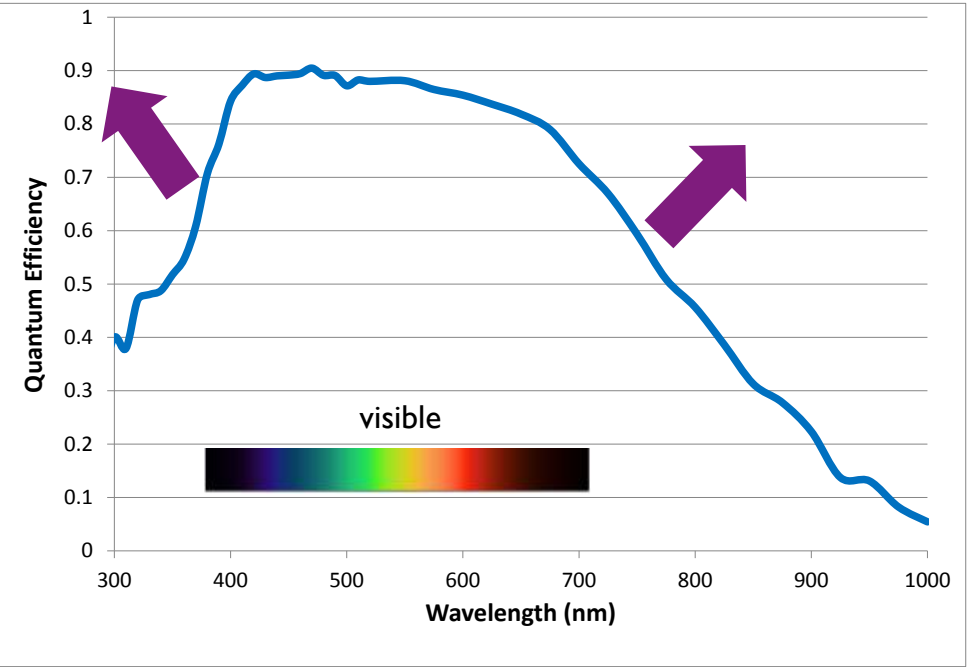
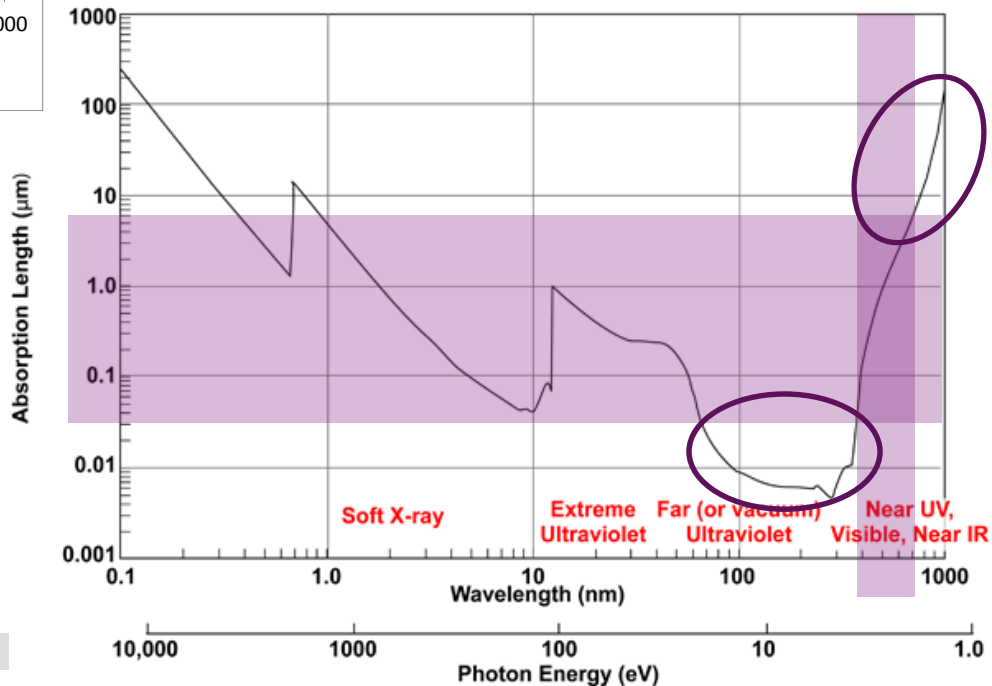
BACKSIDE ILLUMINATED IMAGERS: WAVELENGTH EXTENSION



- near infrared (and soft X-ray):
  - deep absorption of photons → thicker epi material

- ultraviolet:
  - very shallow absorption of photons → very thin backside passivation



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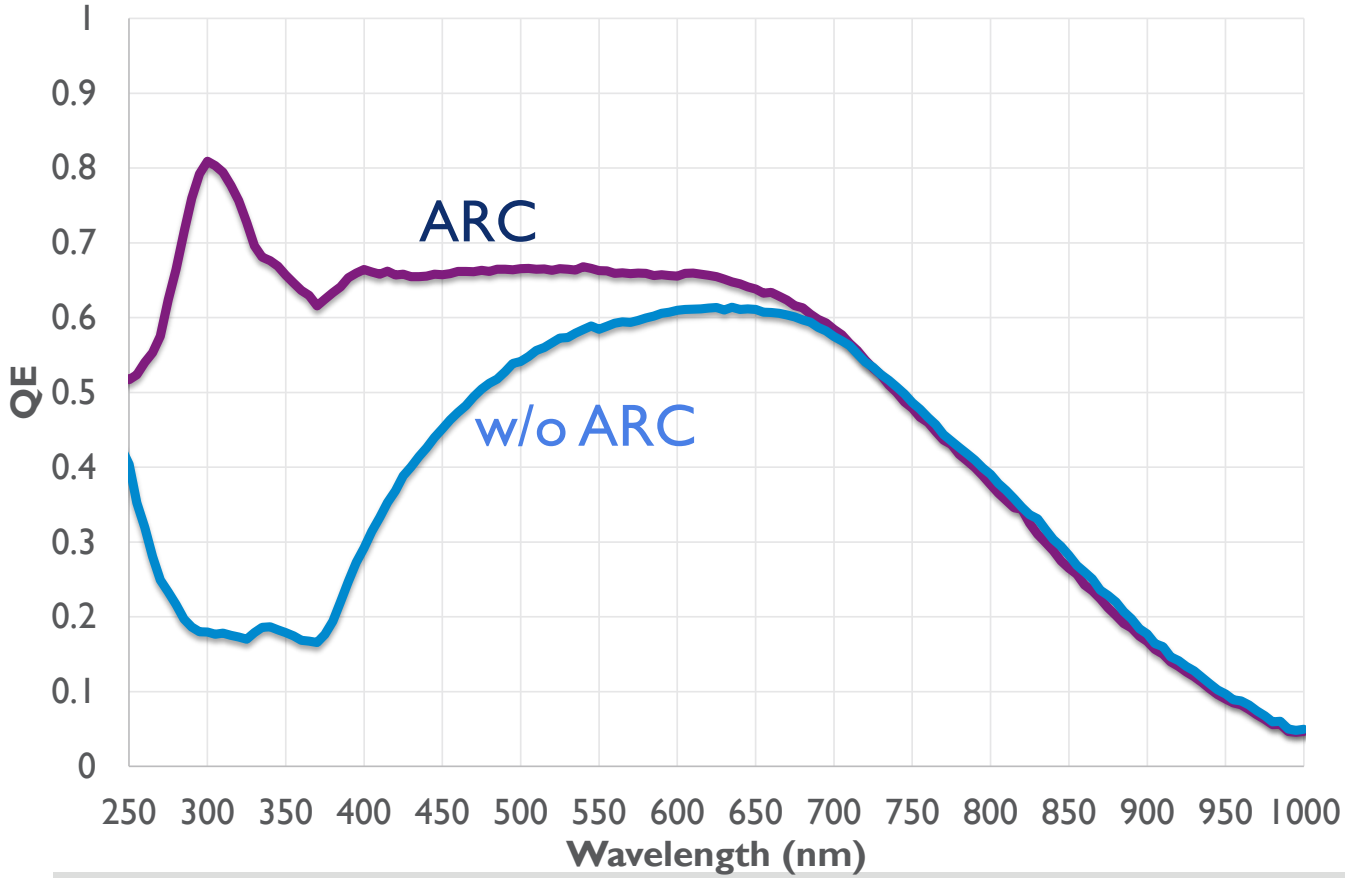
BACKSIDE ILLUMINATION RESULTS: NEAR ULTRAVIOLET

- optimized backside passivation and ARC
- QE > 60% from 270 nm - 700 nm



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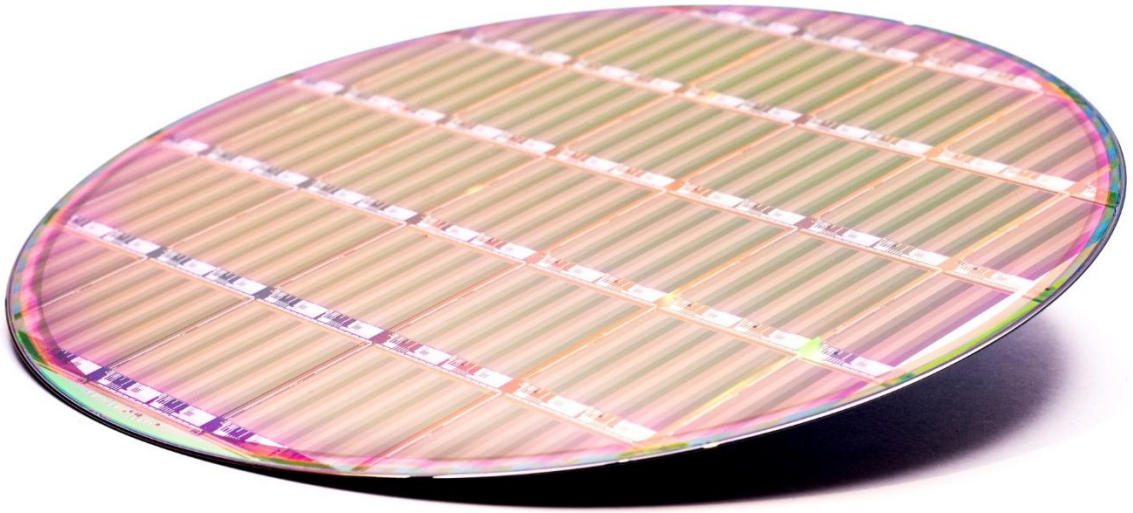
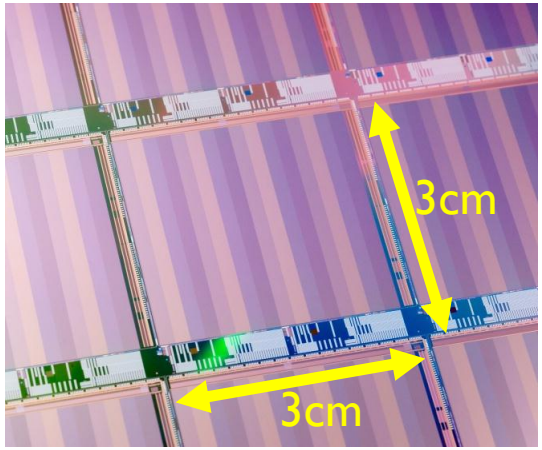
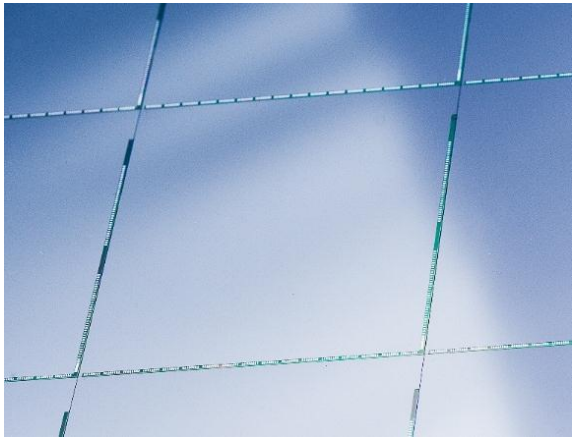
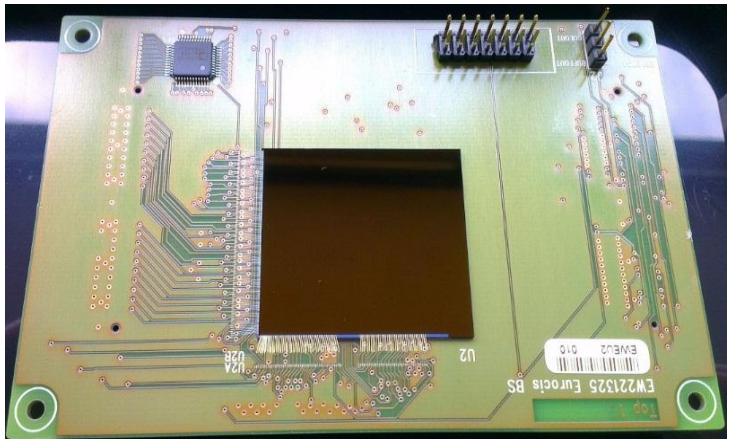
EUROCIS: large area imager for space



- 2k x 2k, 14 um pixels stitched imager
- 8 different flavors of rad hard pixels







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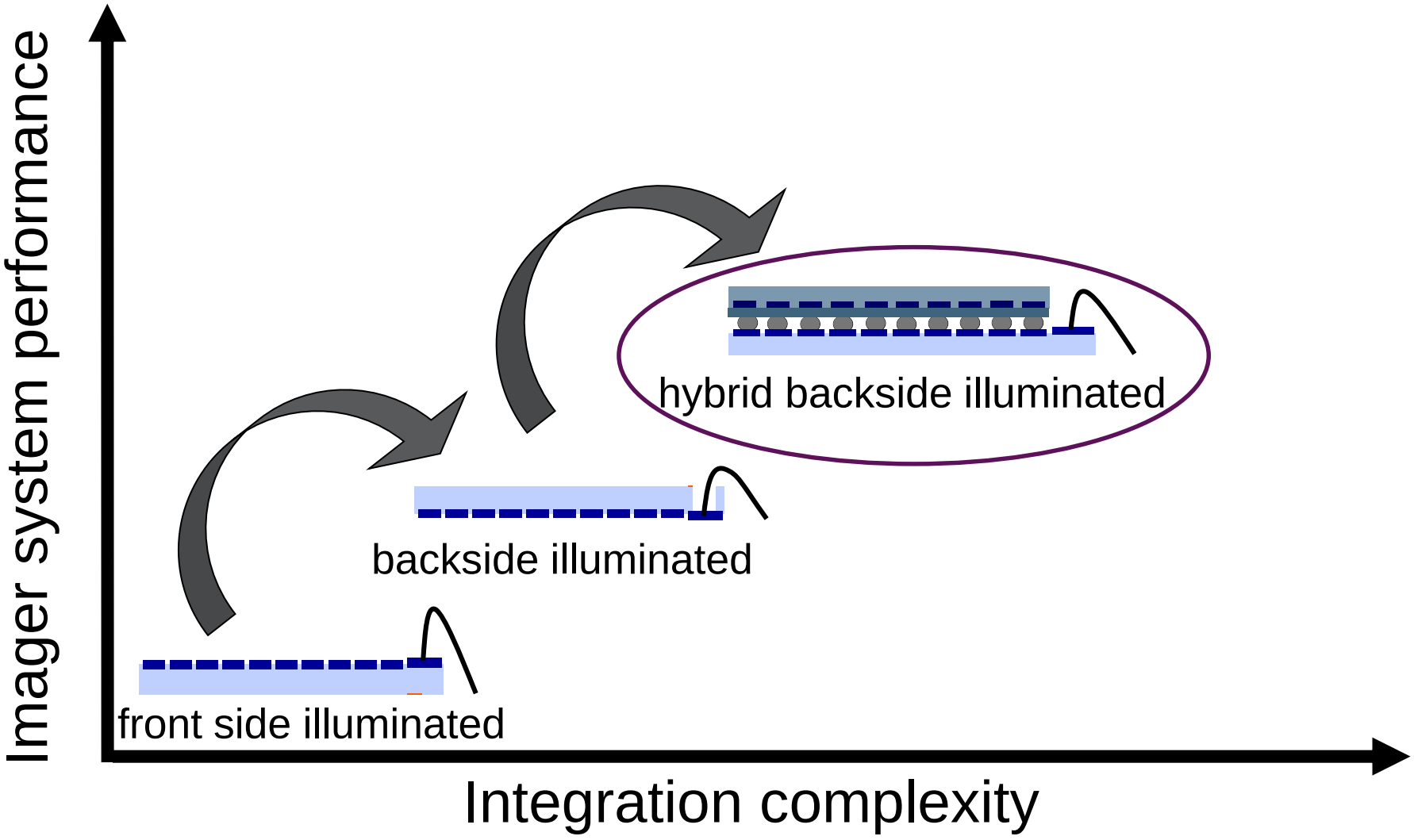
HYBRID (BACKSIDE ILLUMINATED) IMAGERS (HBI)

ADVANCED IMAGER INTEGRATION



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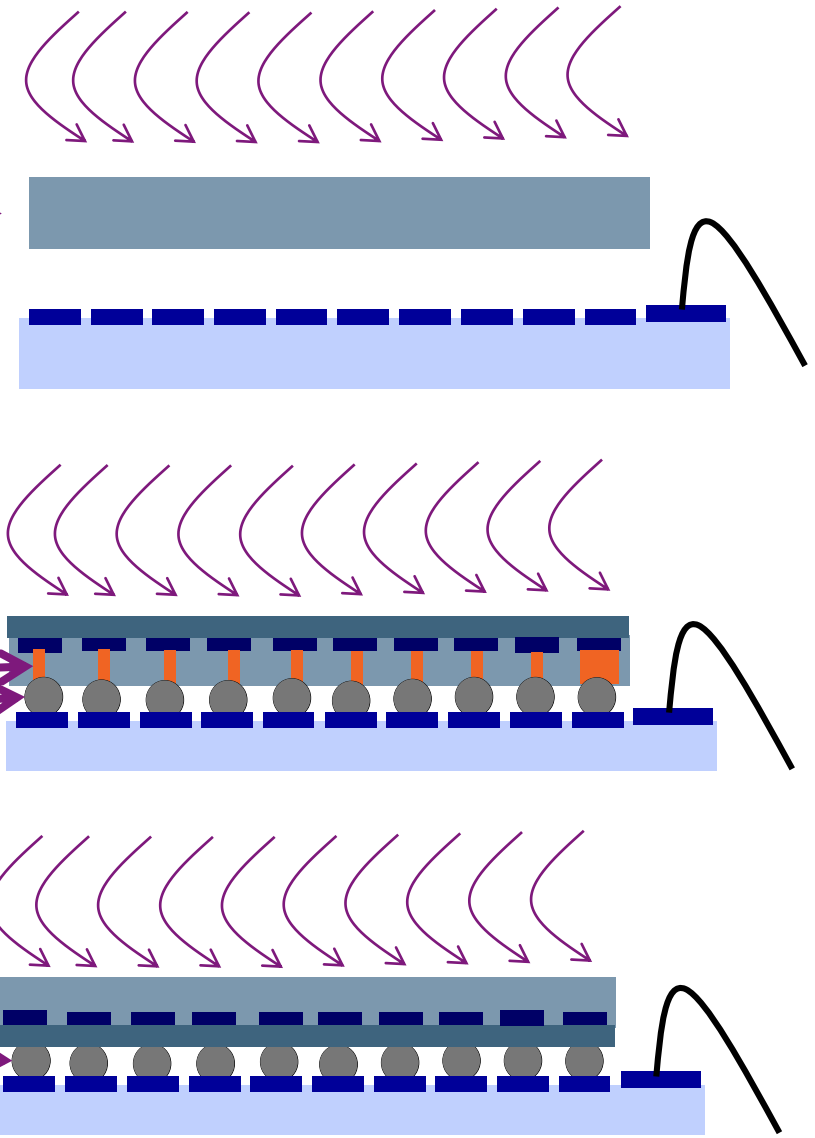
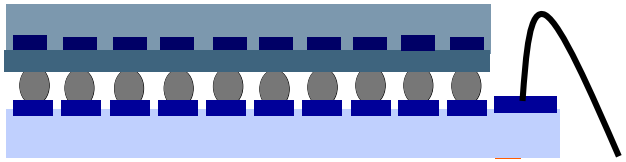
HYBRID IMAGERS: APPROACH

- 2 layers:
  - Detection layer + optional (analog) read-out
  - 2nd read-out layer
- integration options:
  - Front side illuminated::
    - through Si vias (TSVs) + microbumps required
  - Backside illuminated:
    - Backside thinning + microbumps required



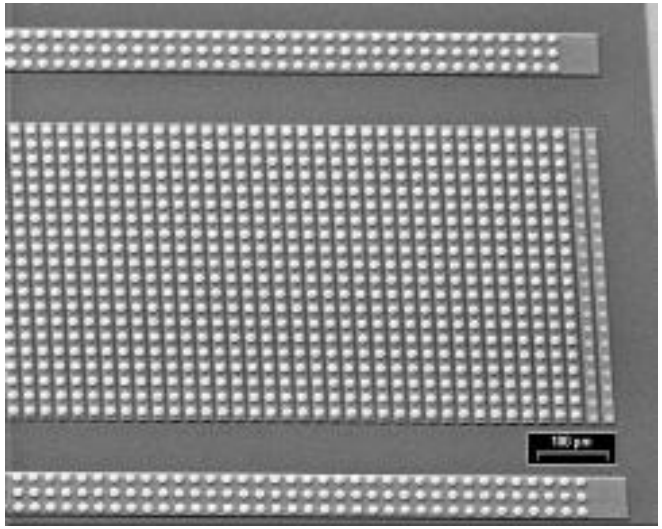
DRIVERS (I): NON-SI IMAGERS

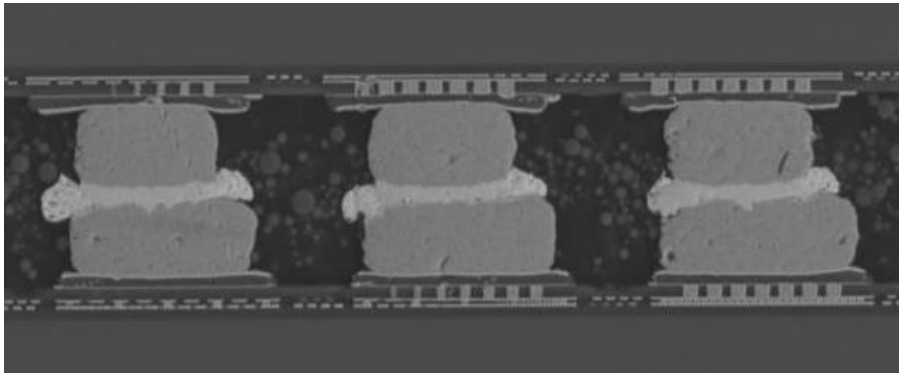


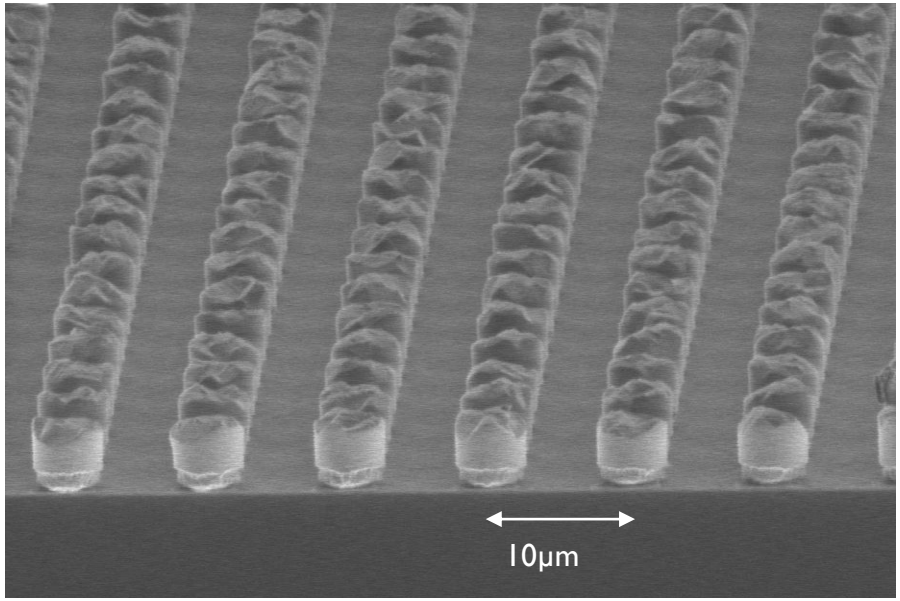
- extension of wavelength range (towards IR) requires non-Si detection layer
- 1D imagers can be wire bonded
- 2D imagers require pixel wise interconnect to Si ROIC = hybrid imager
- standard technology for (near-)IR imagers:
  - InGaAs, HgCdTe, ...
- disadvantages: bump process and flip-chip integration:
  - Cost
  - Scaling to small pixel size (< 10 um) difficult

TECHNOLOGY ENABLER: HIGH DENSITY BUMPING

- In → CuSn microbumps:
  - Post-process at wafer level for both sides:
    - Under-bump metallization (UBM) & patterning
    - Solder deposition & patterning
  - Smallest pitch:
    - 20 um, 10 um under development
- Flip-chip D2D or wafer bonding
- (optional) underfil

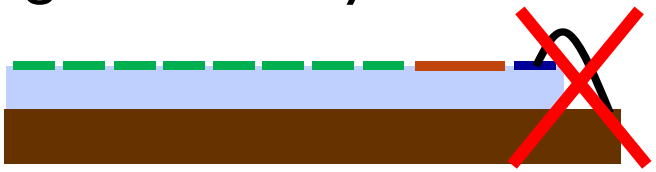


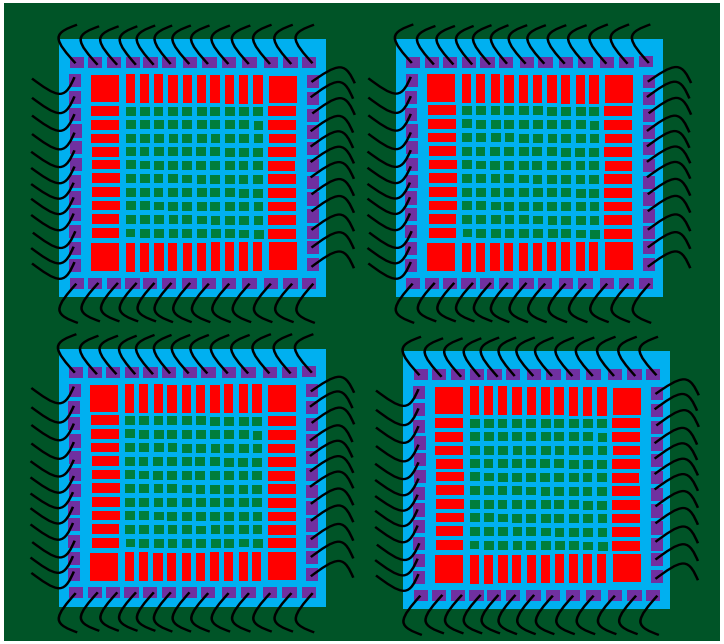


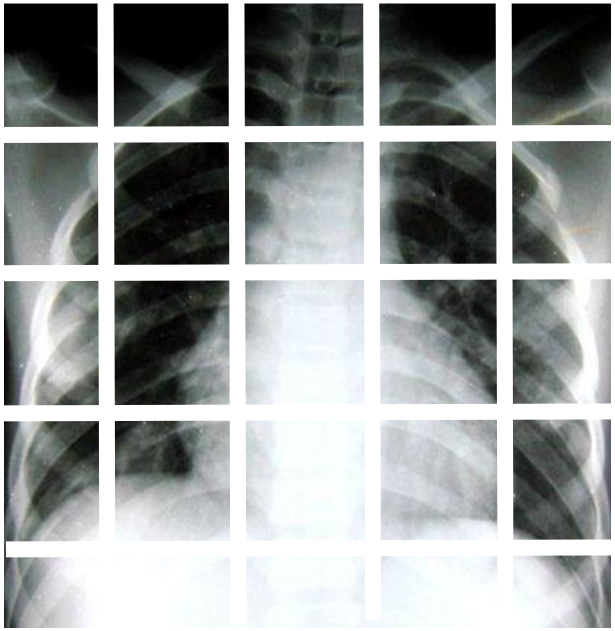


DRIVERS (II):
LARGE AREA/SMALL FOOTPRINT

- applications:
  - consumer imager packaging
  - large area X-ray

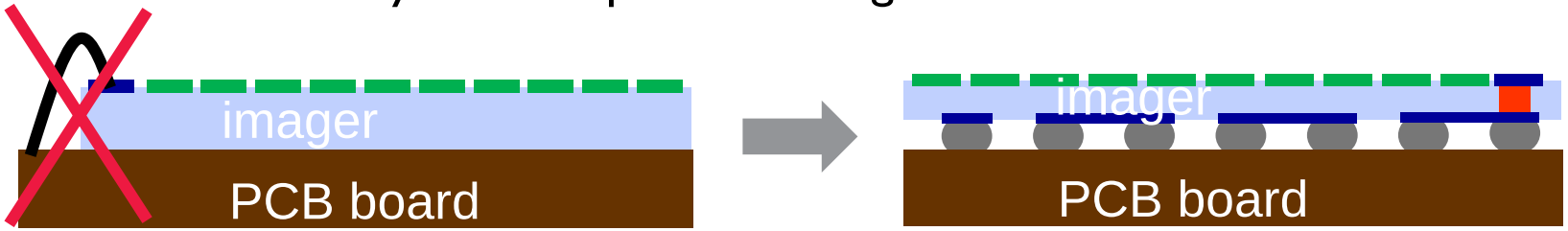






PACKAGING OF IMAGERS

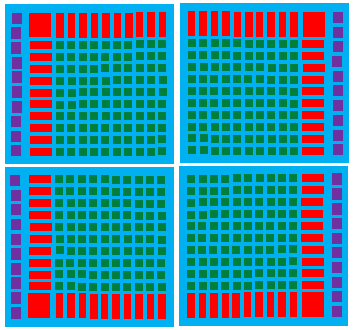
- Advanced packaging technology at bond pad level:
  - Traditional lateral wire bonding → TSV (Through Si Vias) per bond pad + redistribution layer + bump ball bonding

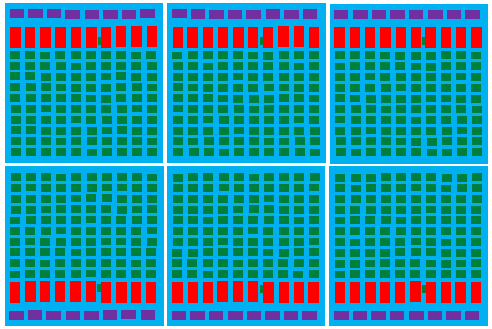


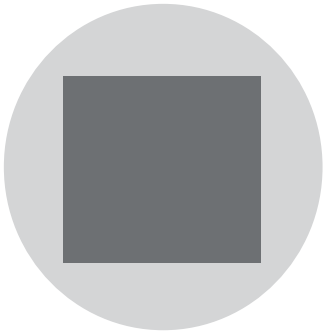
- Advantages:
  - Smaller footprint
  - Reduced capacitance → faster/low power interconnect
- Applications:
  - Consumer imager packaging
  - Endoscopes

SOLUTIONS FOR LARGE AREA IMAGERS

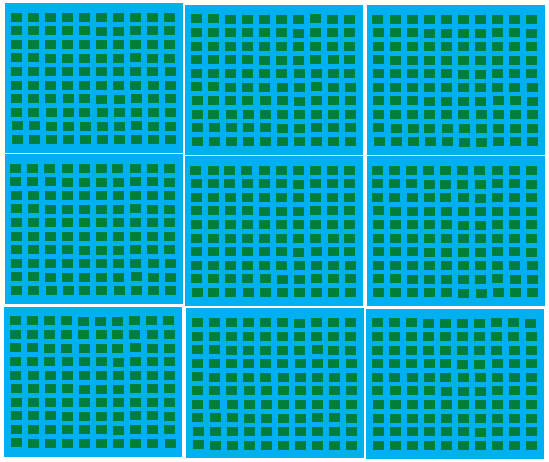
- stitching: yield problem, area limit
- 2-side/3-side buttable/tiling: area limit

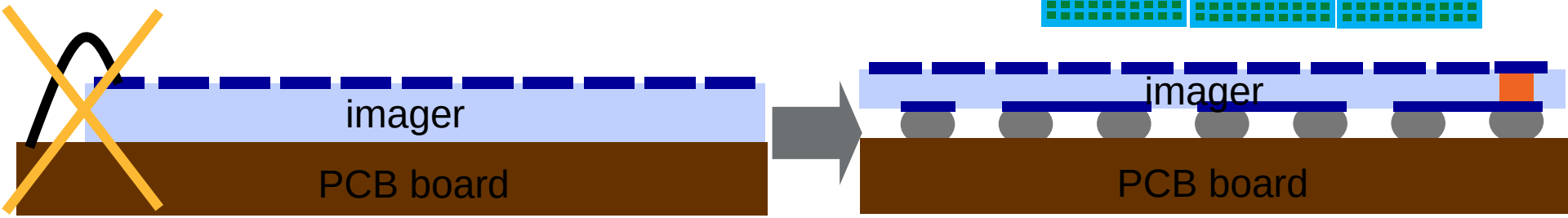




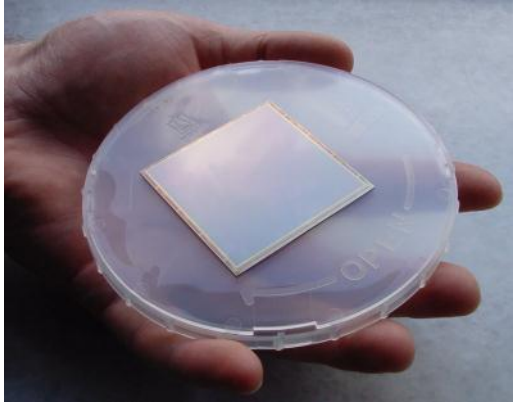


- solution = 4-side buttable using 3D integration
  - minimal non-sensitive area thanks to vertical interconnection

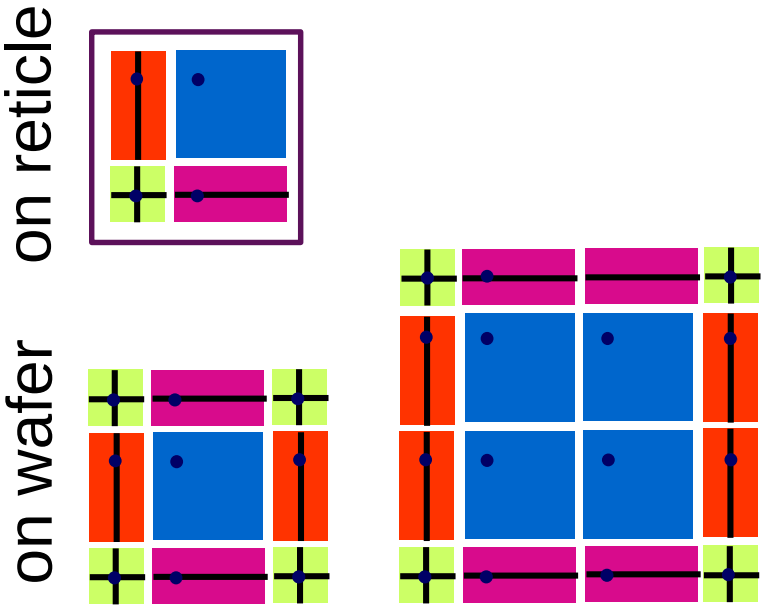


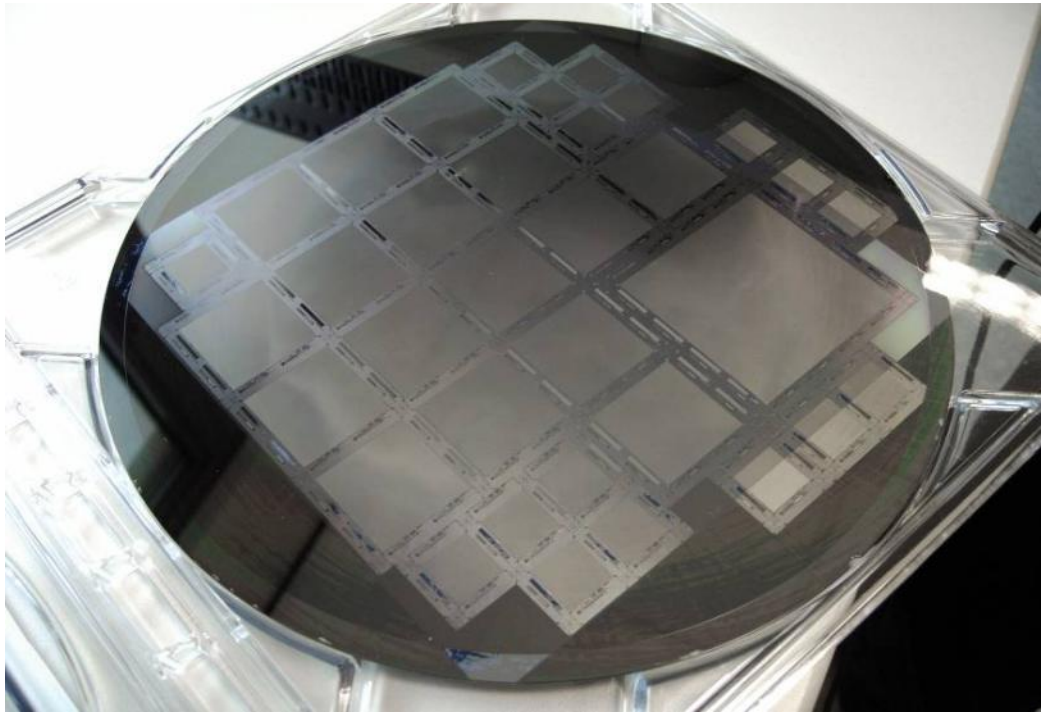


TECHNOLOGY ENABLER: STITCHING



- Stitching allows large area imagers:
  - Up to 1 imager per wafer
- Different imager sizes on one wafer demonstrated:
  - 12x12 mm^2, 25x25 mm^2 and 50x50 mm^2
- Application: e.g. X-ray





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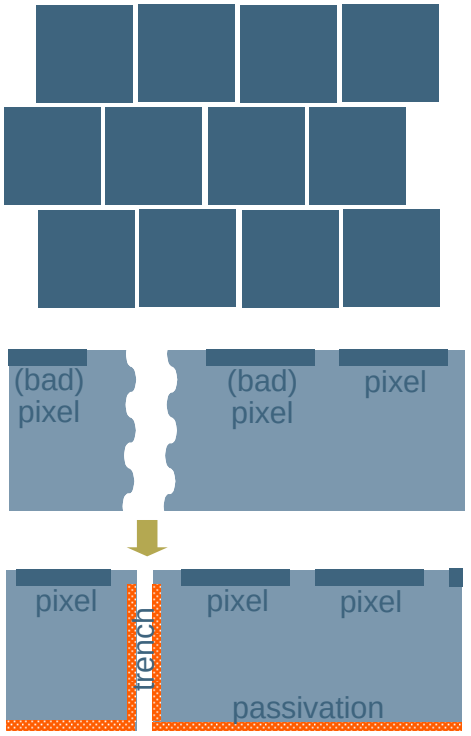
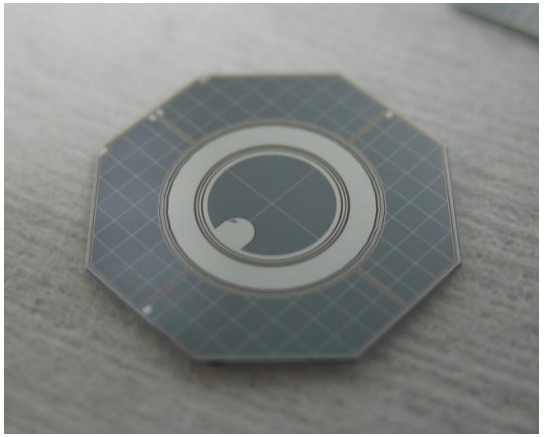
TECHNOLOGY ENABLER: EDGELESS DETECTORS

- Problem of 4-side butting/tiling: dead area between modules:
  - Spacing
  - Bad pixels at edge
- Solution: edgeless imagers = Advanced singulation close to active pixels:
  - Dicing by grinding, stealth dicing
  - Side wall passivation





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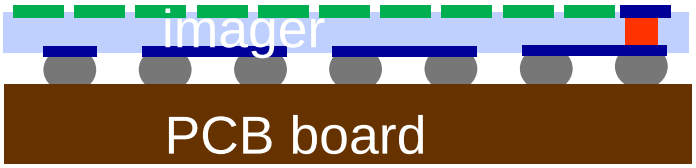
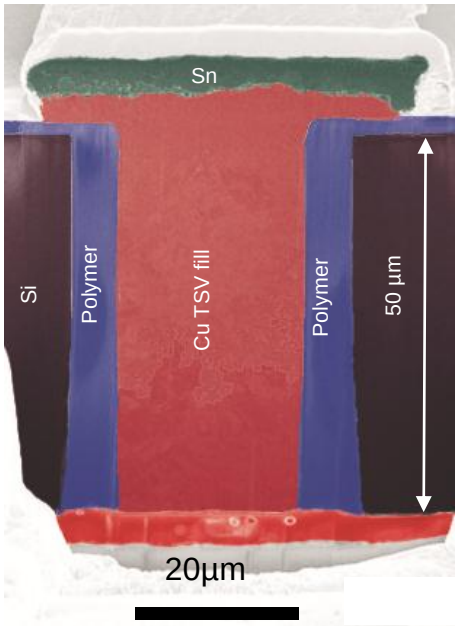
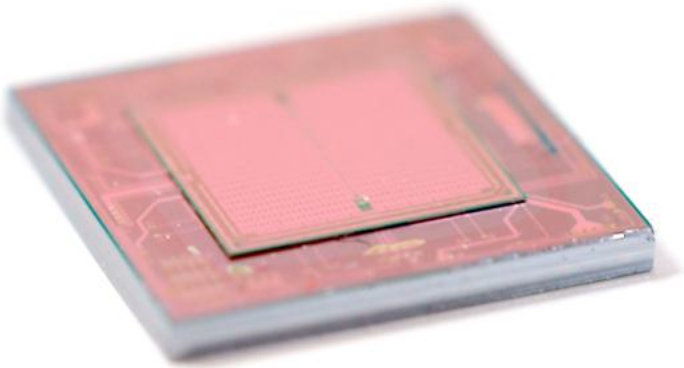
TSV AT BONDPAD LEVEL



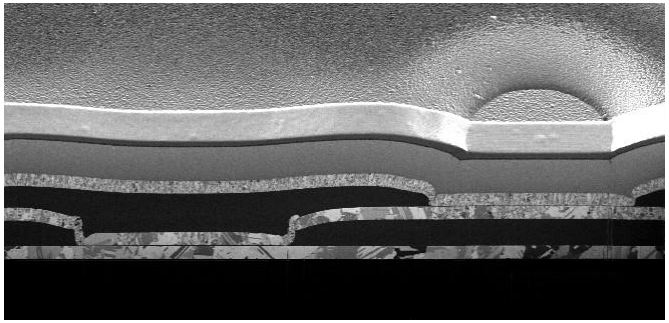
- via-last approach:
  - 1) process CMOS device
  - 2) thin wafer
  - 3) through Si via process
- disadvantage:
  - handling of thin wafer using temporary wafer bonding

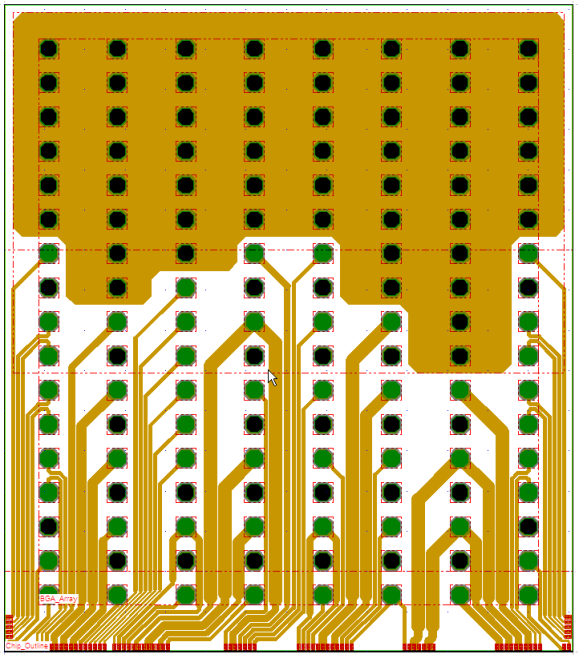


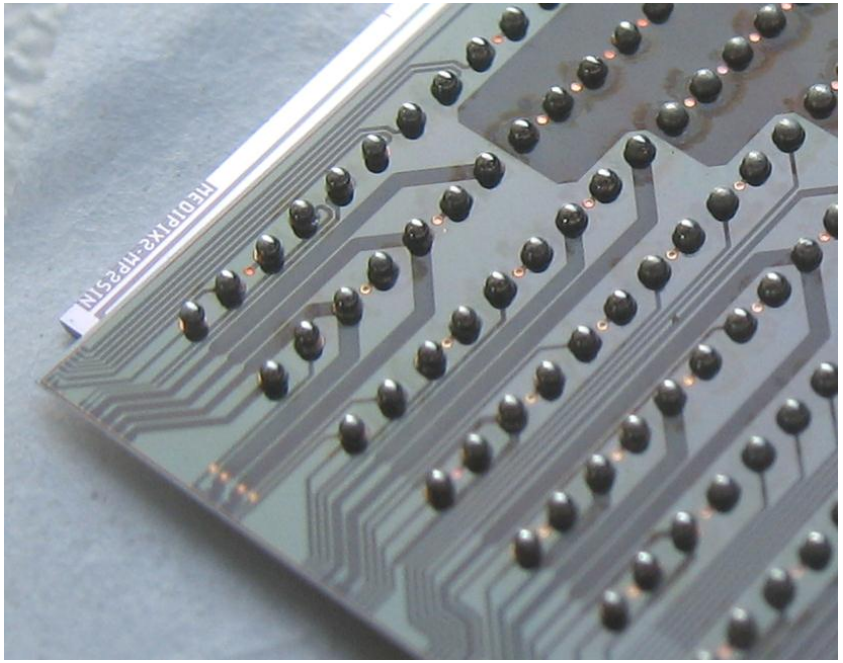


BACKSIDE REDISTRIBUTION AND BUMPING

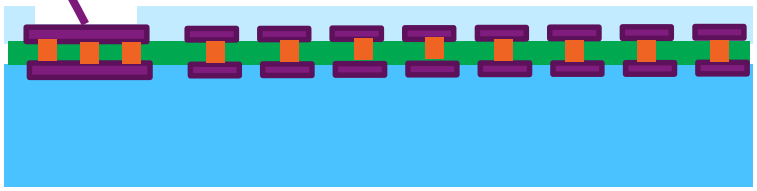
- wafer-level-packaging technology:
  - Cu electroplating and dielectrics (BCB, ...)
  - linewidth: > 5 um lines/space
  - Solder balls







DRIVERS (III) : FAST/SMART SILICON BASED IMAGERS



- 2 active CMOS layers vertically interconnected:
  - Top layer **backside illuminated imager + part of imager readout**
  - Bottom layer: **additional readout electronics**
- Different architectures:
  - Peripheral vertical interconnects
  - Area distributed vertical interconnects

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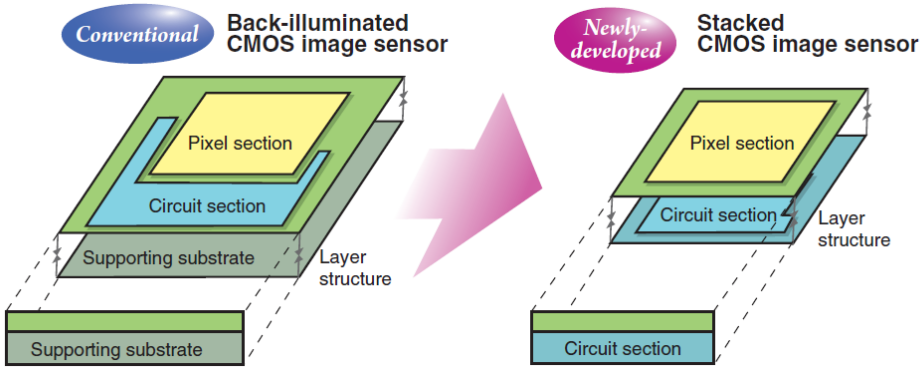
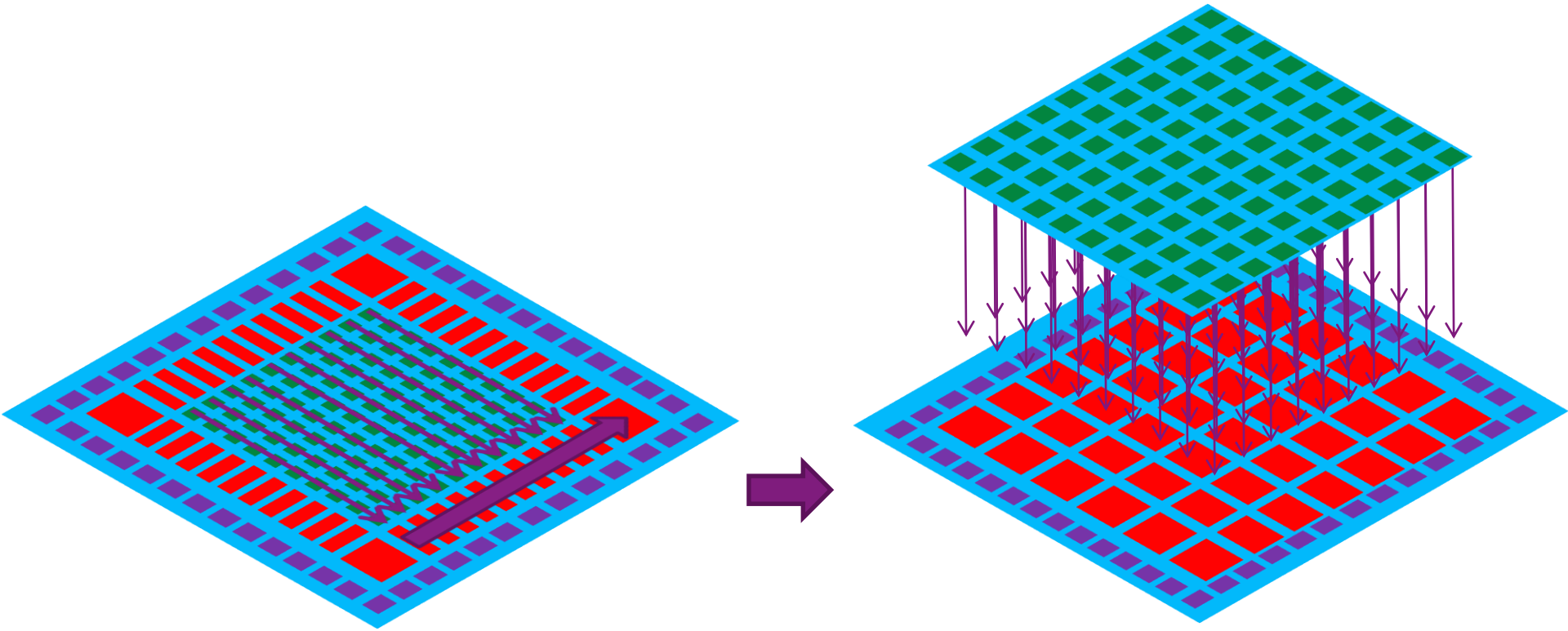
HYBRID IMAGERS IMPLEMENTED BY SONY

- 2-layer imager:
  - top layer: BSI sense layer
  - bottom layer: readout/image processing
- vertical interconnect:
  - only in peripheral electronics
  - using (large) Through Si vias
- advantages (according to Sony):
  - Separate technology use
  - Area reduction



AREA INTERCONNECTED 3D STACKED IMAGERS

- 3D integration using high density vertical interconnects enables:
  - massive parallel vertical readout of pixel array = **high speed**
  - integration of electronics & memory per pixel = **smart imagers**



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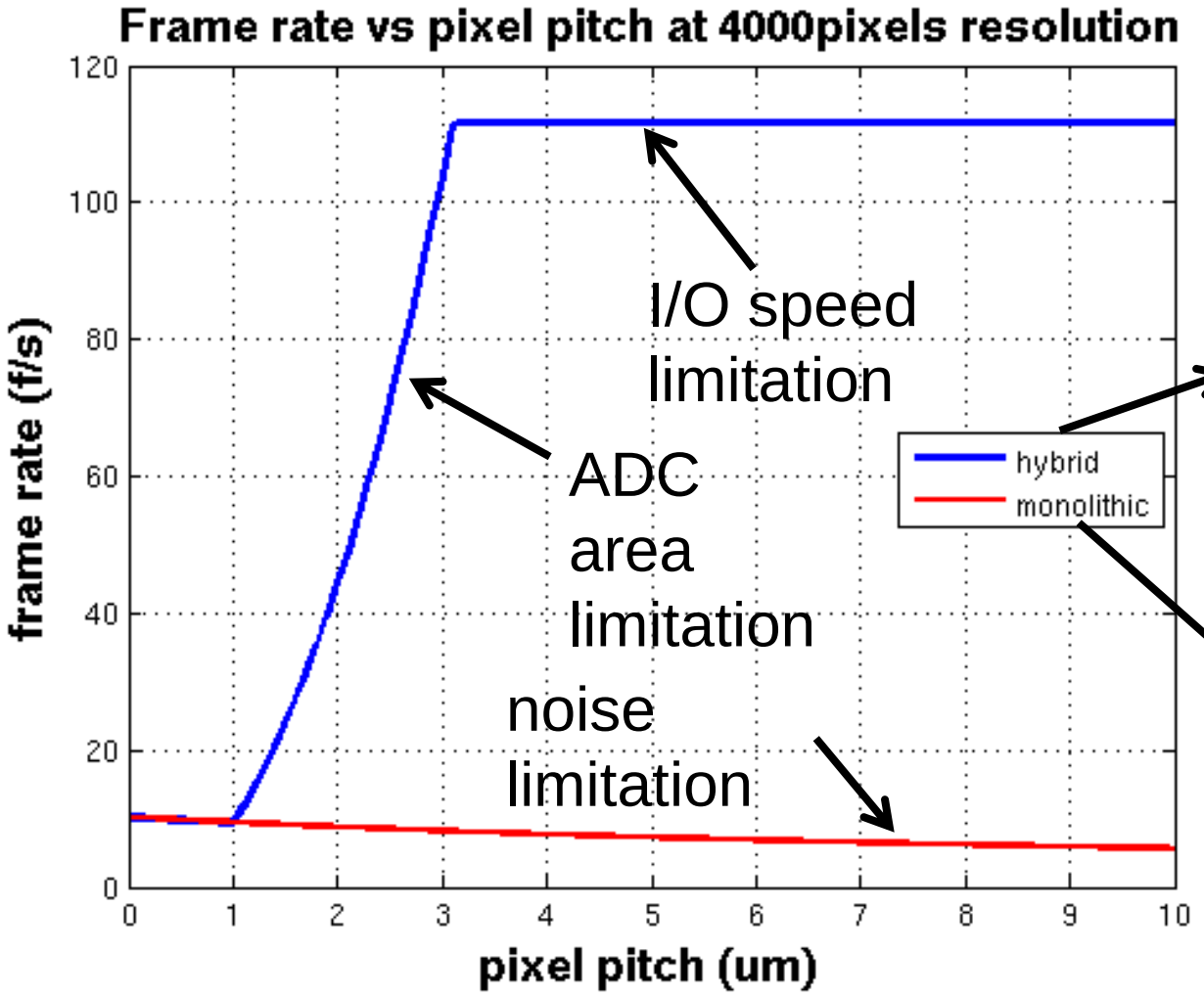
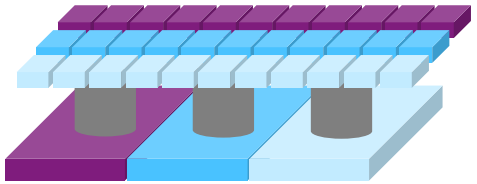
BENCHMARKING HYBRID VS. MONOLITHIC



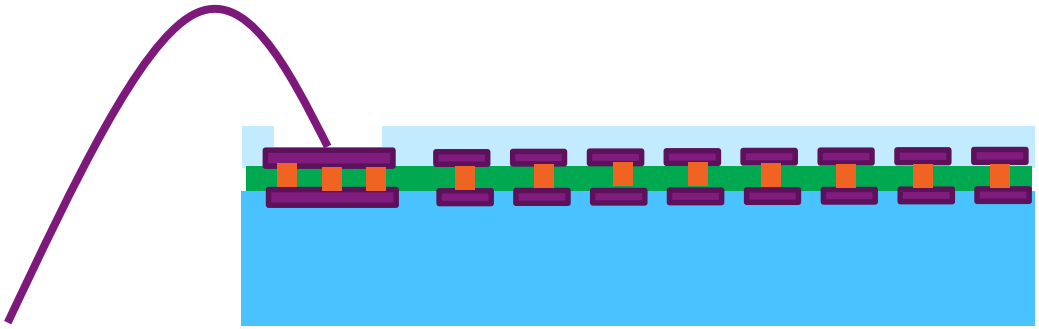


Sub-column addressing + ADC per sub-column

Standard monolithic

Conclusions: enables high speed imaging

HYBRID BSI TECHNOLOGY APPROACH



- Top and bottom die made in (e.g. imec 0.13 um) CMOS
- Wafer to wafer bonding:
  - Mechanical + electrical connection
- Backside illumination module:
  - Backside thinning + passivation
  - Bondpad opening
- Wirebond connection of bottom die using W2W electrical interconnect to top die

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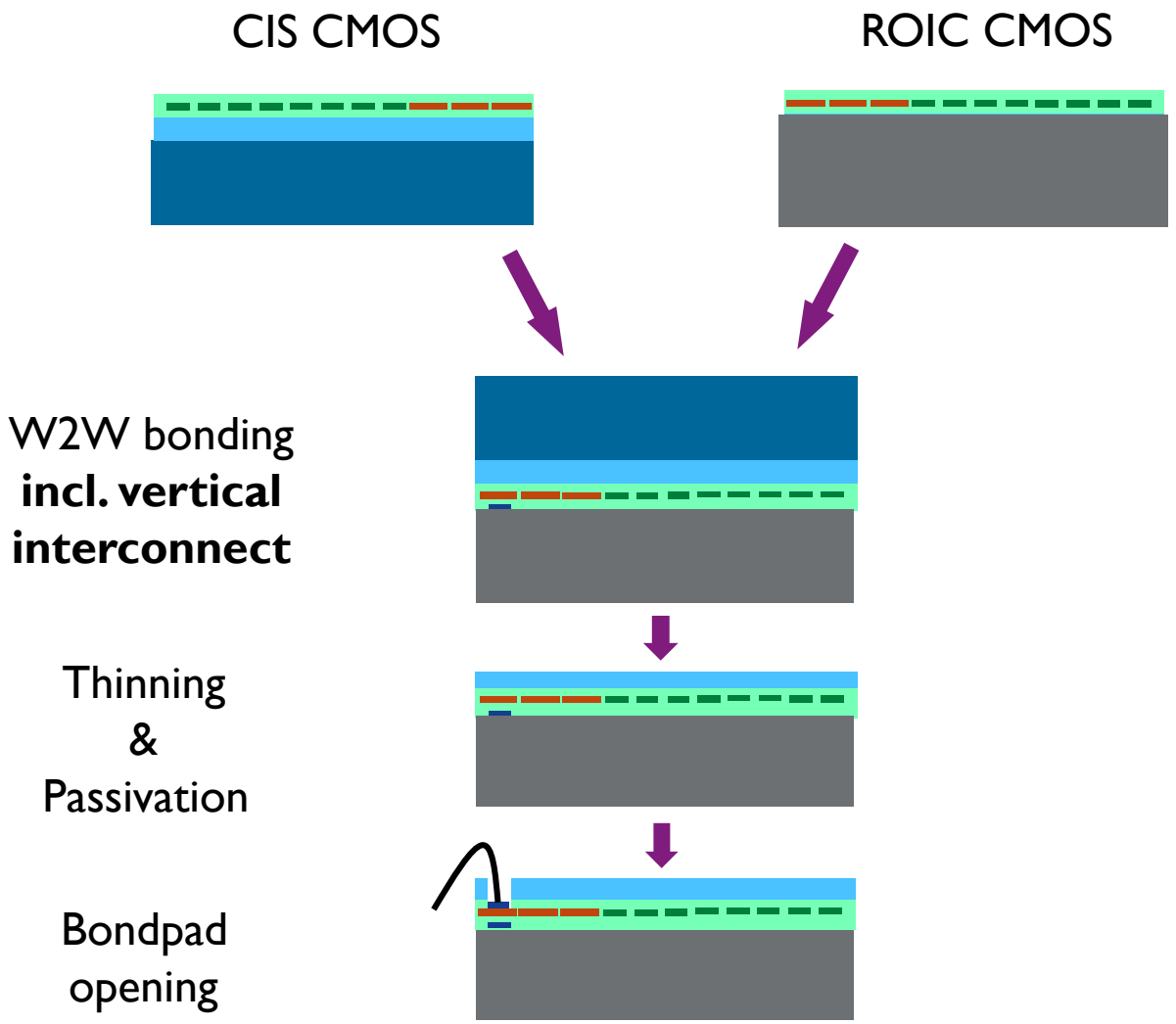
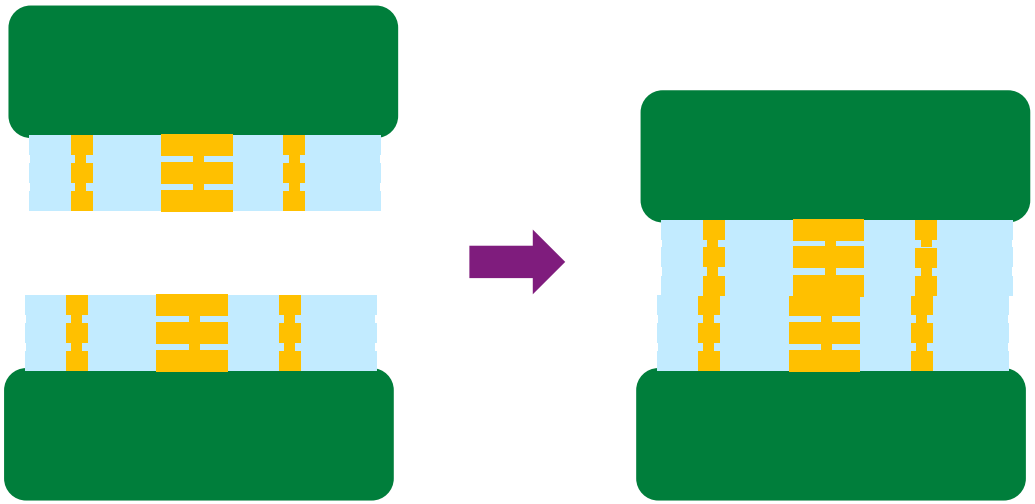
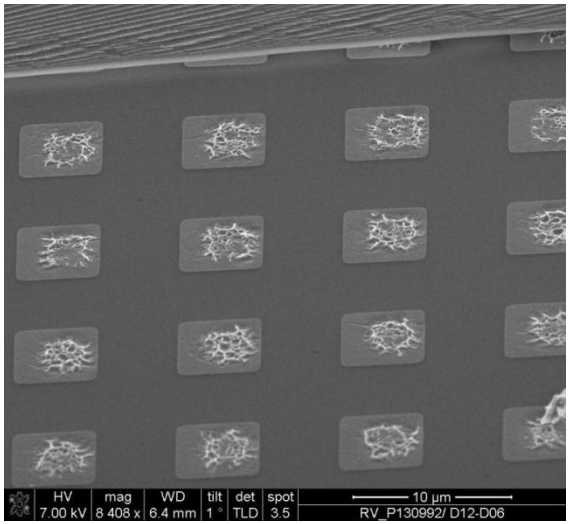
HYBRID BSI FLOW



TECHNOLGY ENABLER:
HYBRID W2W BONDING

- wafer to wafer oxide-oxide + Cu/Cu permanent bonding: critical process
- in-situ alignment with few micron accuracy
- allows high density interconnects: < 10 um pitch
- development ongoing





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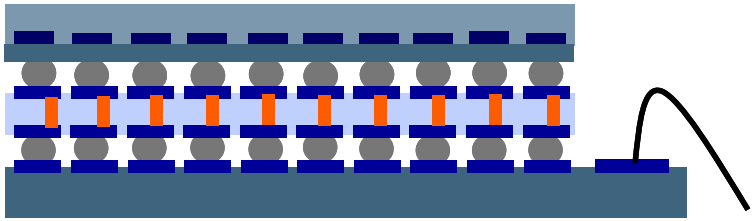
3D STACKED IMAGERS



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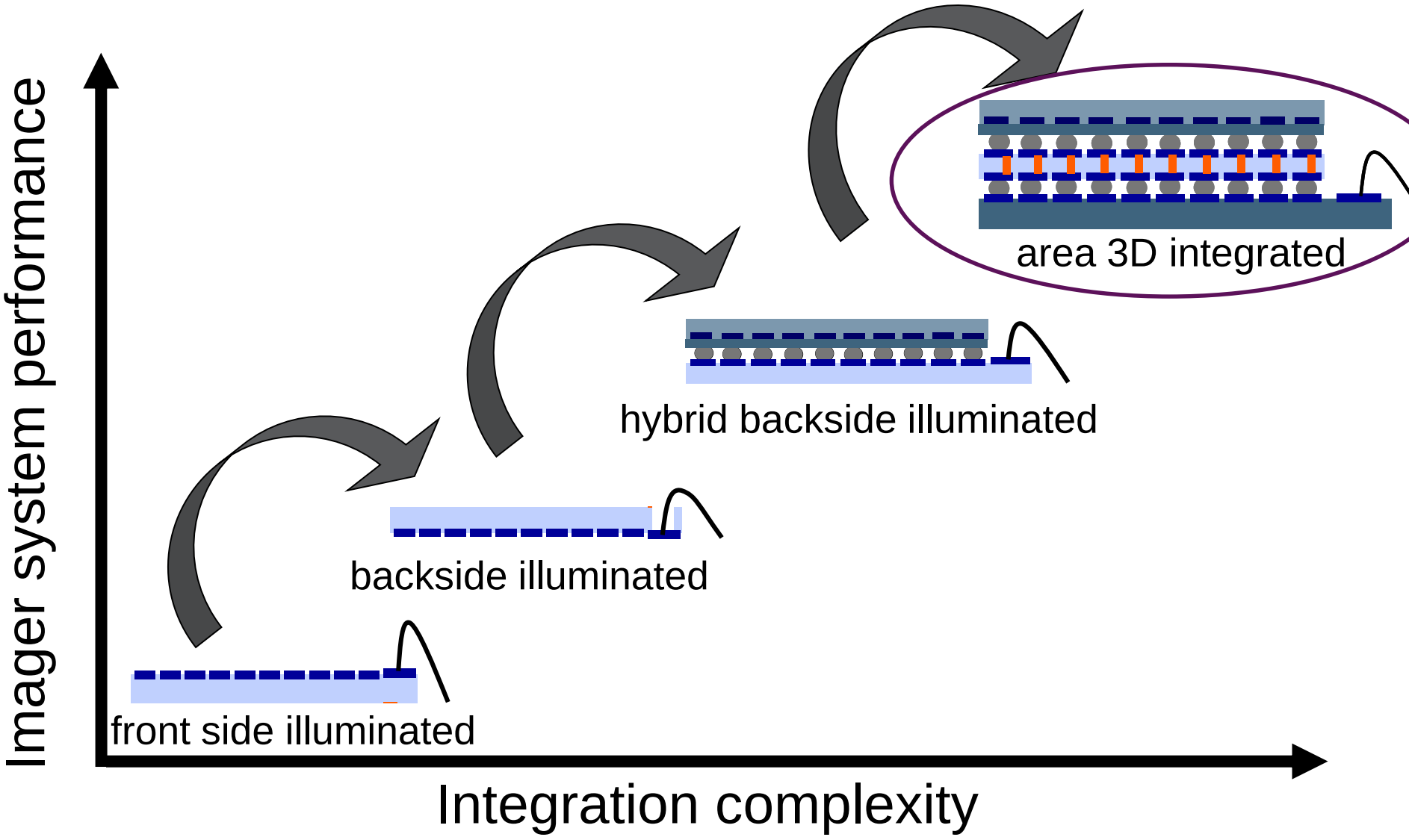
ADVANCED IMAGER INTEGRATION



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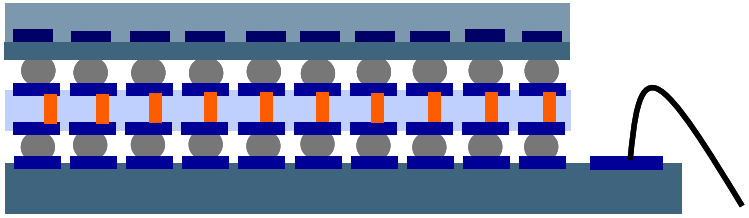
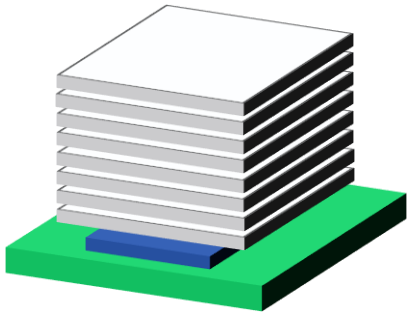
3D STACKED IMAGERS



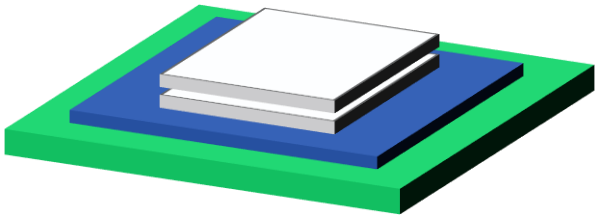
- Concept:
  - Stacking of multiple (>2) layers: detection layer + ROIC layers
    - Example: photodetector layer + analog ROIC + digital image processor
  - Using high density bumping + area redistributed TSVs
- Advantages:
  - General: optimization of (CMOS) technology for different layers
  - Imager system:
    - Vertical parallel readout chain allows high speed
    - Triple (n-fold) area per pixel allows complex electronics per pixel
    - Low capacitance interconnect to digital image processor allows high speed and low power
- Challenge: system architecture:
  - Optimal split in different layers of functionality and technology

3D STACKED IMAGERS: APPLICATIONS

- non-imagers:
  - memory stacking
  - memory



Multi-die Memory stack

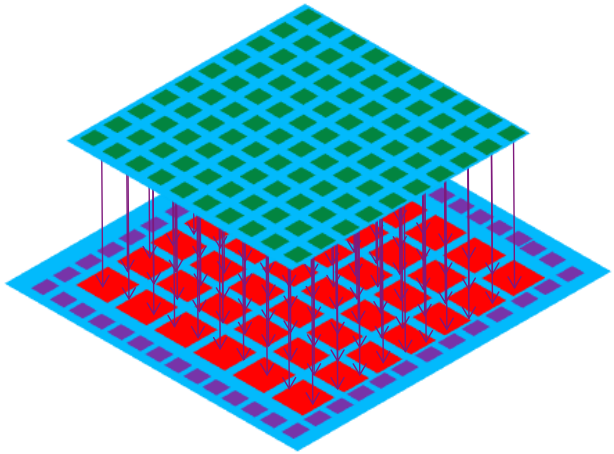


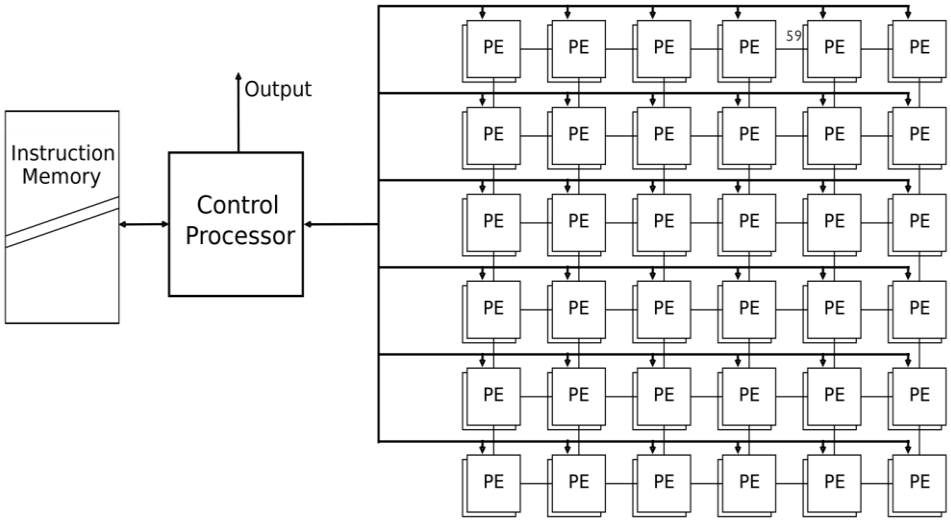
Memory on logic

- imagers:
  - image processing:
    - detection and recognition of faces, roads, cars, ...
    - depth information (3D)
  - image compression

3D STACKED IMAGERS: PARALLEL IMAGE PROCESSING

- area distributed vertical architecture allows parallel processing of image

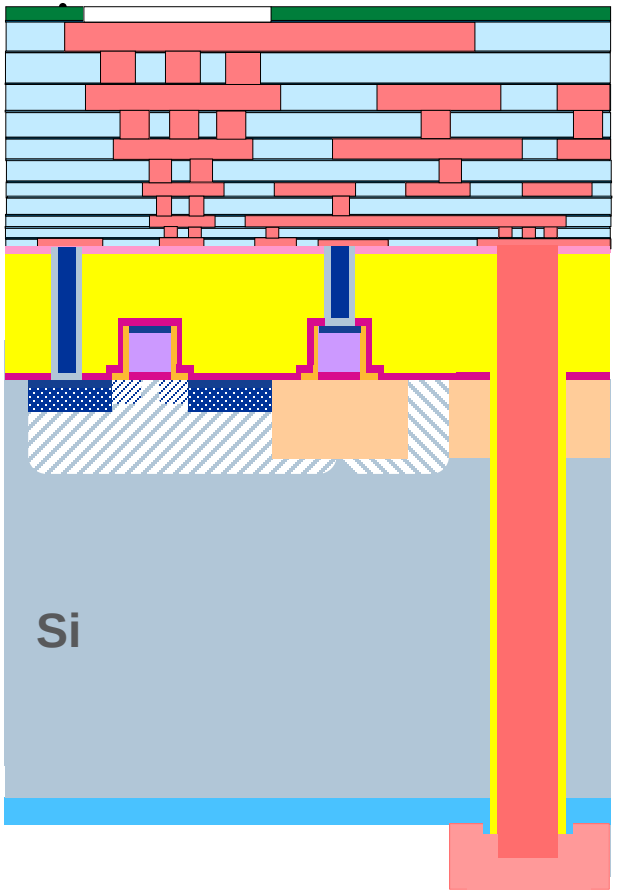


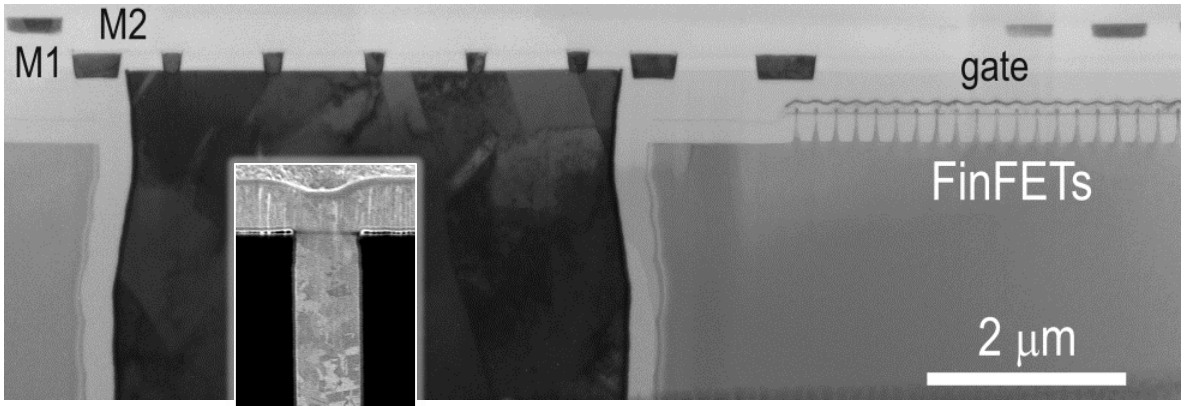


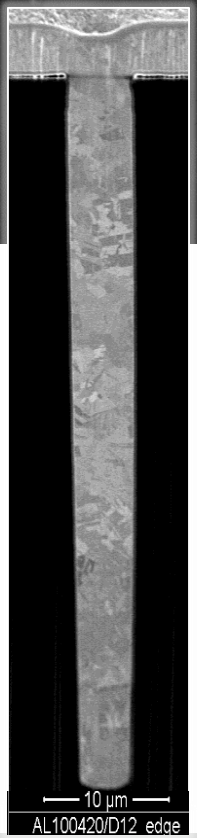
TECHNOLOGY ENABLERS:

THROUGH-SI-VIA PROCESS

- "Via-middle": fabrication TSV's after CMOS FEOL device fabrication processing but before BEOL







imec process:

- ***5 µm diameter;***
- ***50 µm deep;***
- ***Aspect ratio 10***

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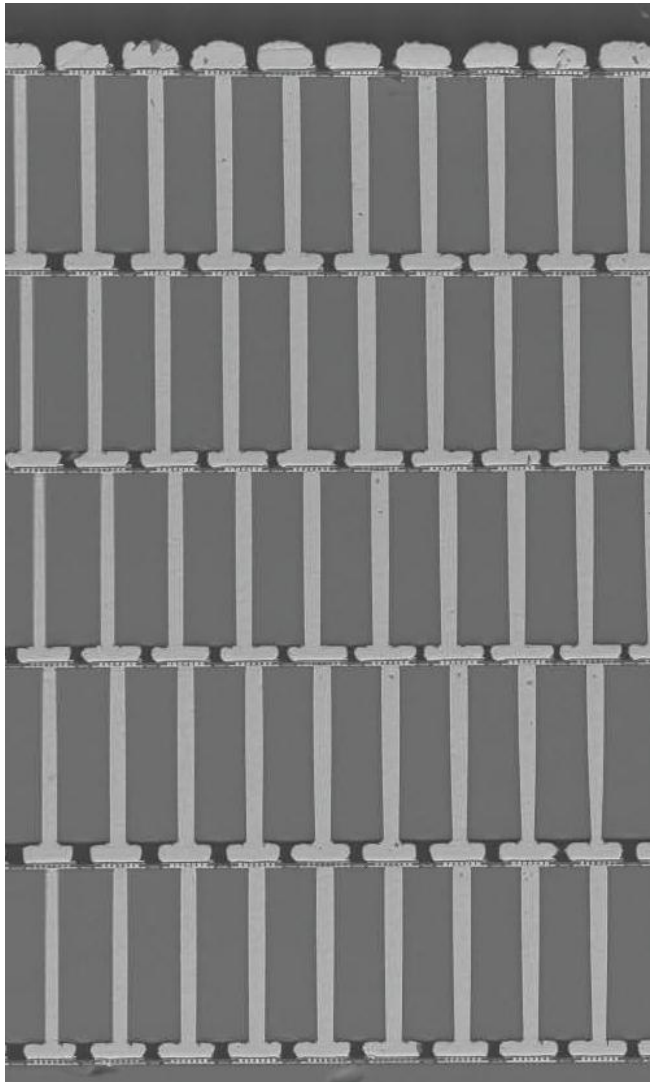
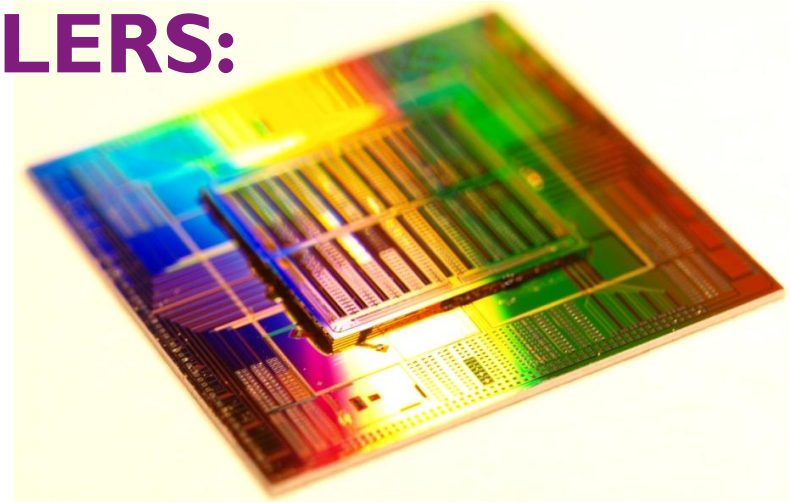
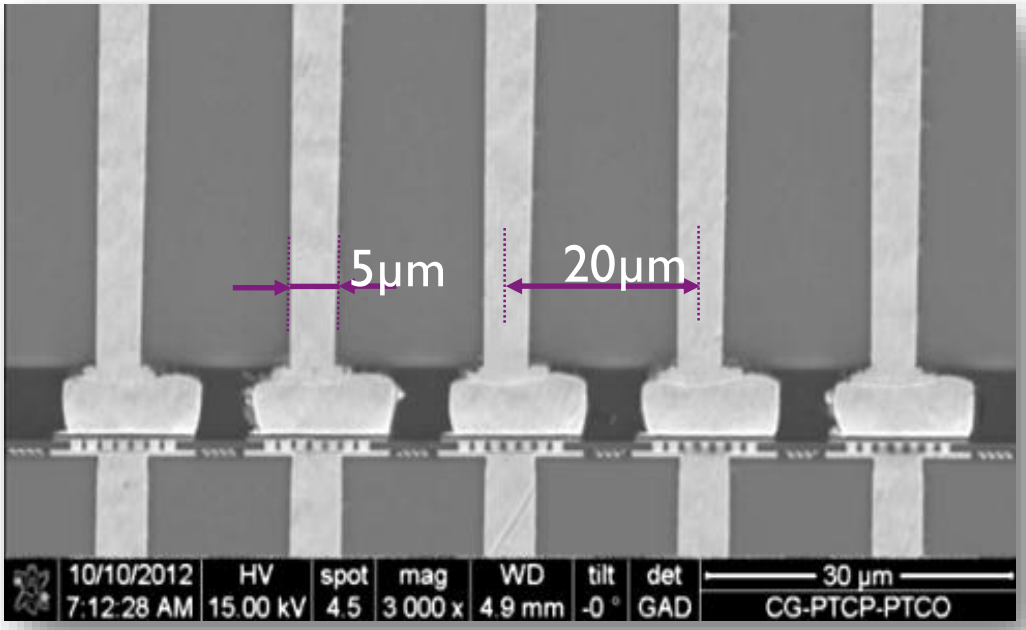
TECHNOLOGY ENABLERS: ASSEMBLY

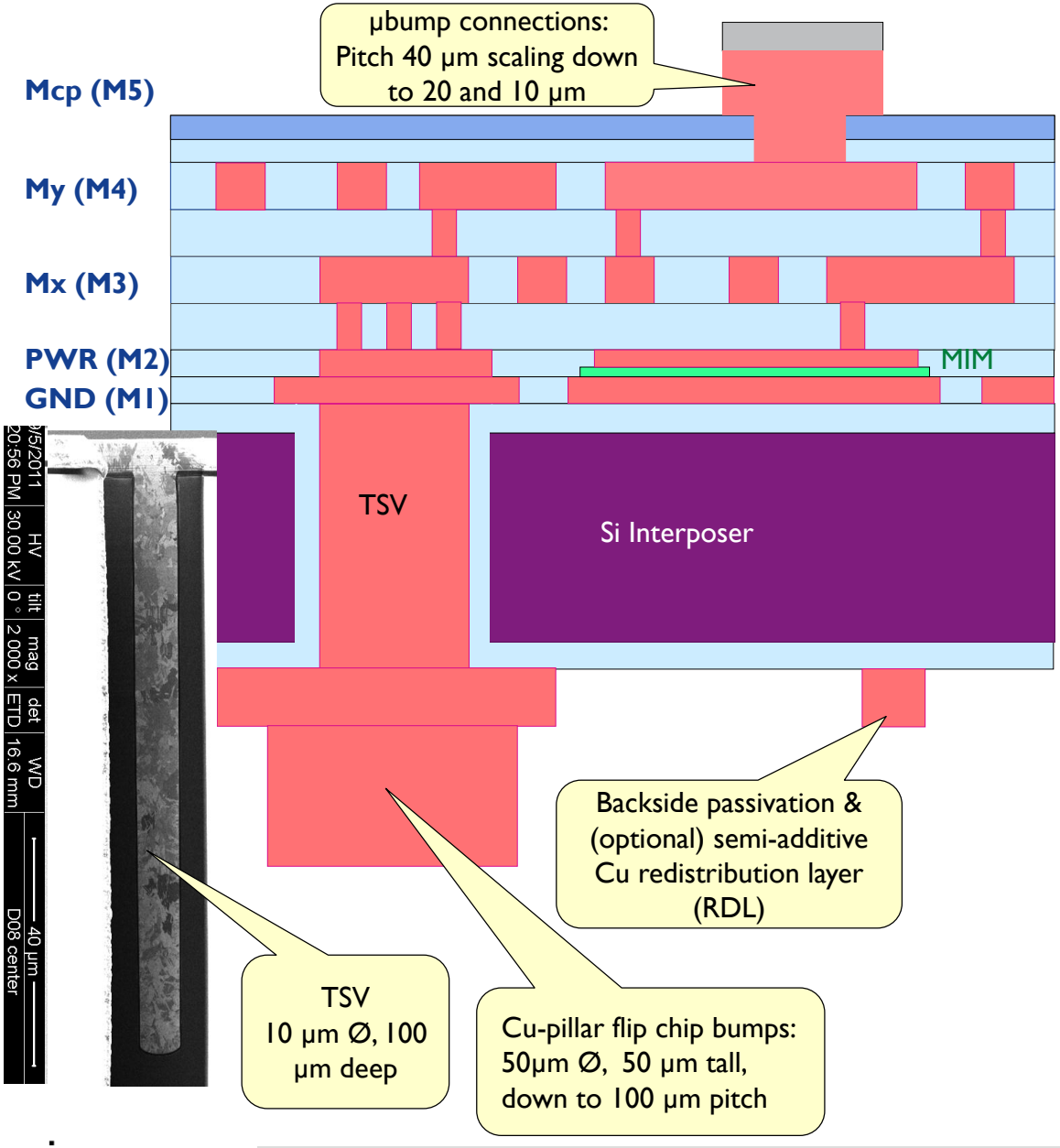




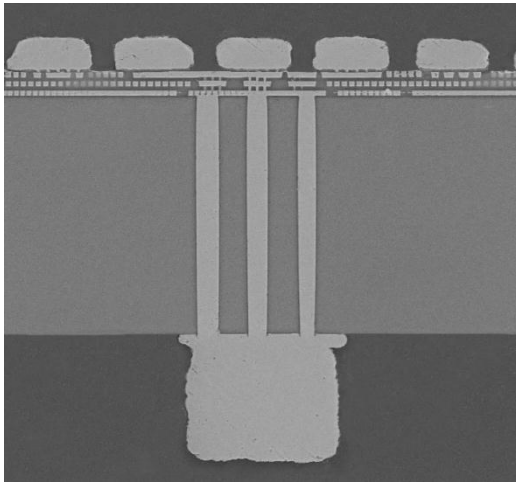
- 6 layer stack demonstrated



TECHNOLOGY: TSV IN INTERPOSER



- TSVs in (passive) interposer substrate
- advantage: standalone fabrication



IMEC 3D SYSTEM INTEGRATION PROGRAM

LOGIC IDM

Panasonic
intel
FUJITSU
SONY

MEMORY IDM

Micron
SAMSUNG
SK hynix

FOUNDRIES

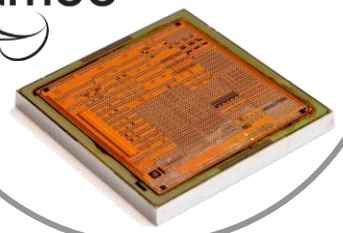
tsmc
GLOBALFOUNDRIES

FABLESS

QUALCOMM
NVIDIA
ALTERA
XILINX

3D PROGRAM

imec



OSAT

Amkor Technology
UTAC

EDA

SYNOPSYS
cadence
ATRENTA

MATERIAL SUPPLIERS

DOW CORNING
brewer science
BASF The Chemical Company
Hitachi Chemical
FUJIFILM

TECHNOLOGY SUPPLIER

ziptronix

EQUIPMENT SUPPLIERS

SUSS MicroTec
Lam RESEARCH
APPLIED MATERIALS
Besi
CascadeMicrotech
Ultratech
TEL TOKYO ELECTRON
PVA TePla
DISCO
Camtek
Entegris

CONCLUSIONS

- there is a future for 3D stacked imaging systems
- application specifications define the required 3D integration technology
- trade-off: performance vs. cost
- technology blocks are becoming mature (with delay):
  - wafer thinning
  - high density D2D and W2W vertical interconnect technology
  - TSV technology
- technology access remains difficult:
  - (large volume) consumer products first by vertically integrated companies
  - no commercial access (yet) for (ultra) low volume
  - research institutes are moving to prototyping and LVM

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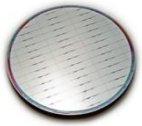
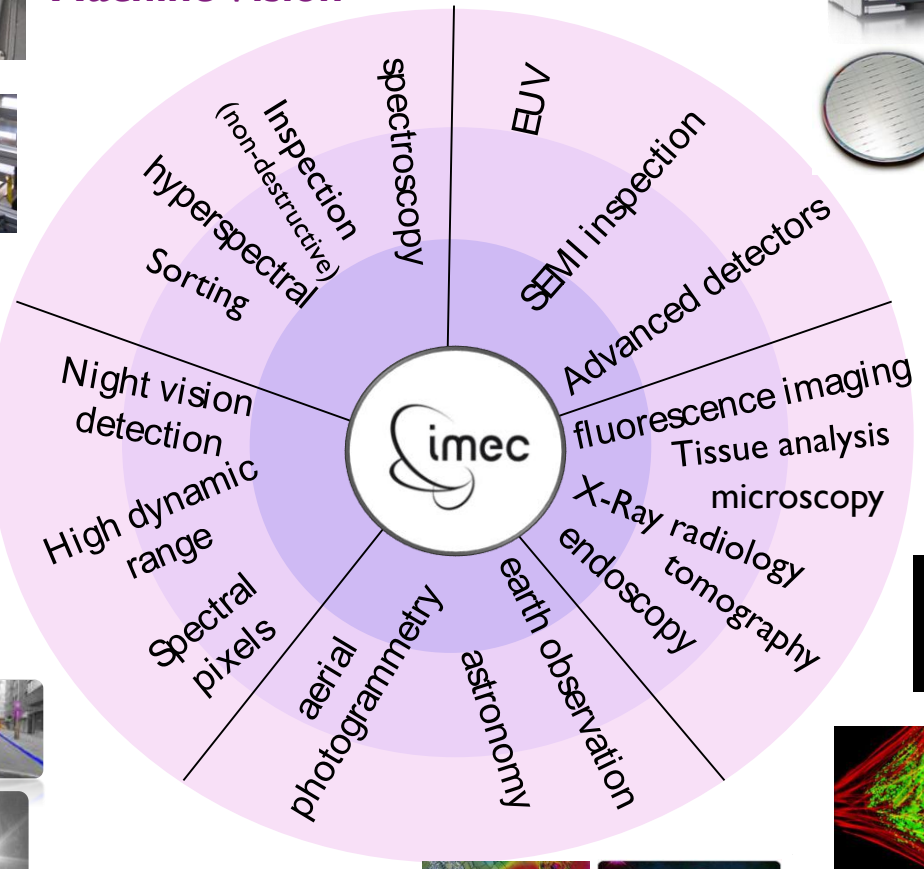
HIGH-END IMAGERS: APPLICATIONS & FEATURES

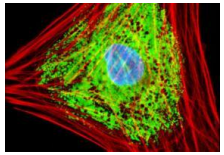
Industrial sorting & Machine Vision

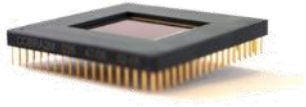
Industrial Instrumentation





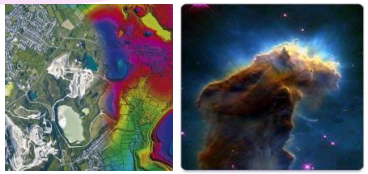
Life-Science & Medical Imaging





High-end **transports, security & surveillance**

Space, Physics & Scientific



Key features

- Low noise
- High QE
- Low power
- High speed
- Radiation Hard
- Non-Visible sensing
- Spectral Filters/ARC

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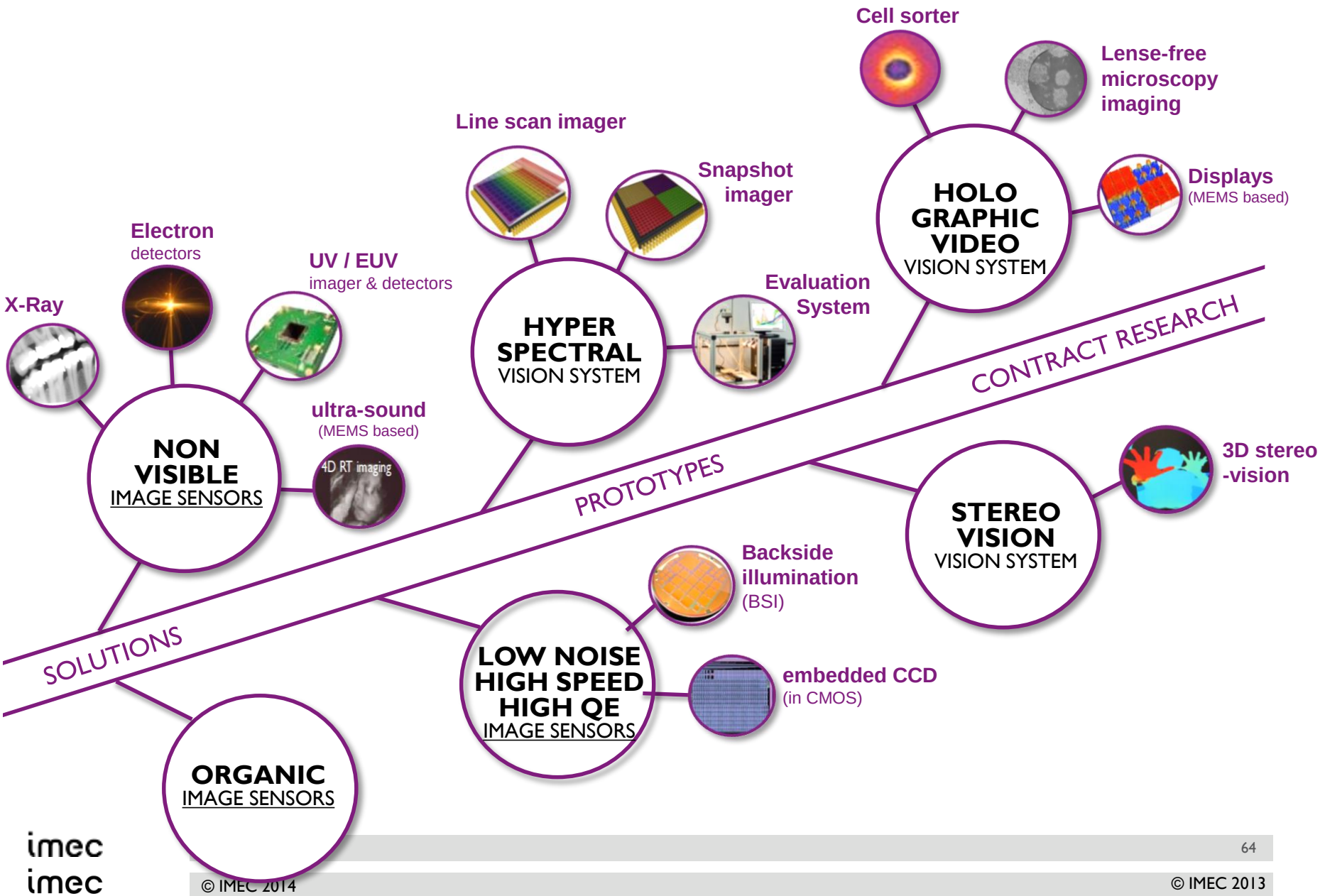
IMEC IMAGERS & VISION SYSTEMS



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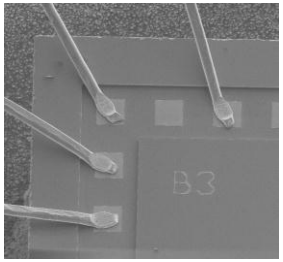
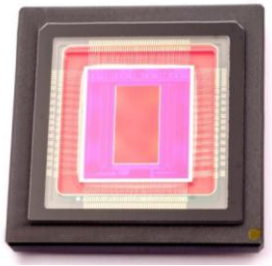
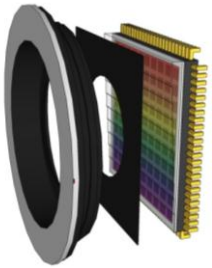
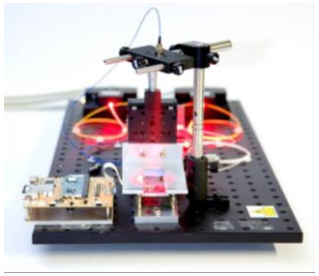
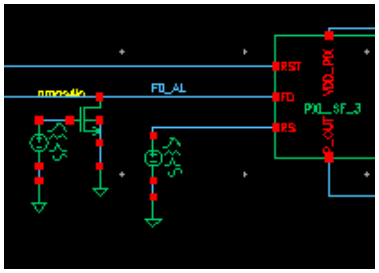
IMEC OFFERING:

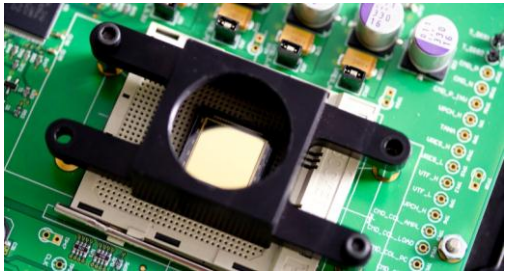
- **Advanced vision systems solutions**



- **Innovation at technology, design and system level**





- **From R&D to Low Volume Production**

Research & Development → Prototyping → Low Volume Production

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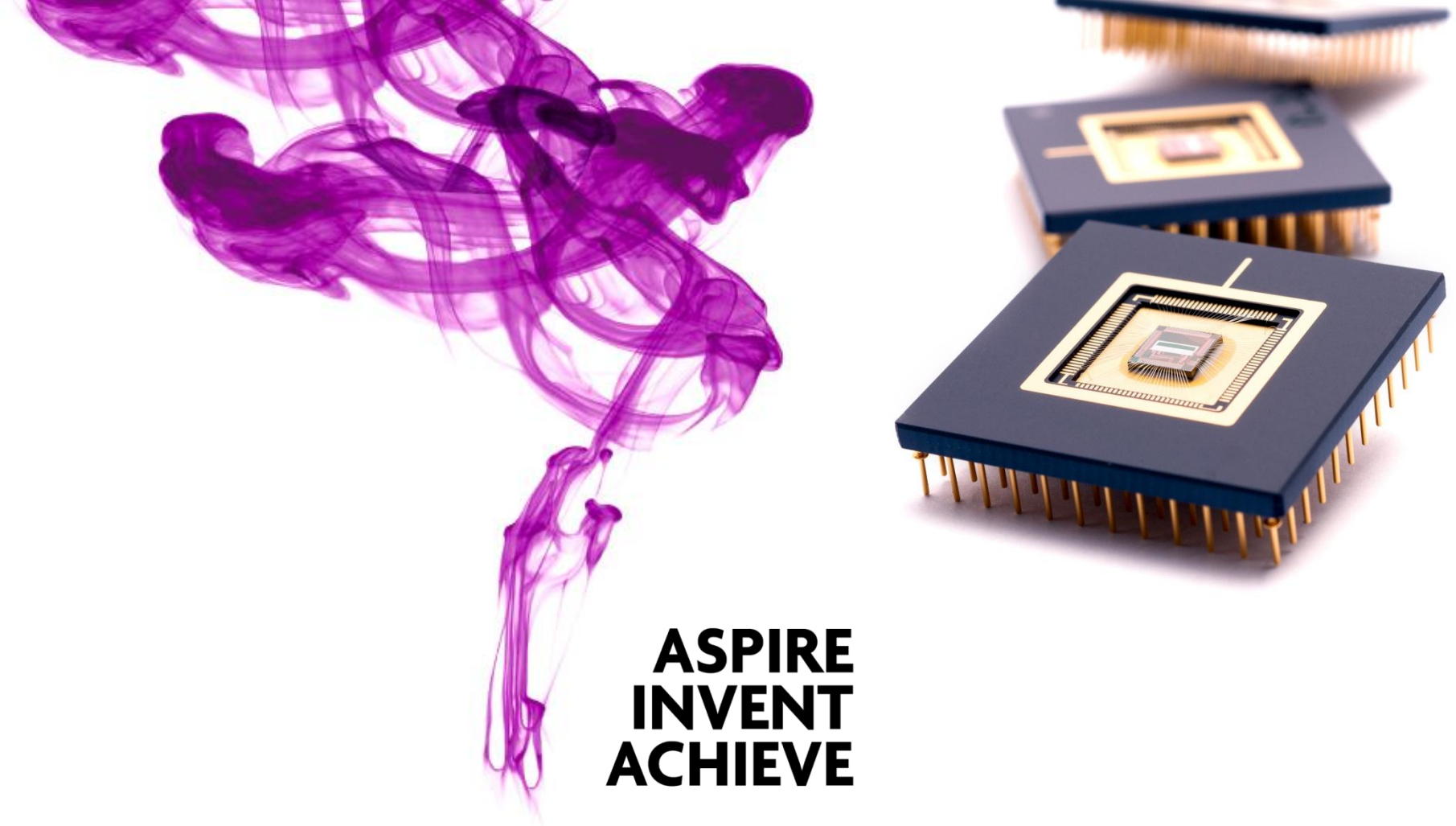

ASPIRE
INVENT
ACHIEVE

imec