PAUL SCHERRER INSTITUT

PSI

Wir schaffen Wissen – heute für morgen

Paul Scherrer Institut

Manuel Brönnimann on behalf of Section LLRF

Status WP 8.2 RF Low Level Electronic

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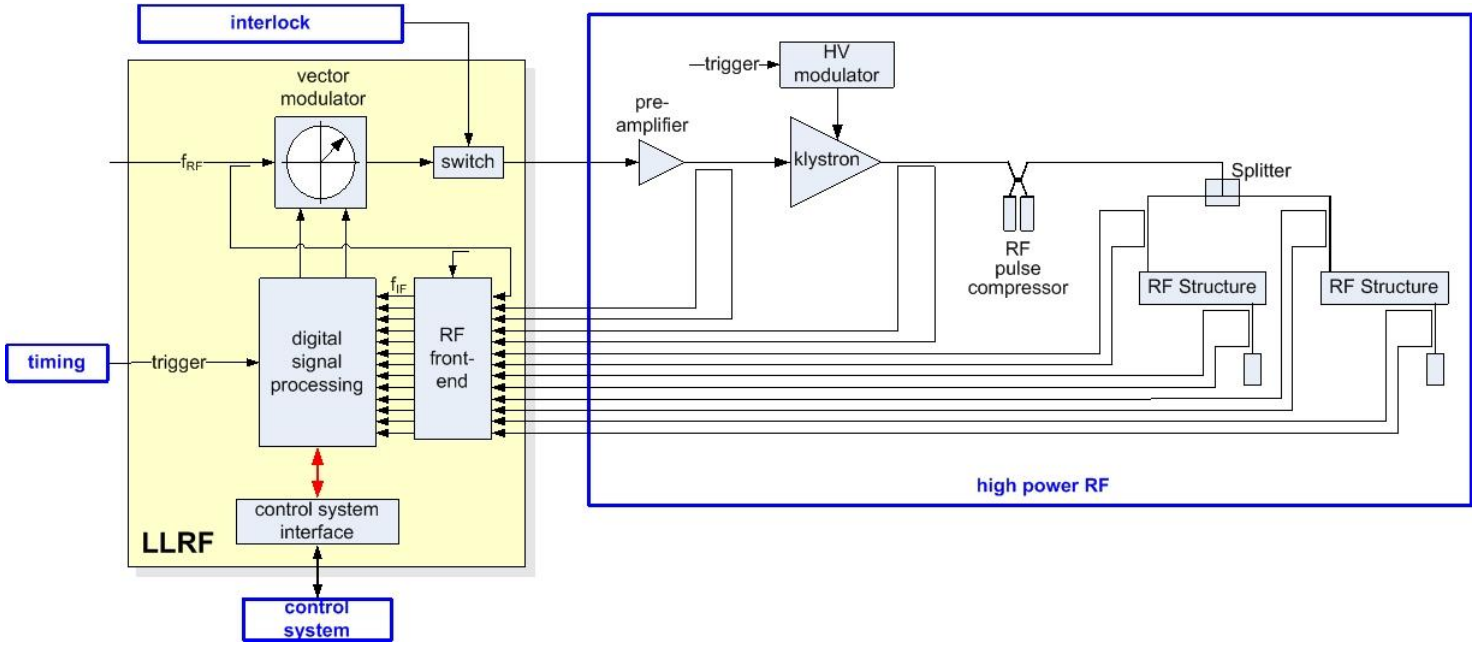
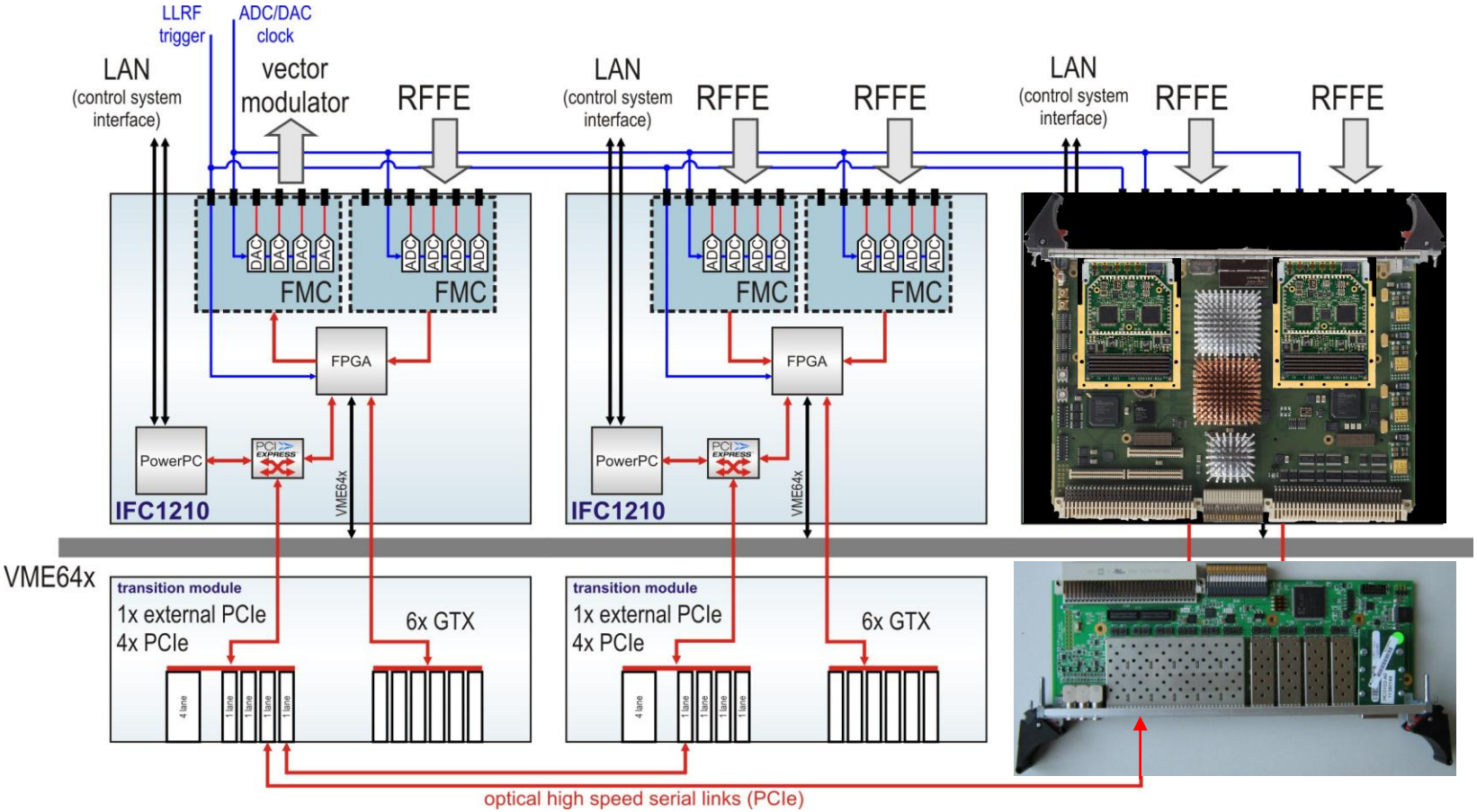
LLRF overview



- Stable and flexible LLRF system for monitoring the shot to shot jitter and for providing corrections to compensate drifts of the systems with feedbacks
- Very stable RF signal for the klystron power amplifier
- Fast phase modulation during RF pulse is required for operation of the RF pulse compressor
- LLRF sampling frequency has to be synchronous to SPARC gun laser frequency
- Phase resolution < 15fs ≈ 0.03° @ 5712 MHz
- Detection bandwidth = 17.8 MHz from carrier to -3dB point

Digital LLRF hardware



- 8 x IFC1210 pre-serial boards from the company IOxOS at PSI for testing
- In-house developed transition modules have been tested successfully
  => due to minor layout bug we launched a redesign
- Commercial FMC boards from different companies have been tested successfully
  => characterisation is ongoing

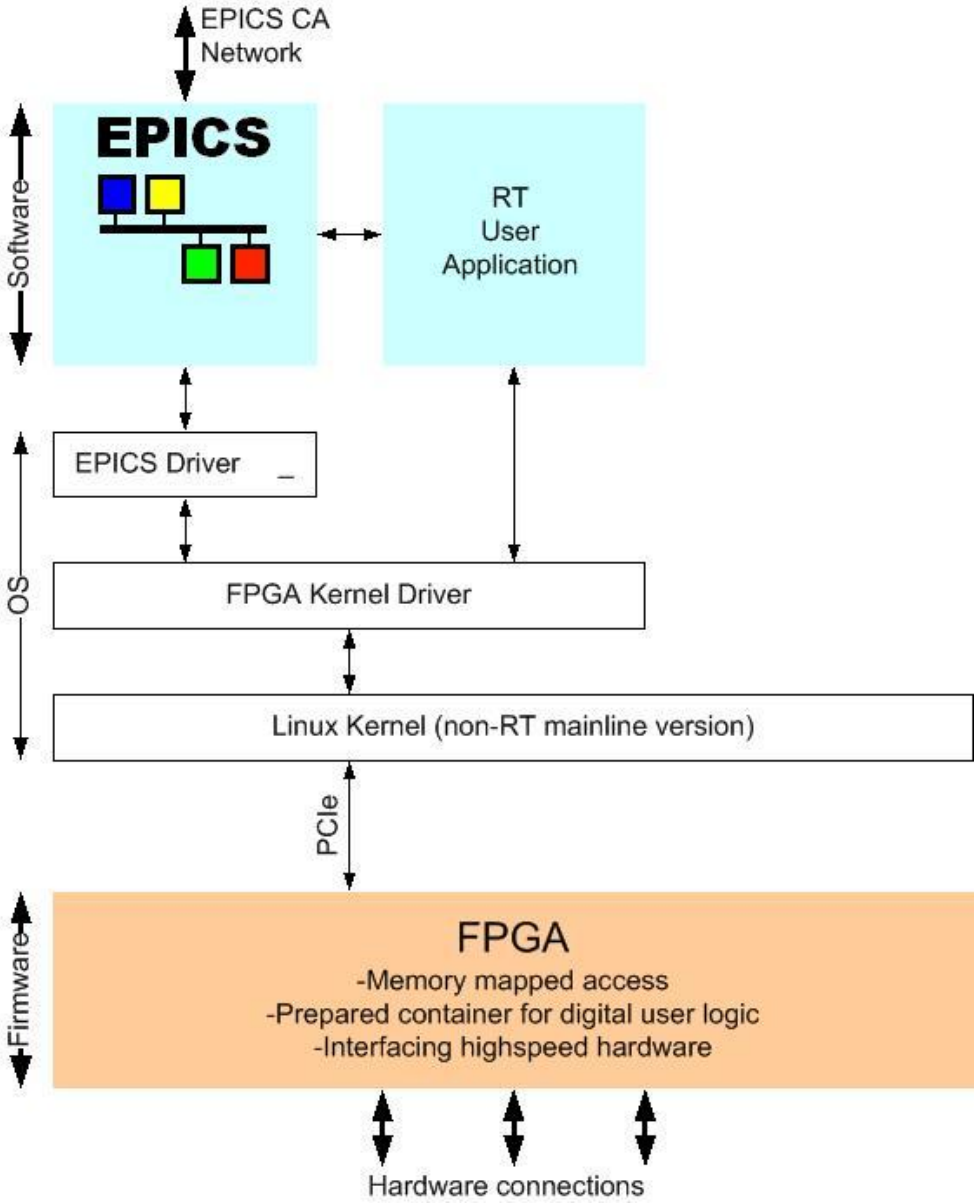
Soft- and firmware

Software:

- Selected development environment ELDK (Embedded Linux Development Kit)
- First successful test with own built mainline Linux kernel
- FPGA kernel driver was supplied by company IOxOS
- EPICS driver has been created
- EPICS version 3.14.12 tested on target platform

Firmware:

- Basic Firmware setup for interface to commercially available ADC/DAC FMC mezzanines exists
- Generic firmware implemented and ready for testing



RF front end design

LO Generation:

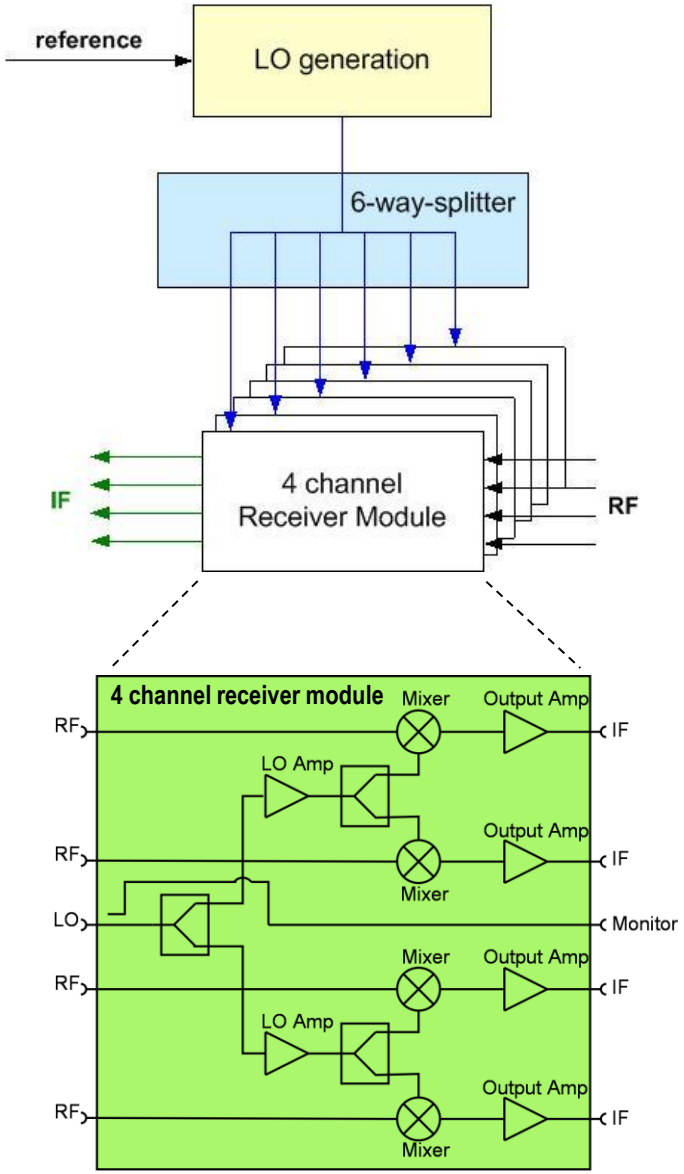
- Choice of conventional design with dividers and filters
- Same concept for 3GHz already tested at PSI

Receiver design:

- 6 modules per LLRF system
- Each module has four RF channels, this results in a maximum of 24 RF channels per LLRF System
- PCB Layout finished, review is ongoing now

Vector modulator:

- Based on the TRF370417 chip from Texas Instruments
- Two pin switches for interlock applications integrated
- Two DACs integrated to adjust offsets of the vector modulator
- PCB prototype ready for production



Summery and Outlook

Design LLRF (milestone 31)

Milestone already reached!

First LLRF prototype (milestone 32)

Digital LLRF hardware:

- Finish verification of digital processing board (IFC1210) prototype features
- Finish PCB revision and start small series of digital processing board (IFC1210)
- Finish verification measurements of ADC and DAC cards

Software:

- Implement readout and write-down records for basic LLRF firmware
- Start with real-time Linux kernel and real-time user application

Firmware:

- Specify and implement basic LLRF system firmware (memory map and signal processing)

Receiver and vector modulator:

- Manufacturing of prototype modules
- Characterisation and measurements of the prototypes

LO Generation:

- Start of schematic and PCB design
- Manufacturing of first prototype

Thank you - Questions