

# TIARA WP8 Status

M. Biagini, INFN-LNF, for WP8

TIARA Mid-Term Meeting

Madrid, June 13<sup>th</sup> 2012



**TIARA**

ACCELERATING KNOWLEDGE AND INNOVATION



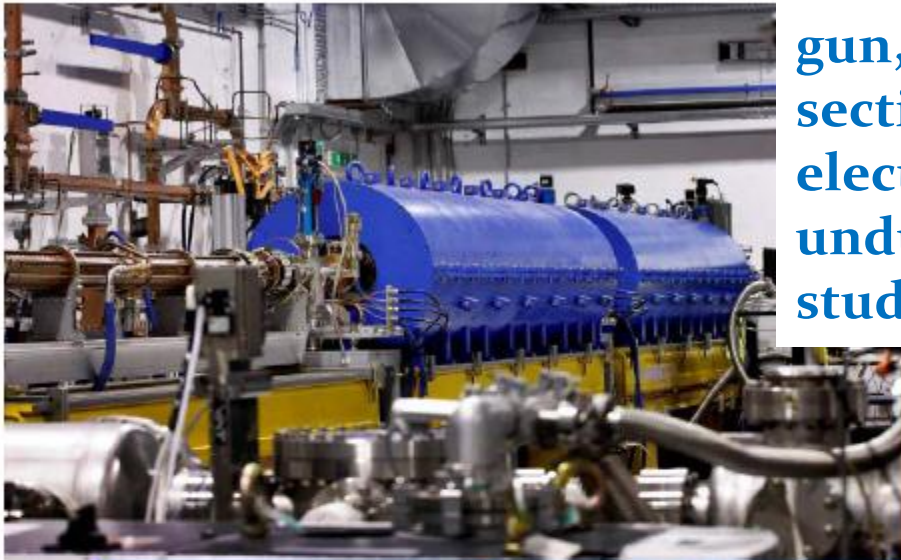
# WP8 – HGA

WP coordinator: M. Biagini (INFN). WP deputy: A. Gallo (INFN)

- Goal: energy upgrade of the Frascati SPARC test-facility linac by designing, constructing and commissioning 2 C-band ( $f=5712$  MHz) TW high-gradient accelerating structures
- Partners: INFN, PSI, University of Rome “La Sapienza” as sub-contractor
- Duration: 3 years
- Work Breakdown:
  - WP8.1 : Study of SPARC upgrade in Energy (INFN)
  - WP8.2 : RF Low level Electronics for SPARC (PSI)
  - WP8.3 : Construction and test of 2 C-band sections (INFN)

# SPARC @ LNF

**SPARC:**  
Photoinjector with  
low emittance RF  
gun, 3 S-band  
sections for 170 MeV  
electrons,  
undulators for FEL  
studies



**RF GUN:**  
-2.856 GHz  
-1.6 cell

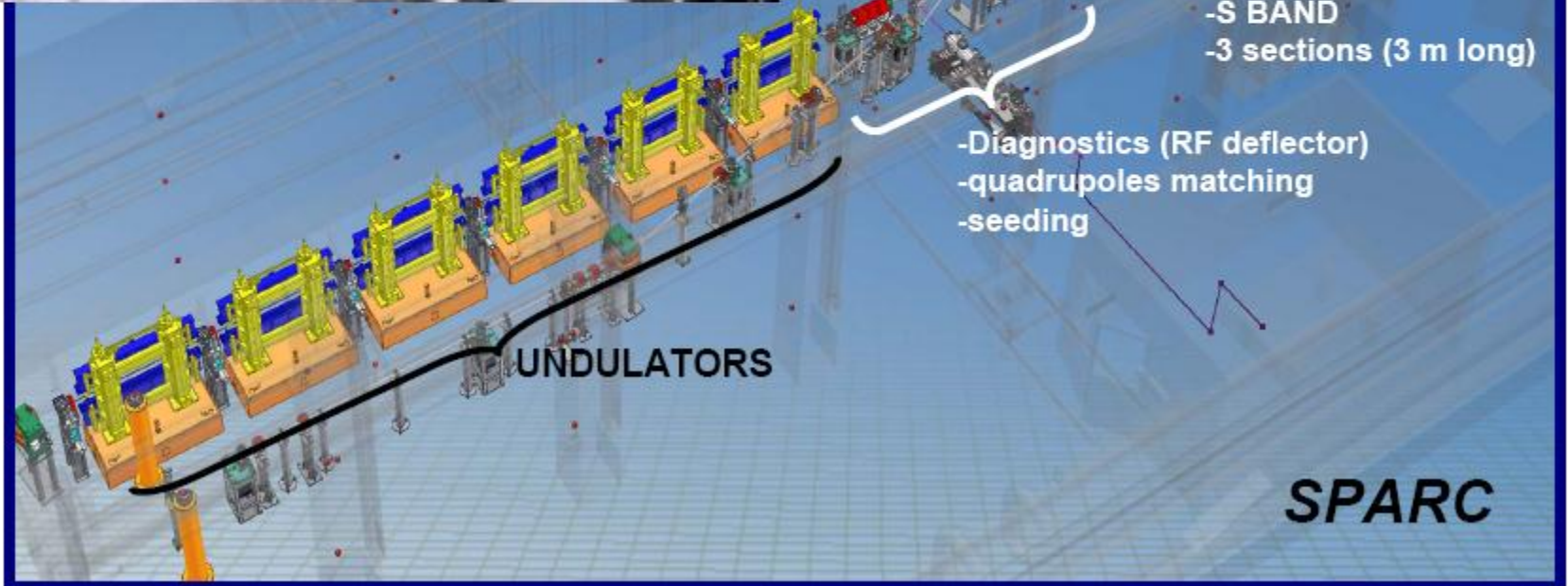


**LINAC:**  
-S BAND  
-3 sections (3 m long)

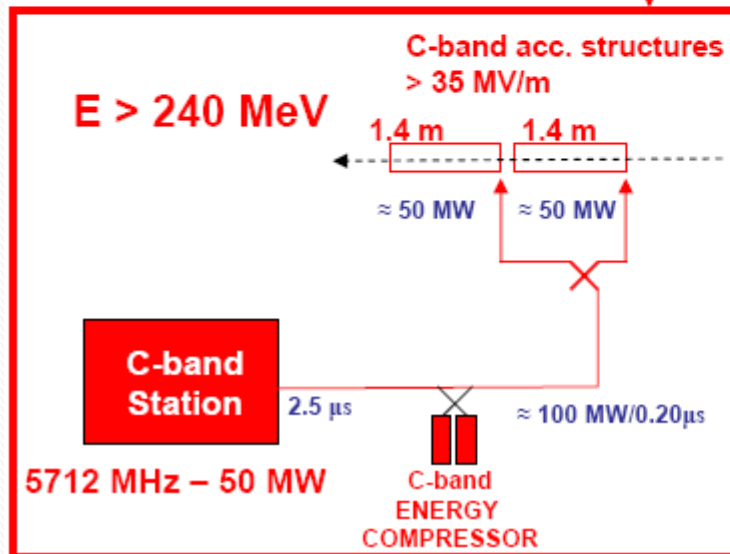
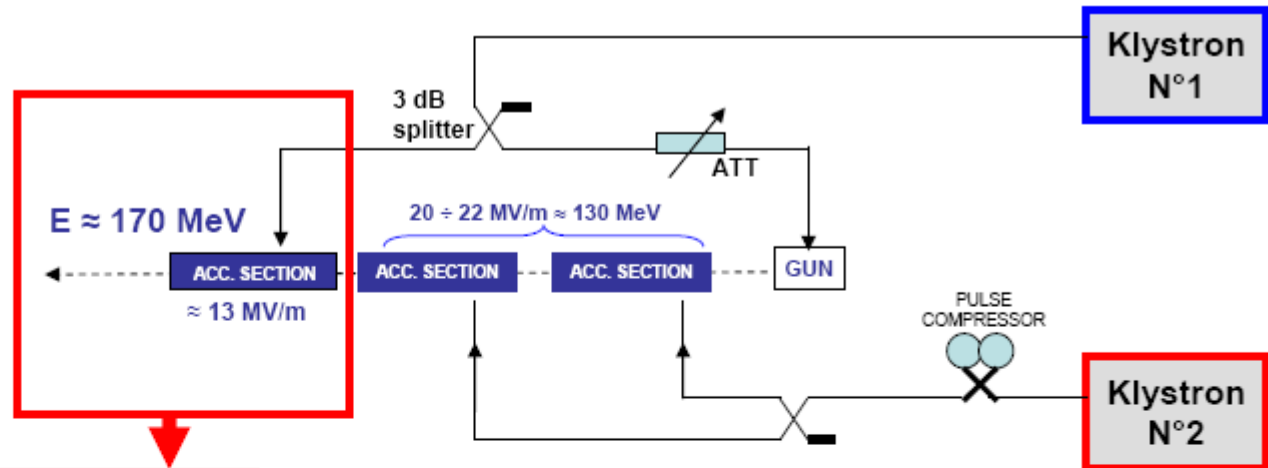
-Diagnostics (RF deflector)  
-quadrupoles matching  
-seeding

**UNDULATORS**

**SPARC**



# SPARC upgrade (hybrid S-C band)

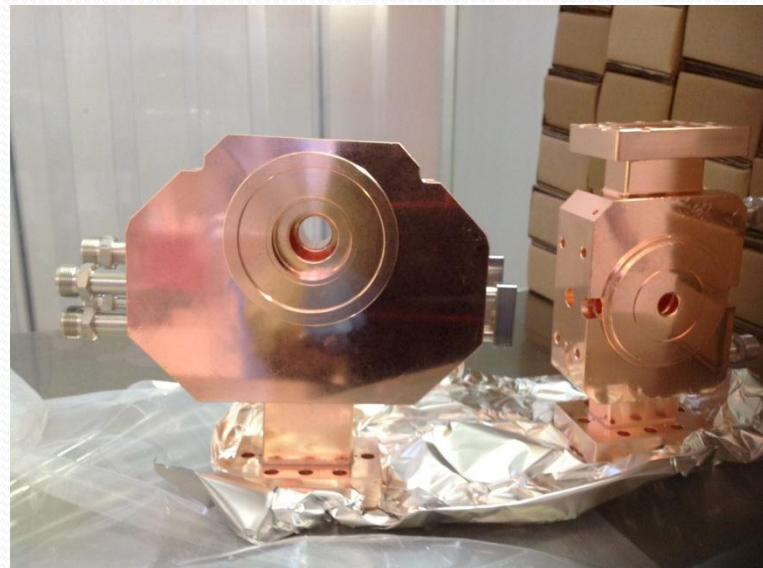
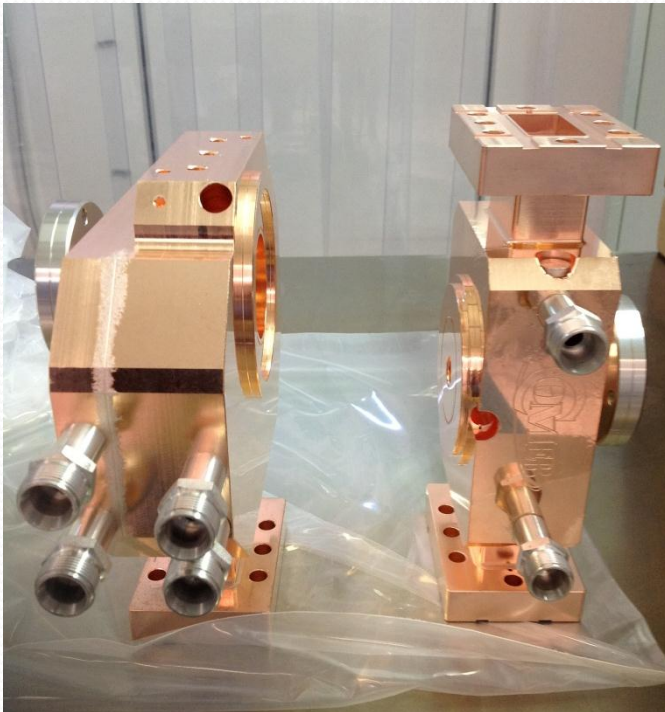


The new C-band system consists mainly of:

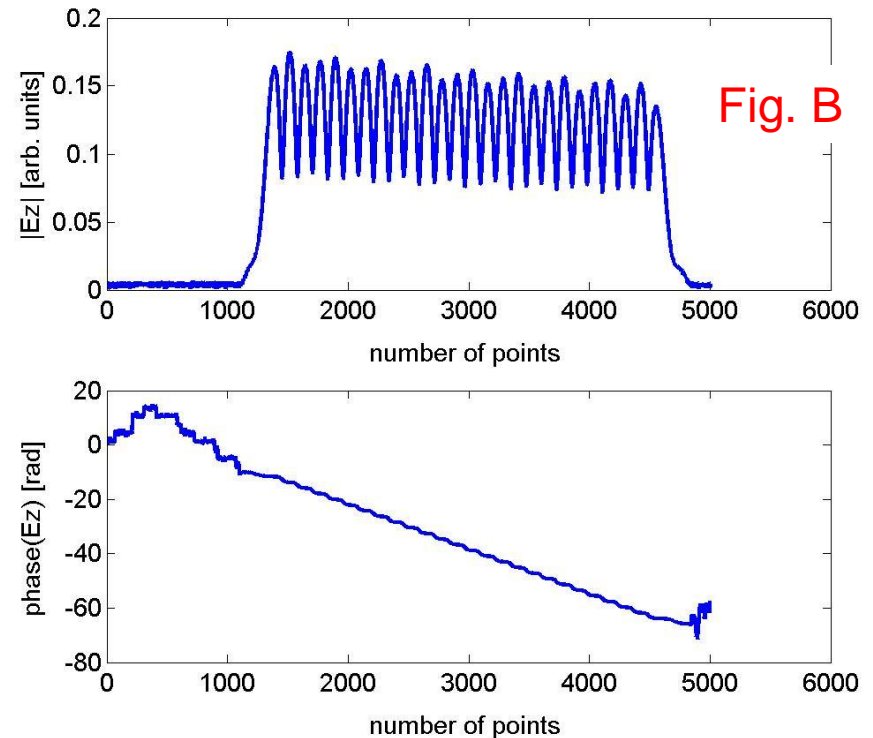
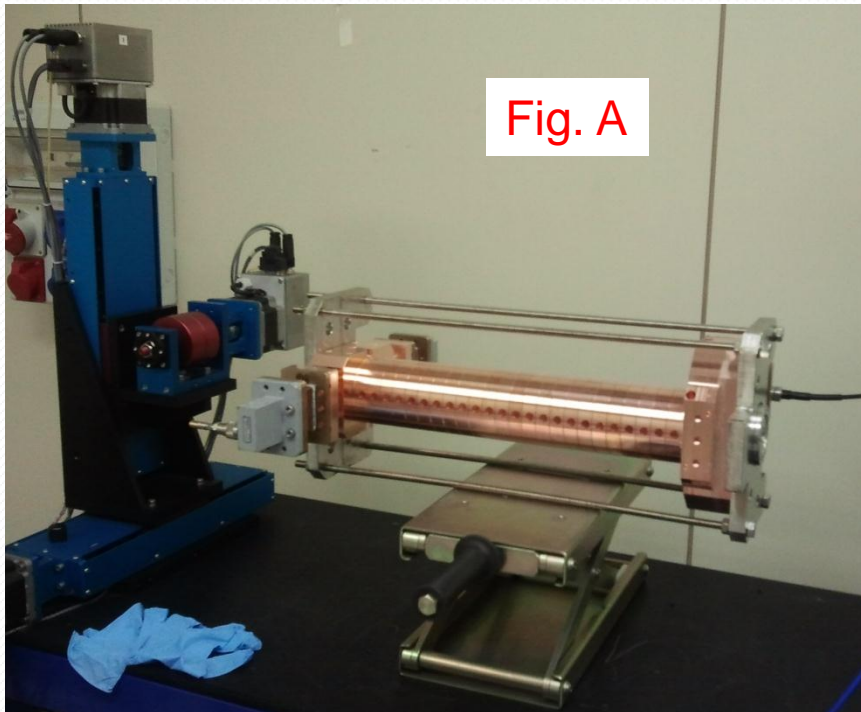
- ⇒ 2 accelerating sections (1.4 m long) ← **TIARA**
- ⇒ 1 C-band klystron (50 MW), by Toshiba Ltd (JP)
- ⇒ 1 Pulsed HV modulator supplied by ScandiNova (S)
- ⇒ WR187 waveguide system
- ⇒ 400 W solid state driver supplied by MitecTelecom (CDN)
- ⇒ SLED

## Task 8.1, 8.3 – C-band sections at LNF: status of design and fabrication

- 1) The cells of the **first accelerating structure** prototype have been fabricated
- 2) The **input/output couplers** of the **first accelerating structure** prototype have been fabricated and the brazing of the input and output couplers with vacuum stainless steel flanges has been done



- 3) Preliminary RF measurements of pre-assembled structures (few cells + input and output couplers) have been done (see Fig. A). They are used to characterize the cells and monitor the quality of the input and output coupler realization. An example of measured accelerating field in magnitude and phase is given in Fig. B
- 4) The cells of the **second accelerating structure** are still under fabrication
- 5) The **input/output couplers of the second accelerating structure** are still under fabrication

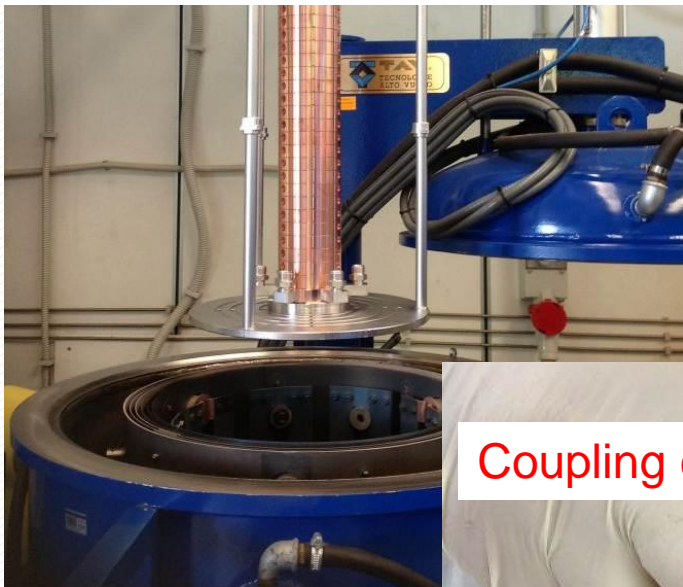


# Task 8.3 – C-band sections fabrication

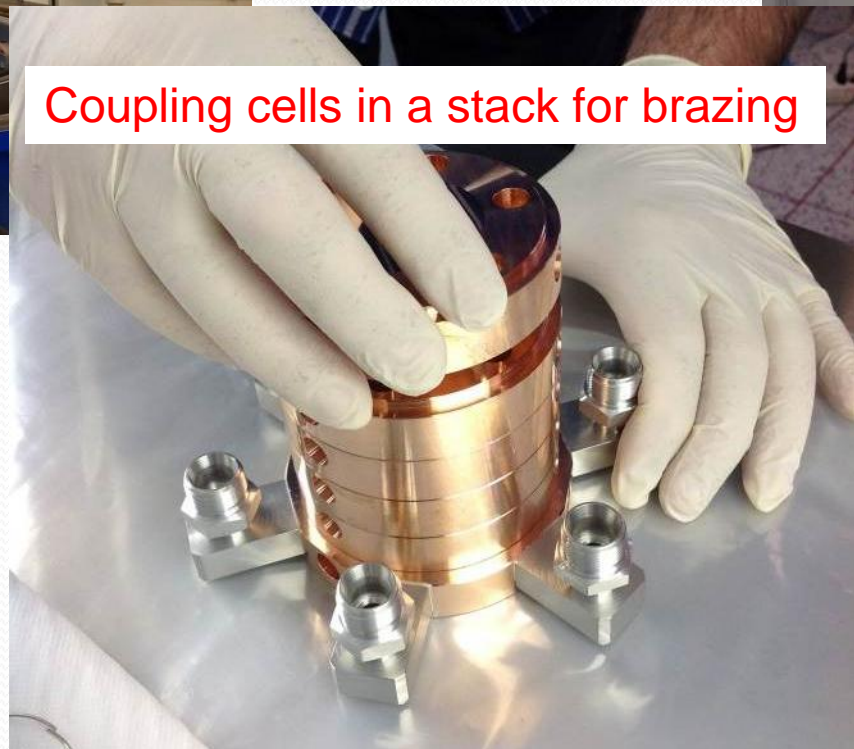




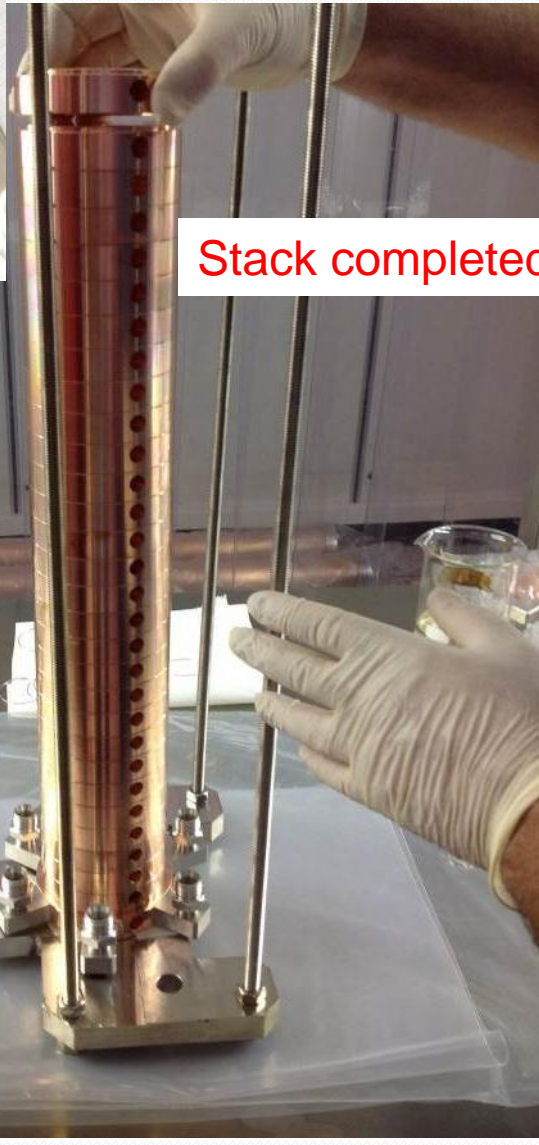
Insert cells into the vacuum oven



Insert rings for brazing



Coupling cells in a stack for brazing



Stack completed

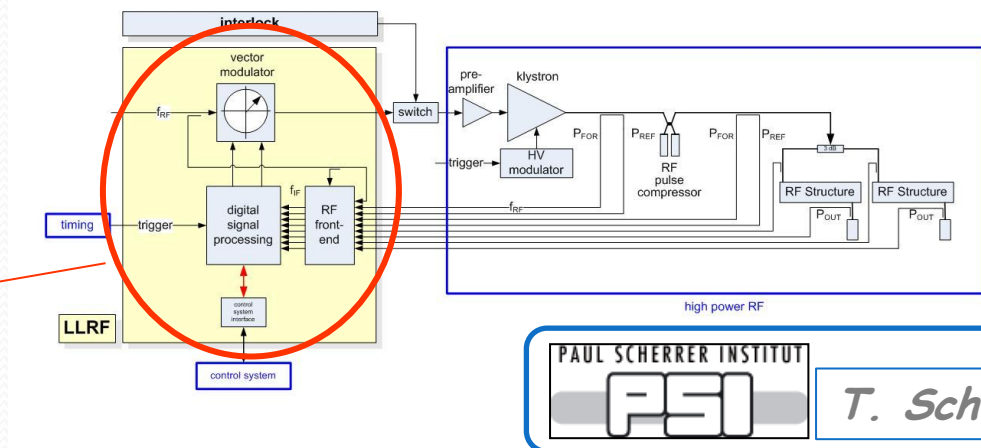


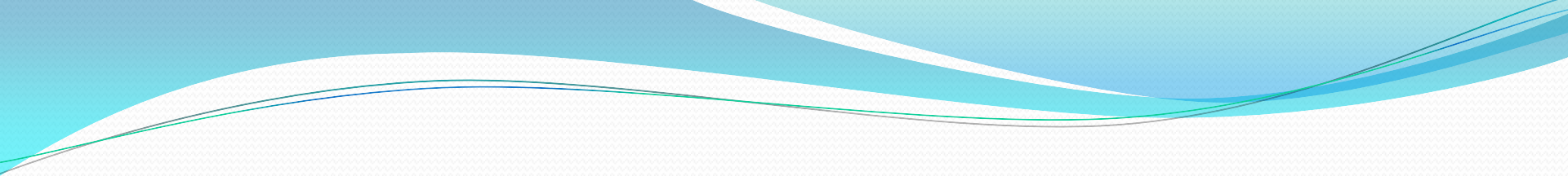
# Task 8.2 - RF Low Level Electronics for SPARC

- Task: design a flexible and high performance Low Level RF system for 5712 MHz (C-band)
- The control of high gradient C-band accelerating structures will be achieved by a digital low level RF (LLRF) system where all RF signals are down-converted to intermediate frequencies which are then digitized and processed on powerful digital processing platforms. The drive signal is finally up-converted to control the RF high power chain
- This system is studied and realized at PSI and will be tested at SPARC

## System layout

*scope of the WP 8.2*





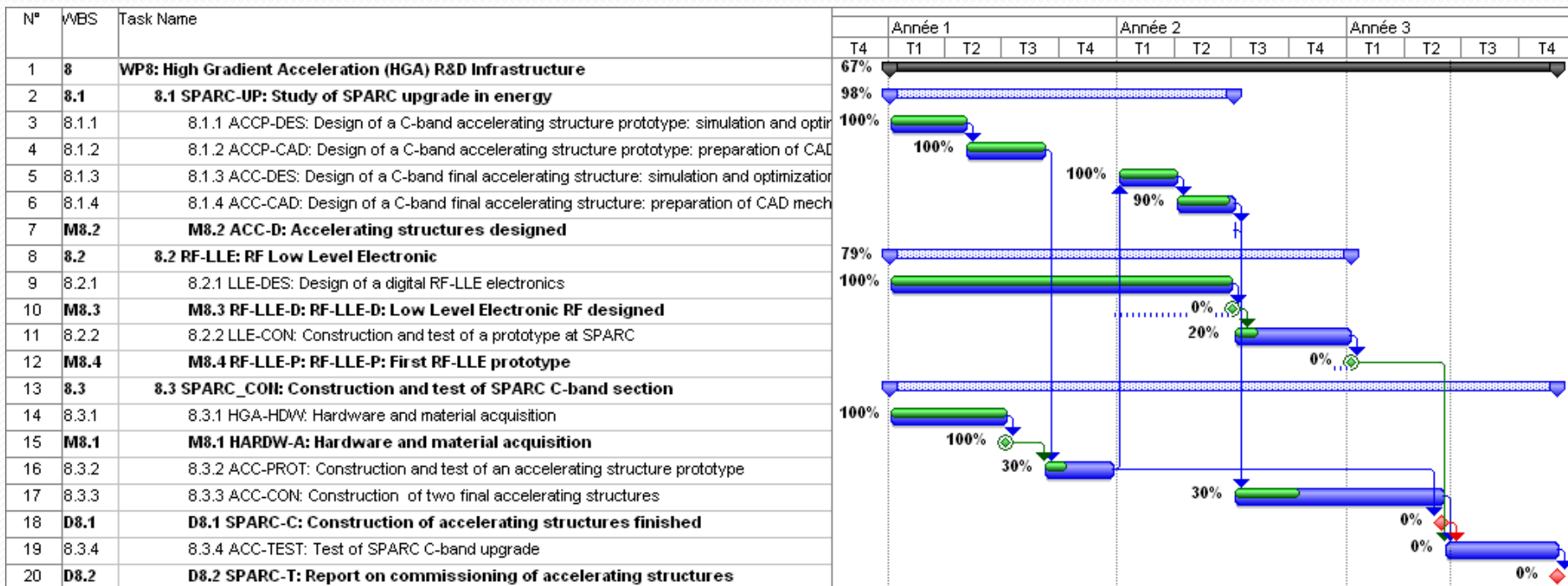
This topic will be discussed  
by Manuel Broennimann (PSI)  
in the second half of my time slot

## Task 8.2 - LLRF at PSI → Milestone delayed

- Request from PSI to move Milestone 32 (RF-LLE-P) from Dec. 2012 to June 2013 (**see letter from PSI Task leader T. Schilcher**)
- Due to the tight specifications of the system the design work took longer than predicted, and an RF engineer who should have supported the senior RF engineer in the design has left PSI. As a consequence, a replacement needs to be hired and requires about 6 months to resume the work
- In the meanwhile, the design tasks of the RF front-end modules can only be processed sequentially instead of parallel as originally foreseen
- PSI is confident to deliver a C-band LLRF system which meets the specifications by the latest **June 2013**
- This delay (if kept to 6 months) means that the LLRF system will not be tested before its installation on SPARC. **This may not represent a real problem, but the delay should not exceed the 6 months**
- Discussion on this topic will be carried out during the WP8 parallel session today

# Milestones and time schedule

Num	Short name	Description	Month	Status*
MS29	HARDW-A	Purchase of crucial hardware components	6	Achieved
MS30	ACC-D	Design of accelerator structures	18	Done at 90%
MS31	RF-LLE-D	Design LLRF	18	Achieved
MS32	RF-LLE-P	First LLRF prototype	24	In progress (to be delayed by 6 months)



# Conclusions

- Tasks 8.1 and 8.3 are proceeding on schedule, procurement of hardware **accomplished**, design of cavities **accomplished**, assembling and brazing of cells **in progress**
- Task 8.2, design of LLRF system **done**
- Milestone 32 (**LLRF prototype ready**, PSI): a **6 month delay** will allow for delivering the LLRF prototype with all specifications met