



AGH UNIVERSITY OF SCIENCE
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Towards front-end for LHCb upgrade tracker

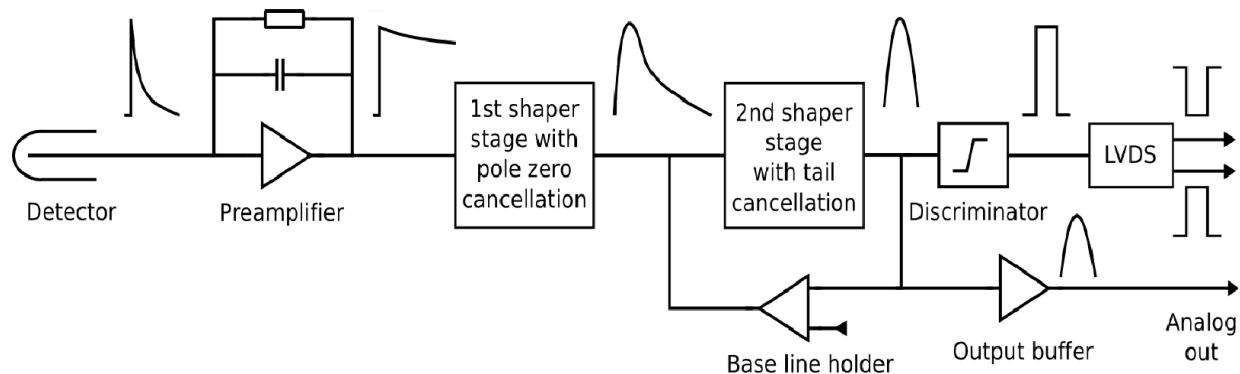
Some considerations

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Workshop on Common ASIC for the LHCb Upgrade
AGH - UST, Krakow, 05 July 2012

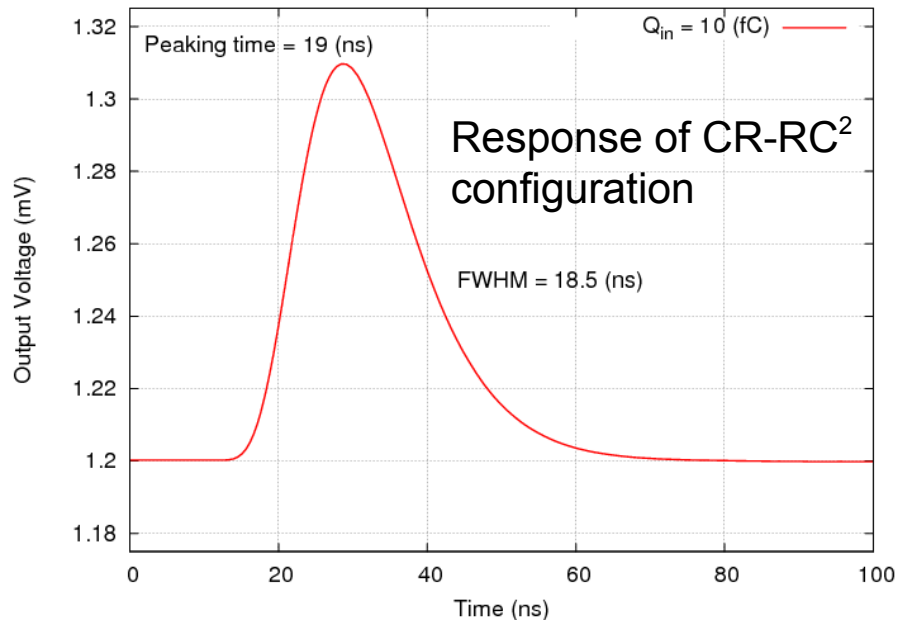
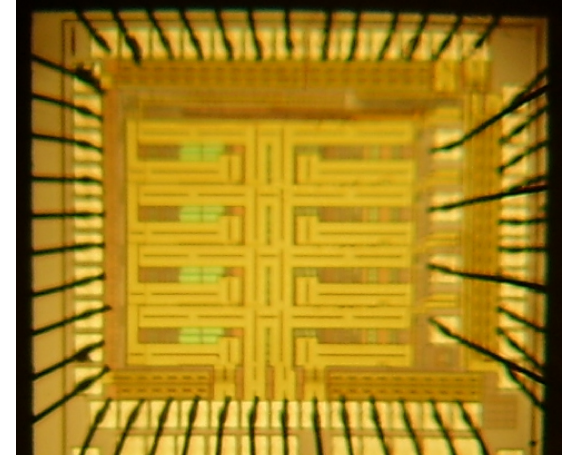
PANDA STT Front-End Architecture



- Preamplifier with variable gain and time constant
- CR-RC² shaper with variable T_{peak} (default $\sim 20\text{ns}$ for delta)
- Tail cancellation with two variable time constants
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time measurements
- Fast LVDS output
- Buffered analog output

PANDA STT ASIC – First Prototype

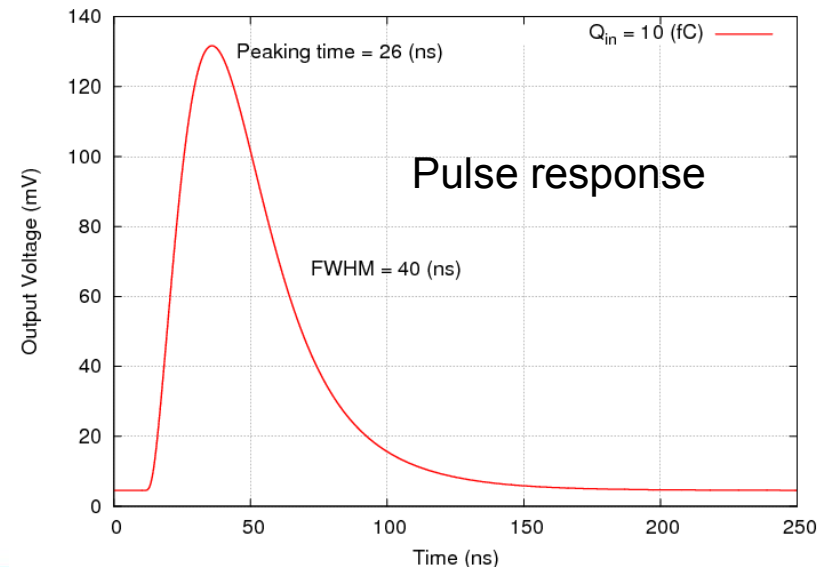
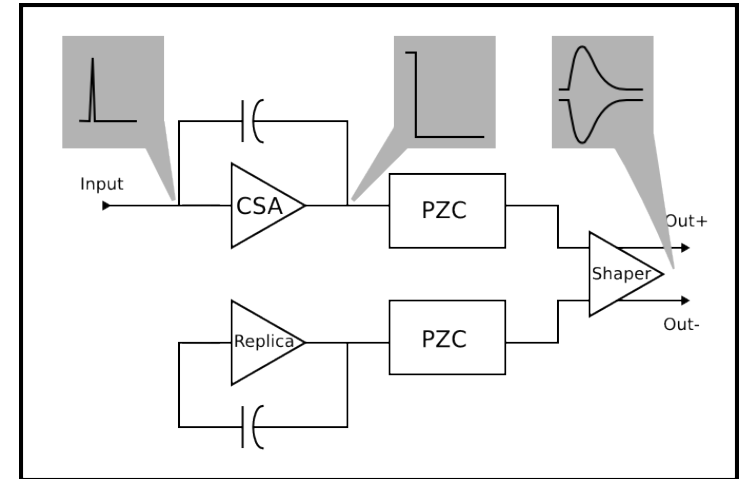
- ASIC designed and fabricated in AMS 0.35 μ m technology
- Four channels implemented
- ~ 15.5 mW/channel plus LVDS (~ 12 mW)
- Channel size 200 μ m x 1130 μ m
- Gain in 2 – 20 mV/fC range
- ENC < 700e⁻ for highest gain (25pF Cd)
- Time walk < 8ns; Jitter < 0.2ns



LumiCal FEE in 130nm, in progress...

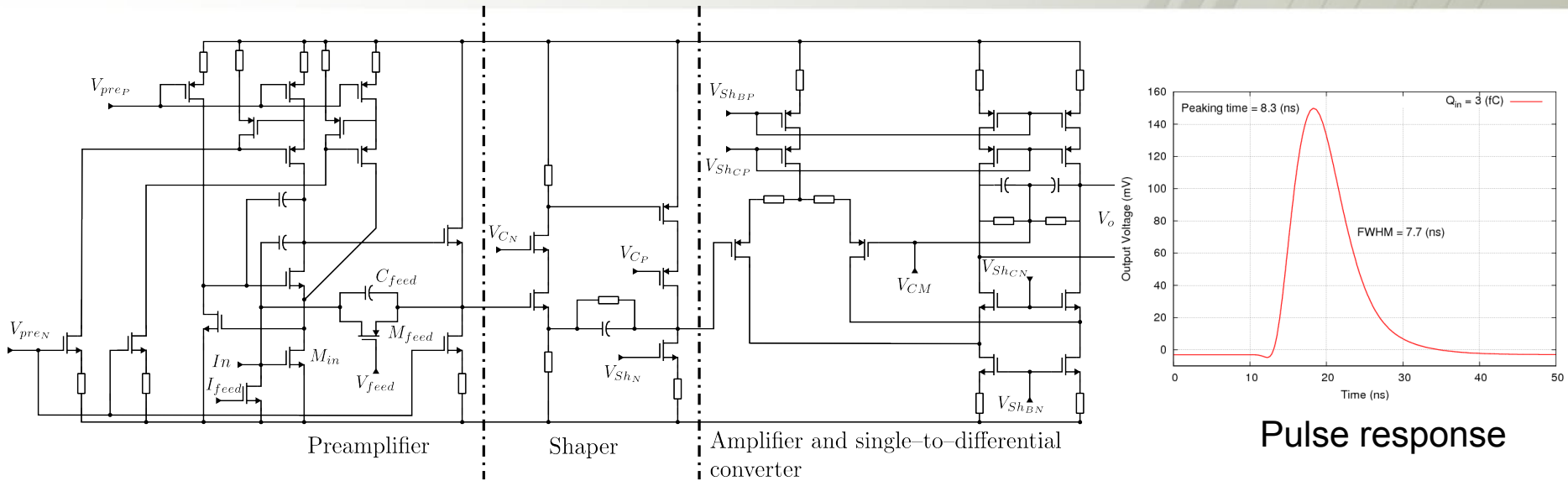
Specifications, still under discussions:

- Charge Sensitive Preamplifier with PZC
- Fully differential CR-RC Shaper
- Variable gain: $0.15 \text{ mV}/_{\text{fC}} - 15 \text{ mV}/_{\text{fC}}$
(Two modes: calibration – high gain and physics – low gain)
- Variable peaking time: 25 – 100 ns
- Cdet $\sim 5 - 30 \text{ pF}$
- Noise $< 0.4 \text{ fC}$ (SNR ~ 10 for MIP)
- Power cons. $\sim 2\text{mW}/\text{channel}$



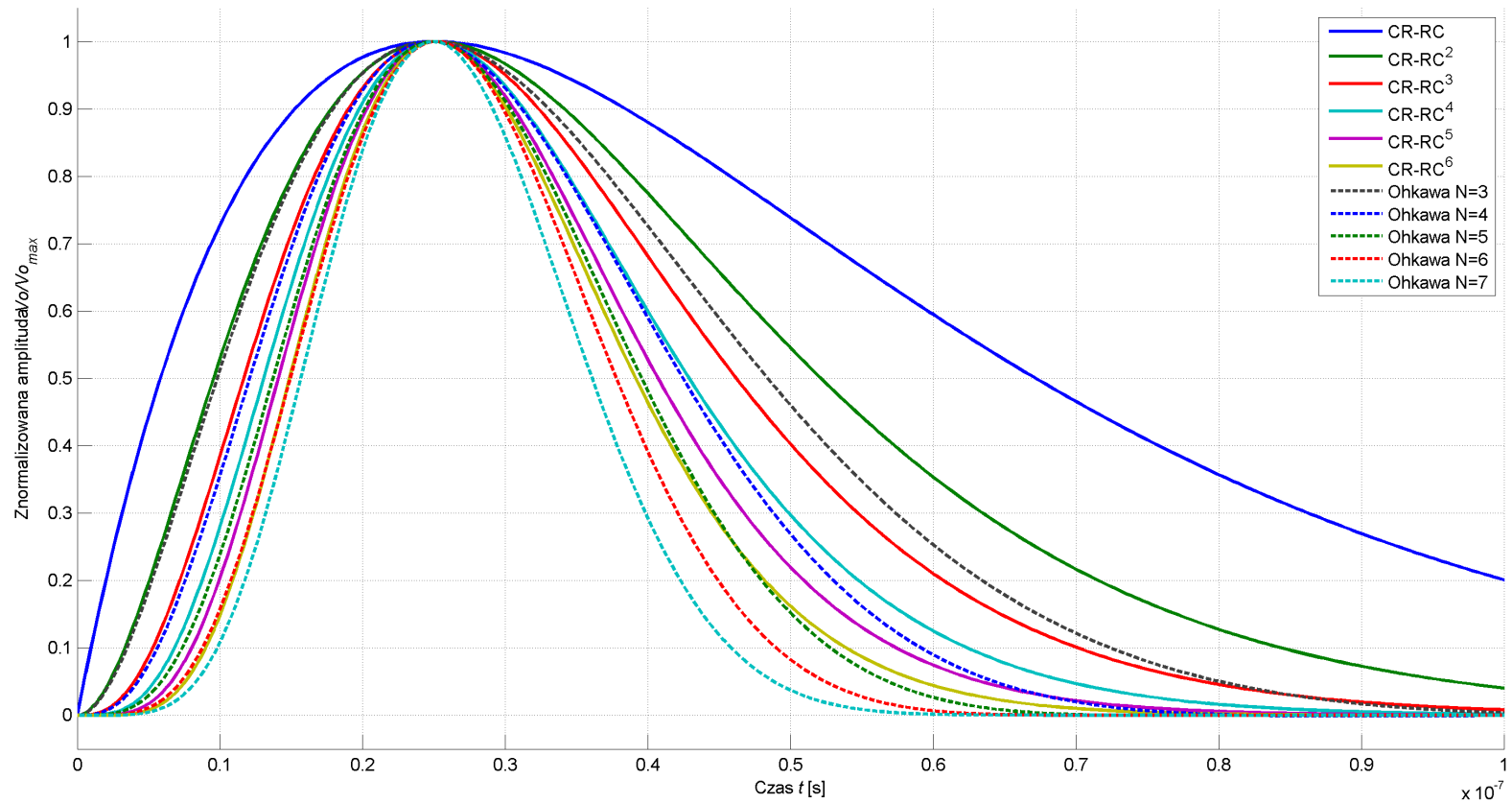
Front-End for BCM, in progress...

D. Przyborowski under J. Kaplon supervision



- IBM 130 nm Technology
- Fast transimpedance preamplifier with CR-RC² shaping
- HV enabled design – 2.5V supply with thin oxide devices
- 50mV/fC gain
- ~8 ns of T_{peak} and FWHM
- < 800e⁻ for 5pF C_{in}
- Power cons. ~1.3 mW/Ch
- Fast return to baseline after high overdrive signal (~200ns for 1pC input)

Pulse shaping - theory



Few conclusions for LHCb upgrade front-end

- For fast return to baseline higher order and non-standard pseudo-gaussian shaping is advocated, or shorter peaking time...
- Differential output requires fully differential amplifier driving capacitive ADC inputs (each one $\sim 0.5\text{pF}$),
- Both mentioned issues together with rather large sensor capacitance (5-30pF), will affect front-end power consumption.