
AGH University of Science and Technology

# Development of 6-bit Successive Approximation ADC for LHCb tracker upgrade

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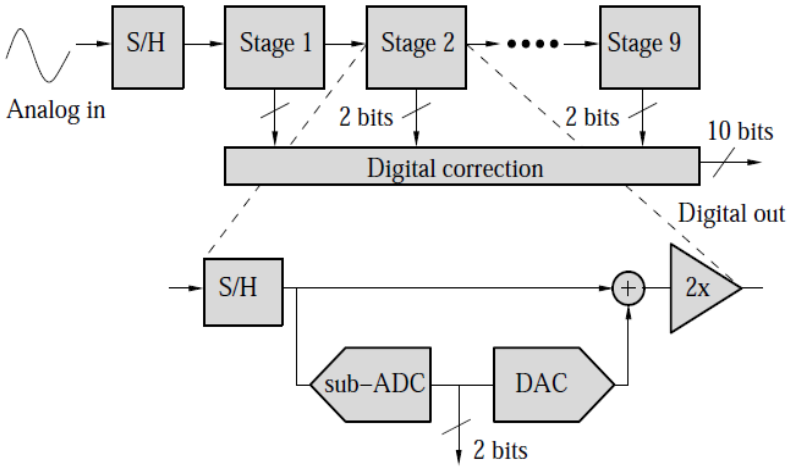
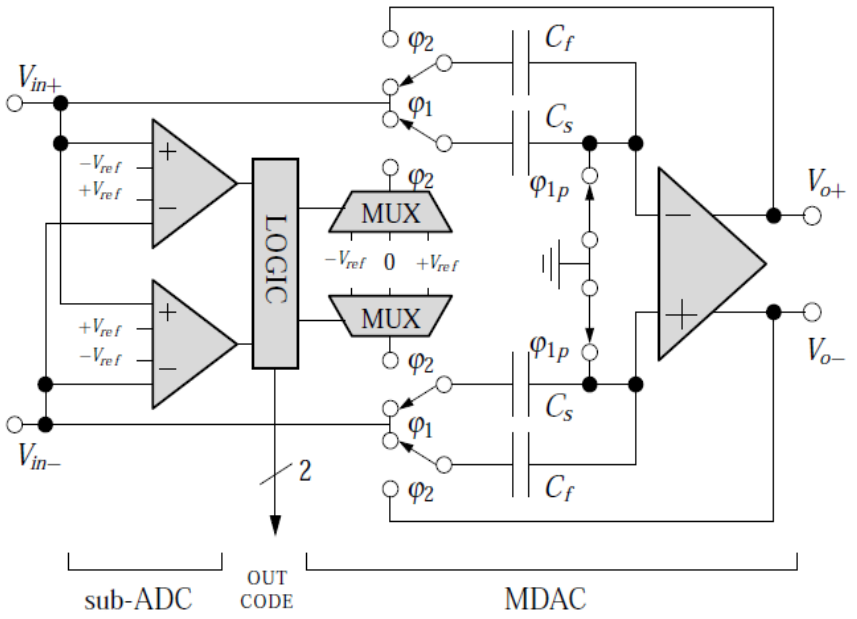
# Agenda

- Previous experience with pipeline ADC
- Successive approximation ADC
- 10-bit ADC prototypes in 130nm IBM
- 6-bit ADC design in 130nm IBM
- Simulation results for 6-bit ADC
- 8-channels 6-bit ADC prototype core

# 10-bit Pipeline ADC in 0.35um AMS




- 10-bit pipeline ADC with 1.5 bit per stage architecture
- S/H stage + 9 pipeline stages



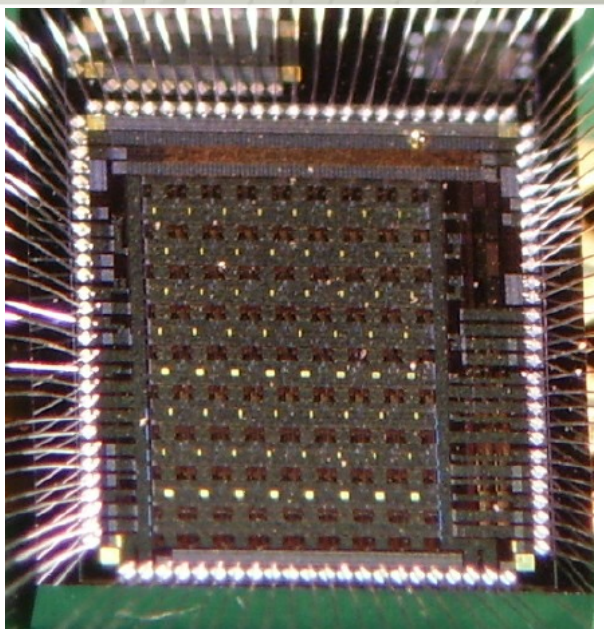

- Fully differential design
- Maximum sapling rate **25MS/s**
- Power pulsing

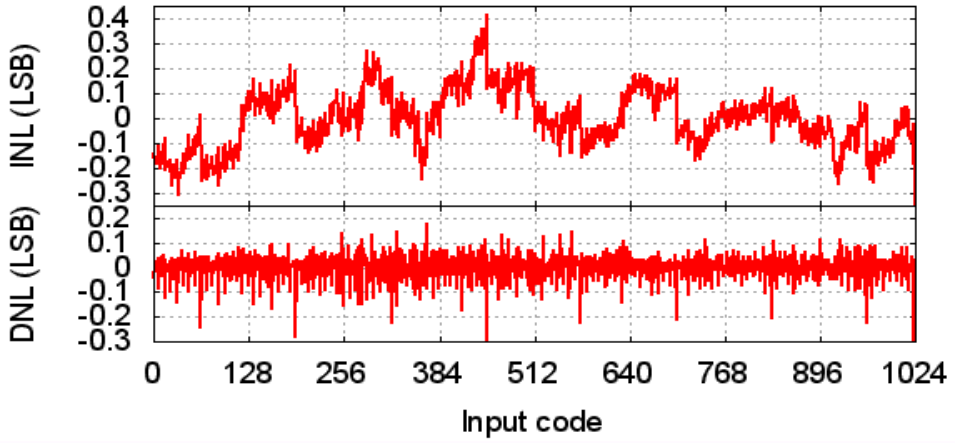
*M. Idzik, K. Swientek,T. Fiutowski, Sz. Kulis, P. Ambalathankandy "A power scalable 10-bit pipeline ADC for Luminosity Detector at ILC", JINST 6 P01004, 2011*

# 10-bit Pipeline ADC in 0.35um AMS

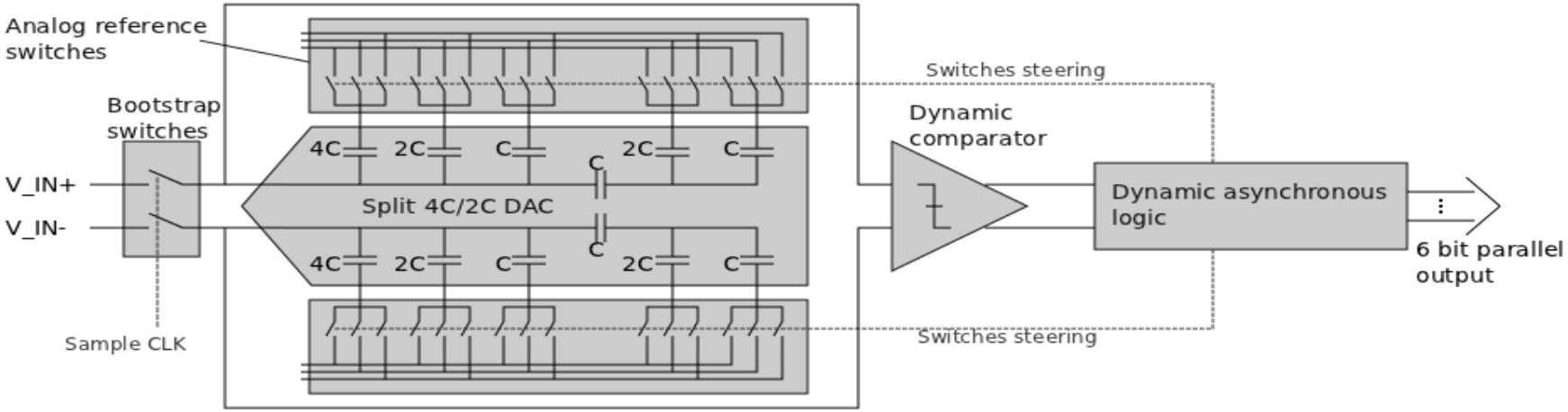
- Designed and fabricated in 0.35um AMS
- Single channel area **0.87 mm²**
- 8-channel ASIC – **2.6mm x 3.2mm**

- Sampling rate **1kS/s-25MS/s**
- Scalable power **~0.8mW/MS/s**
- Sinad ≈ **60dB**
- ENOB = **9.7 bit**
- INL < **0.42 LSB**
- DNL < **0.42 LSB**





# SAR (successive approximation register) architecture




- Power and area-efficient architecture – the same circuitry is used n-times (for n-bit ADC) to approximate the input voltage
- Asynchronous logic – no fast clock needed for bit cycling, only sampling signal needed
- Only one comparator per channel – small layout area
- Split DAC architecture – lower area and power consumption
- Not for ultra-high sampling rate – next conversion cannot be started before the current one is completed

# 10-bit SAR ADC in 130nm IBM

Two ADCs designed in 130nm IBM

- Both: channel area ≈ 0.09 $mm^2$ (146um x 600um)

- First prototype submitted in February 2012
- Simulated ENOB ≈ **9.5 bits**
- Maximum sampling rate above **50 MS/s**
- Power consumption ≈ **1.4mW @ 40 MS/s**
- Simulated FOM ≈ **50 fJ/conv.bit**

- Second prototype submitted in May 2012
- Simulated ENOB improved to **9.8 bits**
- Maximum sampling rate above **50 MS/s**
- Power consumption ≈ **1.1mW @ 40 MS/s**
- Simulated FOM ≈ **35 fJ/conv.bit**

First prototypes from February submission already arrived. Tests will start soon...

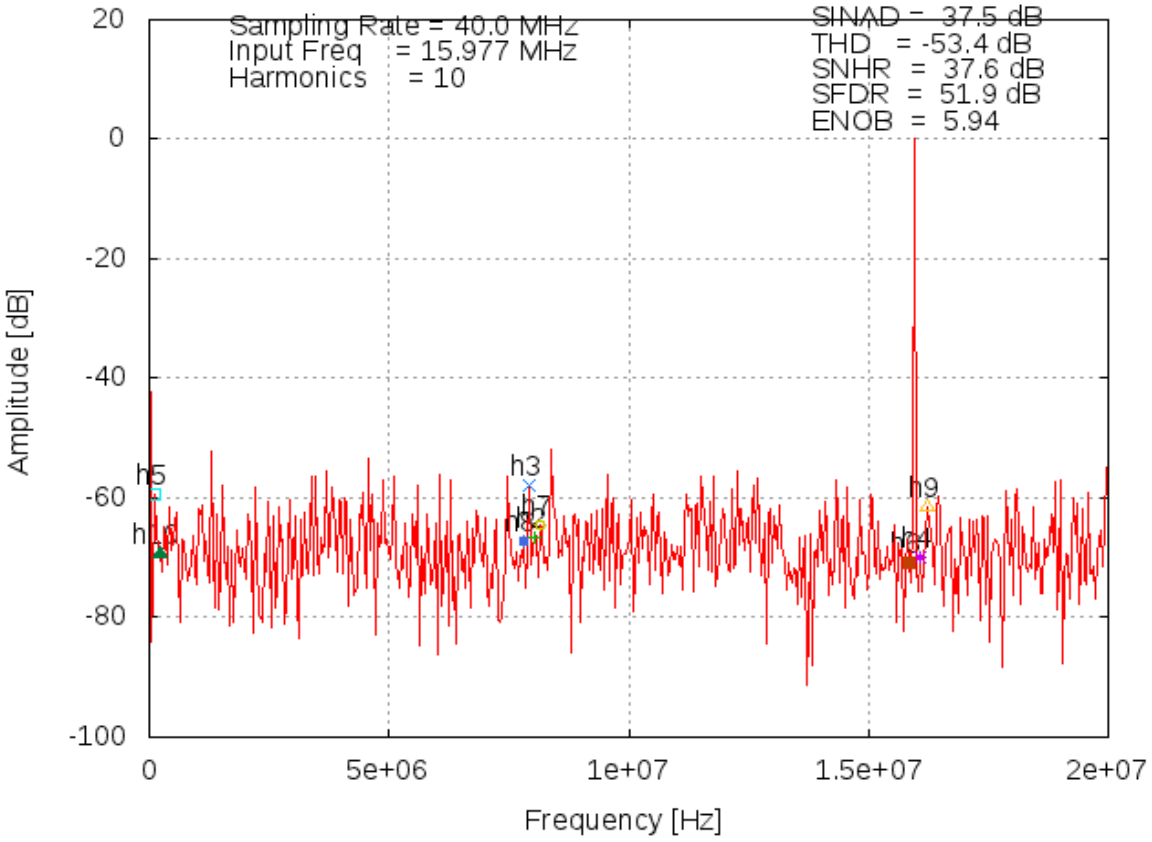
# 6-bit SAR ADC in 130nm IBM

Based on experience with 10-bit ADC design a 6-bit SAR ADC was developed for LHCb upgrade in 130nm IBM technology

- Design guidelines
  - Channel pitch = **40um**
  - **6 bit** resolution with simulated ENOB > **5.8 bits**
  - Maximum sampling rate > **50 MS/s**, nominal sampling rate = **40 MS/s**
  - Power pulsing
  - Power consumption < **0.5 mW** per channel @40 MS/s

# 6-bit ADC simulation results

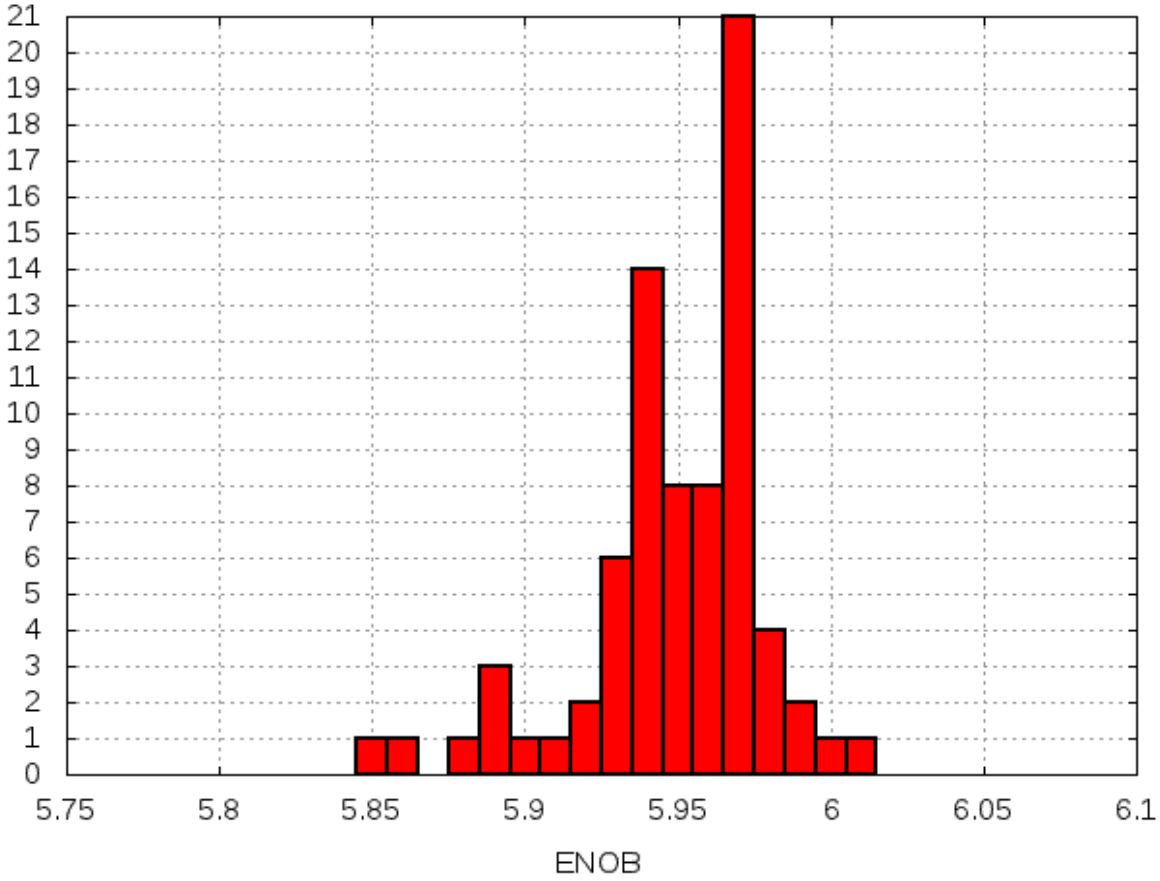
Dynamic parameters obtained from discrete Fourier analyses of n (i.e. 1024) samples of input sine wave.




Post-layout simulation results:

- SINAD ≈ **37.5 dB**
- ENOB ≈ **5.94 bits**
- Maximum sapling rate **~100MS/s**

# 6-bit ADC simulations results



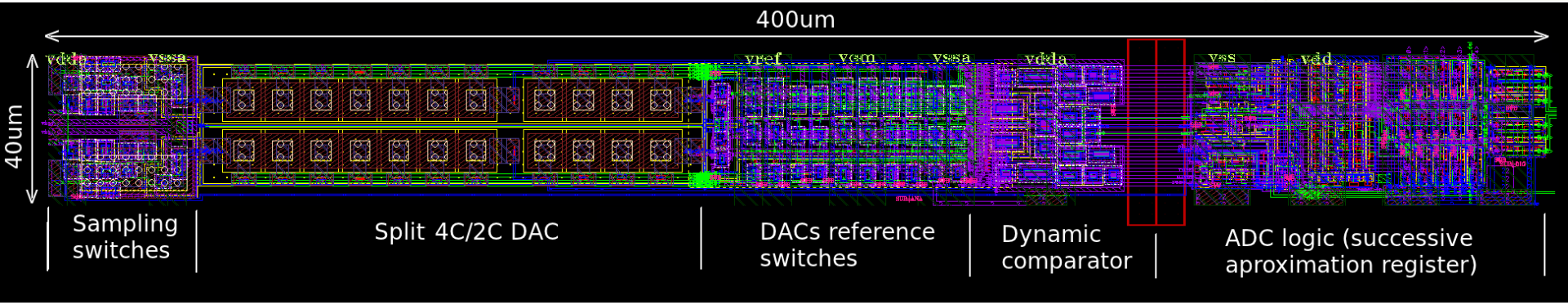

Dynamic simulations performed 100 times for component parameters mismatch obtained from Monte Carlo distribution

Excellent results: ENOB not less than **5.8 bits,** average **5.95 bits**

# 6-bit ADC power consumption

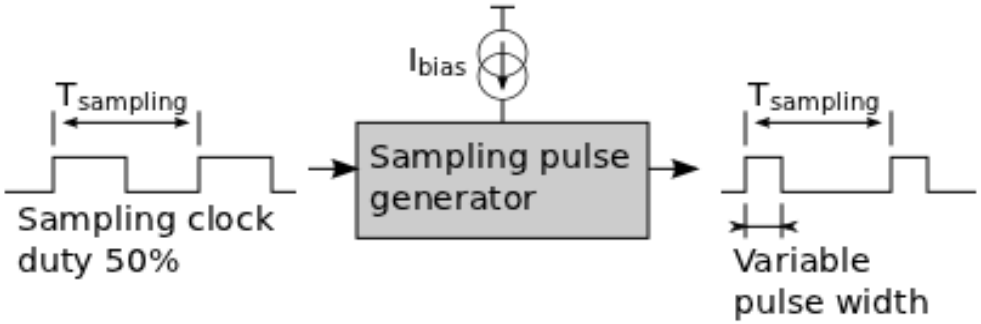
- Power consumption at **40MS/s** sampling rate **<300uW**
- Simulated FOM (Figure of merit) ≈ **120 fJ/conv.bit**
- Design optimized for high resolution and sampling rate, not for lowest power consumption
- About 75% of power needed by digital circuit due to high maximum sampling rate (~100MS/s)
- Asynchronous logic together with dynamic architecture of comparator results in ~0 static power - power pulsing is given for free
- Power consumption linearly scales with sampling frequency

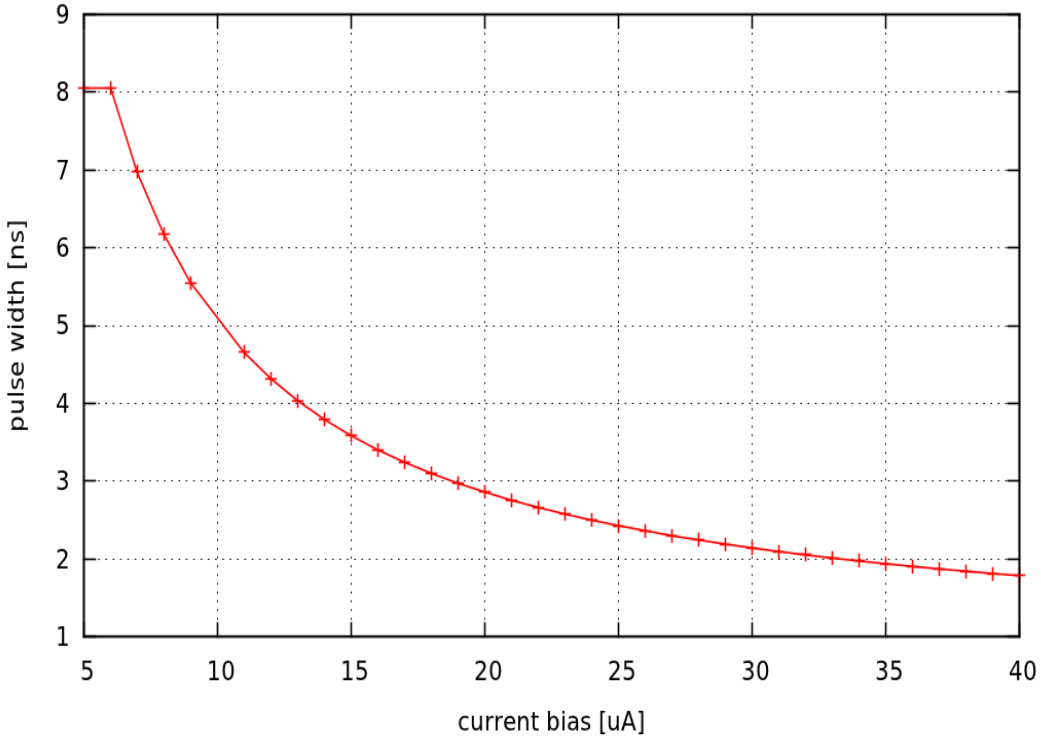
# 6-bit ADC channel layout




- Designed and fabricated in 0.13um IBM technology
- Single channel: **40um x 400um** (area **0.016 mm²**)
- Custom capacitor p-cell layout needed to obtain 40um pitch
- Test ASIC containing 8 channel submitted for fabrication on 5th May 2012

# 6-bit SAR ADC sampling pulse generator



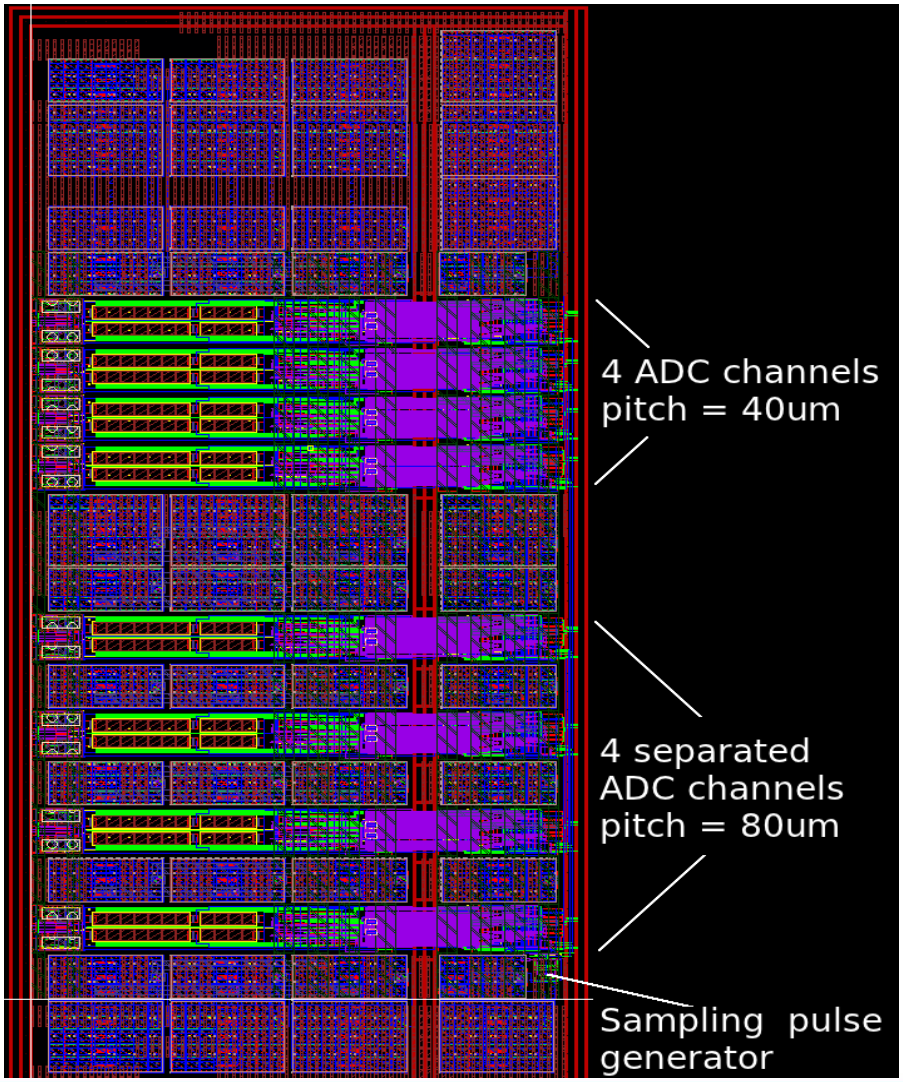




Generator of sampling pulse converts 50% duty external sampling clock into internal variable width pulse (controlled by Ibias)

Simulation results:

- Pulse width in range **2-8ns**
- Bias current in range **5-40uA**

# 8-channel 6-bit SAR ADC prototype core




8-channel 6-bit SAR ADC prototype core was designed

- **4** channels with nominal **40um** pitch
- **4** channels with pitch increased to **80um** to check the effect of layout variation on ADC performance
- Sampling pulse generator driven by external clock
- Sampling pulse distribution tree

**We hope to see the results soon…**