AGH University of Science and Technology

Development of general purpose PLL block, and DLL serializer

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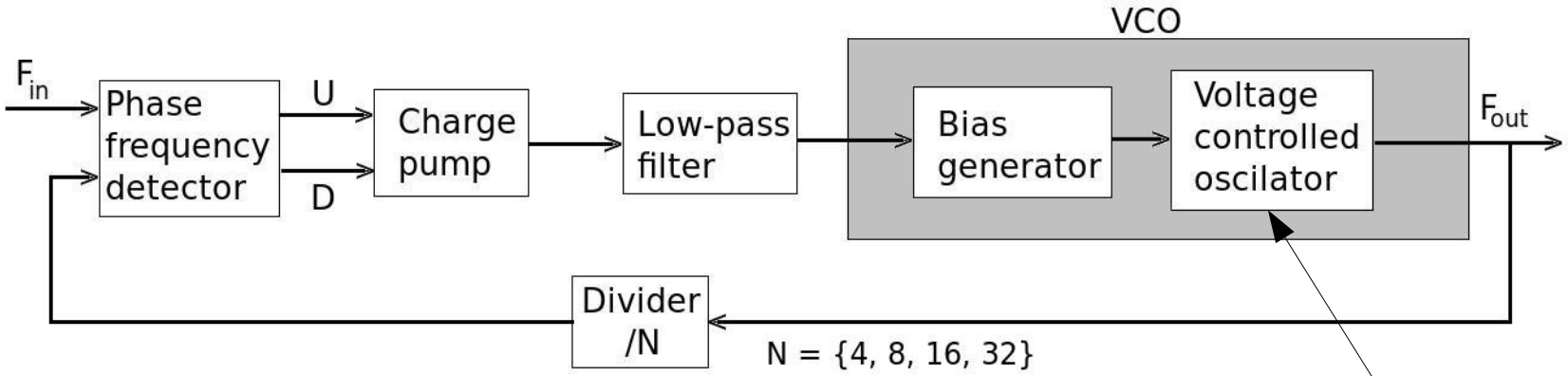
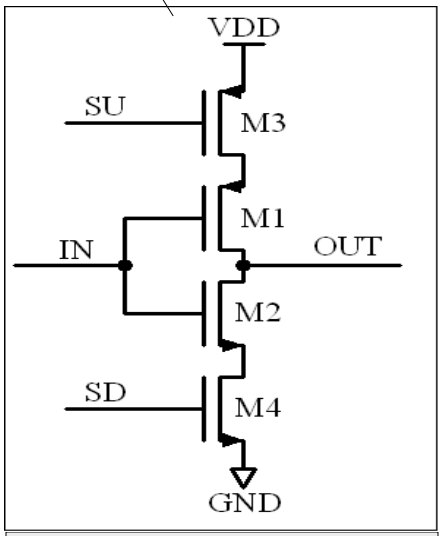
Agenda

- PLL principle
- Experience in AMS 0.35µm technology
  - Transceiver (with first PLL prototype)
  - Improved PLL prototype
  - Present project for neurobiology (PLL and DLL)
- PLL prototypes designed in IBM 0.13um technology
- Serialization in 6-bit ADC for LHCb upgrade

PLL – Phase Locked Loop

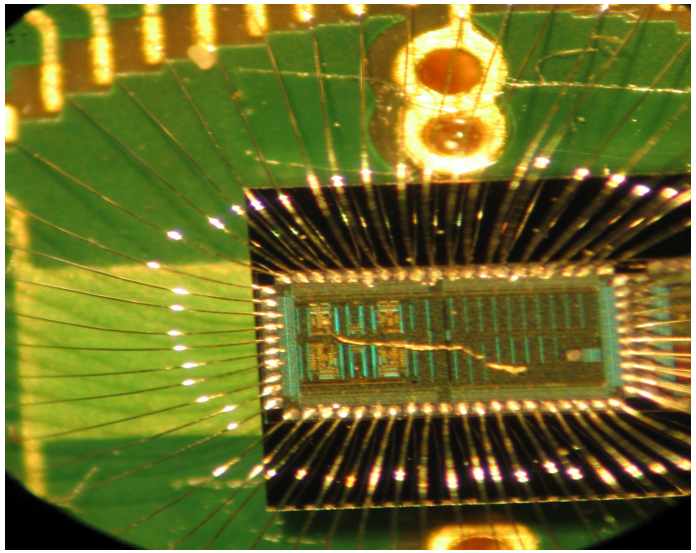


- Voltage Controlled Oscillator (VCO) - core block of PLL - generates output square wave
- Phase Frequency Detector (PFD) compares VCO signal (divided by **N**) with reference signal
- PFD output signals, after processing in Charge Pump (CP) and filtering, give negative feedback to control VCO frequency
- Output wave (**N** times faster) is synchronized with reference clock



Current starved VCO

First transceiver in AMS 0.35µm



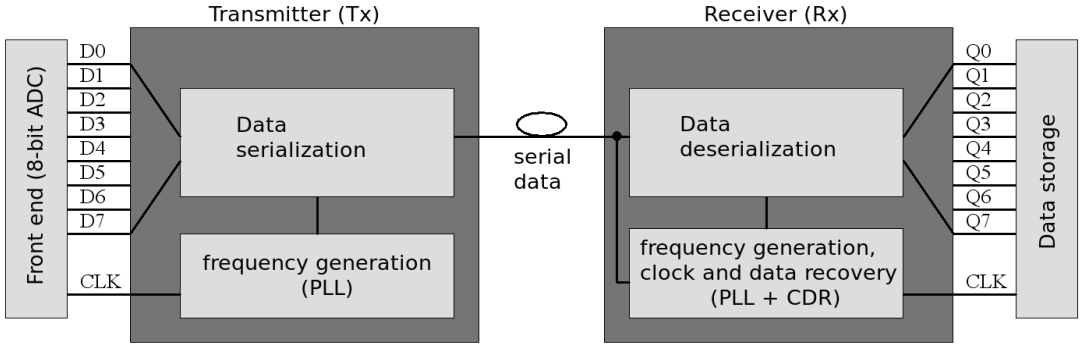
- Transceiver ASIC works in few modes
- Prototype contains:
  - 1st PLL with frequency range:

    480 ÷ 1072 MHz
  - Transceiver with frequency range:

    640 ÷ 976 MHz

PLL generates high frequency in transmitter and receiver

Transceiver architecture

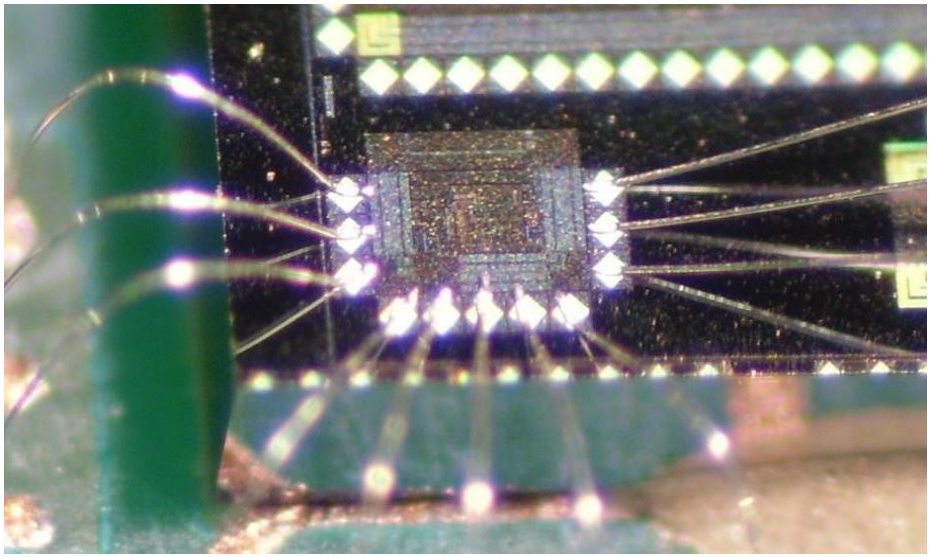


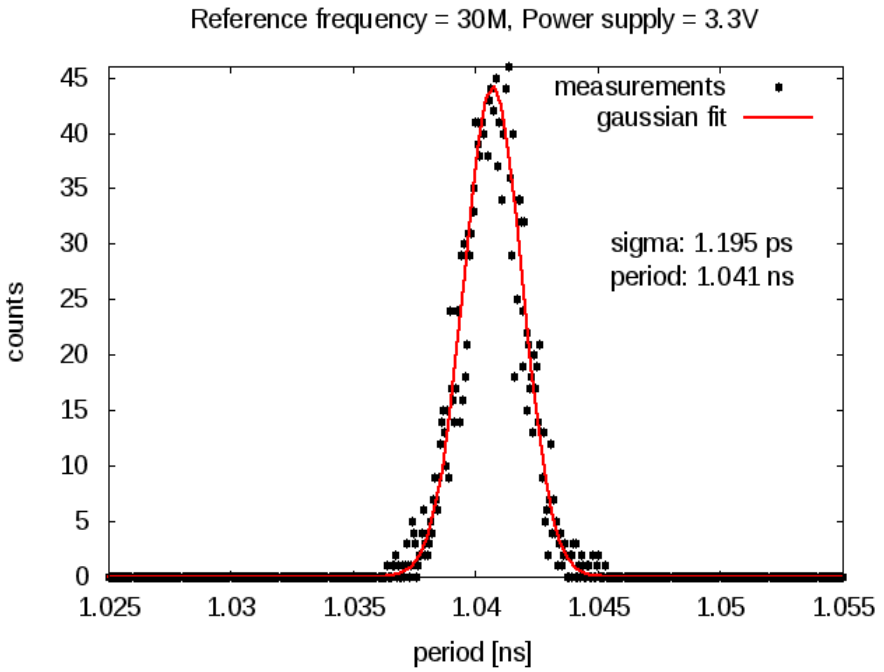
Prototype fully functional

Improved PLL prototype in AMS 0.35µm (as key transceiver block)

- Wide frequency range
  380 ÷ 1120 MHz
- Low power consumption
  4.3mW at 960 MHz
- Low cycle-to-cycle jitter
  <1.2ps at 960MHz

Power consumption about 4 times smaller than 1st PLL prototype

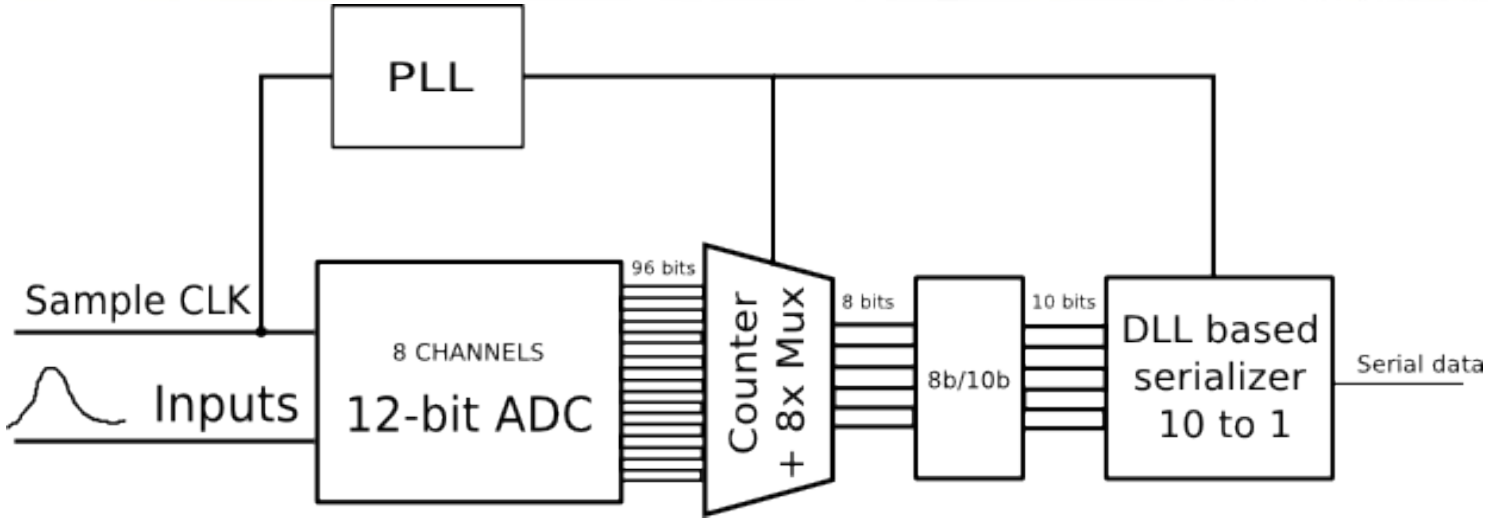




Period distribution measured in Time-domain using 40Gs/s, 4GHz Agilent DSO80404B scope

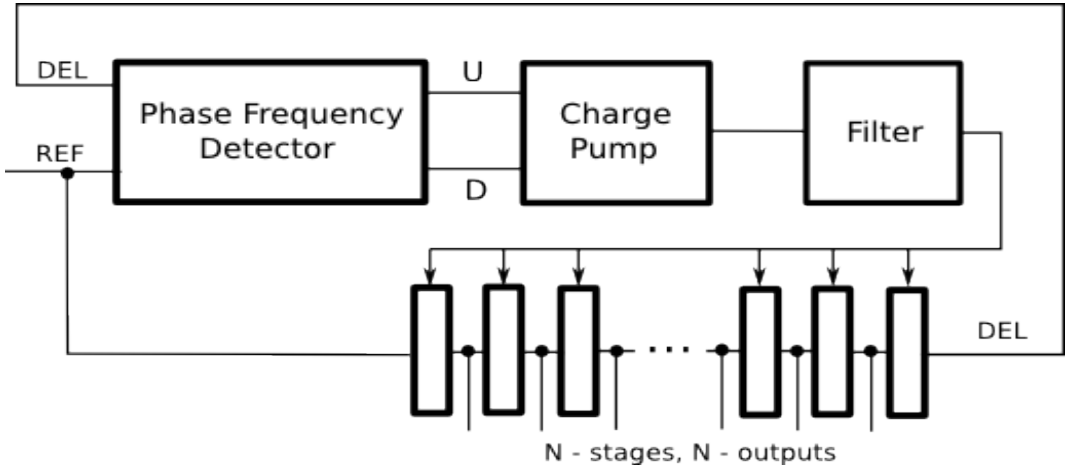
Prototype fully functional

Present project for neurobiology in AMS 0.35µm 8 channel low power 12-bit digitizer & serializer



- **Sample CLK** multiplied by **PLL** is used in first serialization stage (12b → 1b)
- Multiplied clock is used also as reference signal for **DLL**
- **8b/10b** data coding
- **Serial data** rate up to 3Gb/s
- High frequency clock signal is not necessary in this project Sample CLK~20MHz x 12 = PLL output = reference clock for DLL

Present project for neurobiology in AMS 0.35µm
How does Delay Locked Loop (DLL) work?

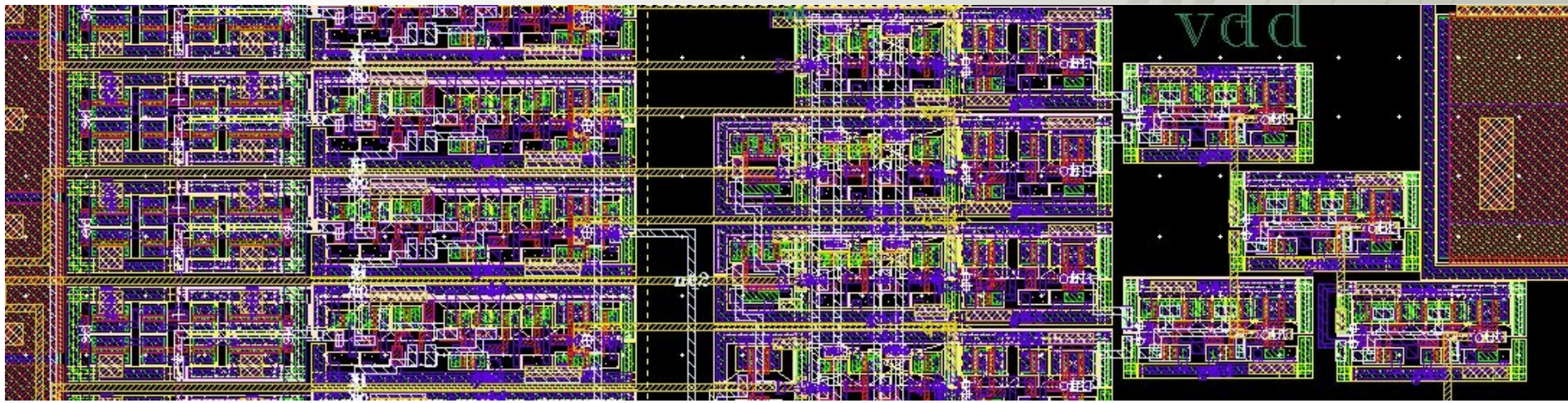


DLL advantages:

- Avoid problems with fast clock distribution
- Same logic for each stage
- Simple multiplexer (in serializer) without decoder and counter

- Variable delay stages are most important part of this design
- **N – stages** gives total delay between 0.5 - 1.5 periods of **REF** clock
- **REF** clock is compared with delayed (**DEL**) clock. As a result the signal controlling the delay of DLL stages is created.
- After synchronization the delay between **REF** and **DEL** is exactly equal to one period of **REF** clock

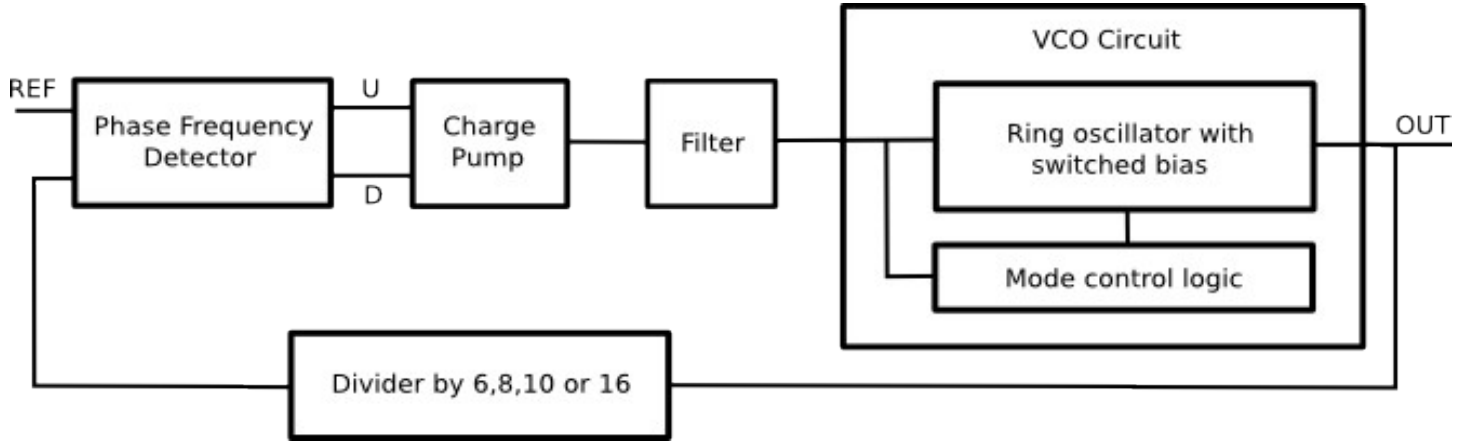
DLL based data serializer in AMS 0.35µm



- Layout dimensions 170 x 220 µm
- Power consumption ~11mW @ 2.5Gb/s (post-layout simulations)
- 10 bit to 1 bit serializer
- Working range:

  250Mb/s – 3Gb/s (switch modes)
- Layout manually drawn
- Project under development – not fabricated yet

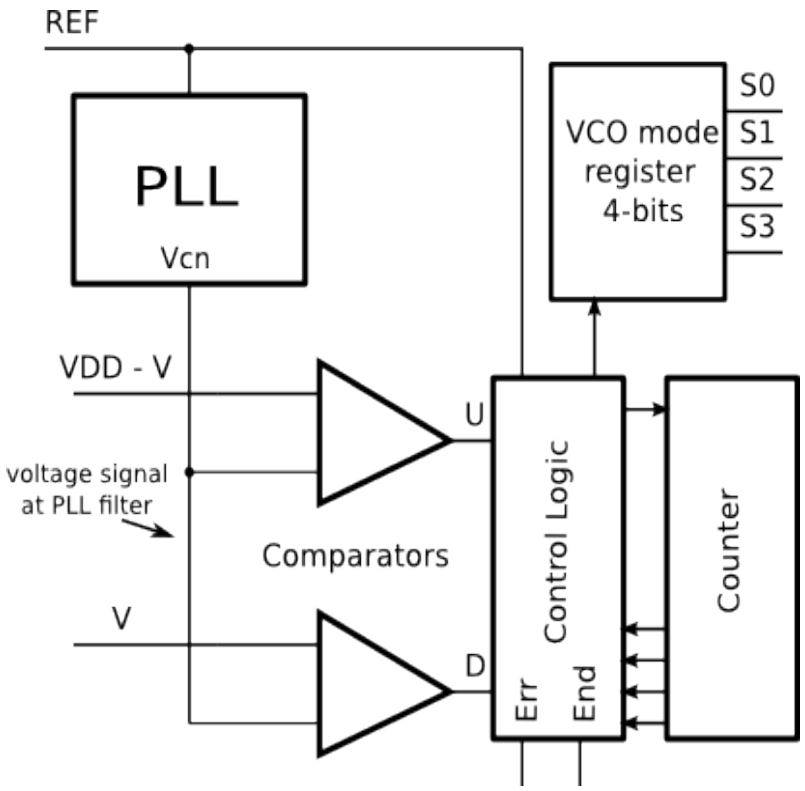
PLL design - IBM 0.13µm – core block for clock generation and data serialization



Expected features:

- General purpose PLL block
- Very wide output frequency range
- Automatically changed (with reference frequency) VCO mode
- Low jitter
- Low power consumption
- Variable loop divider

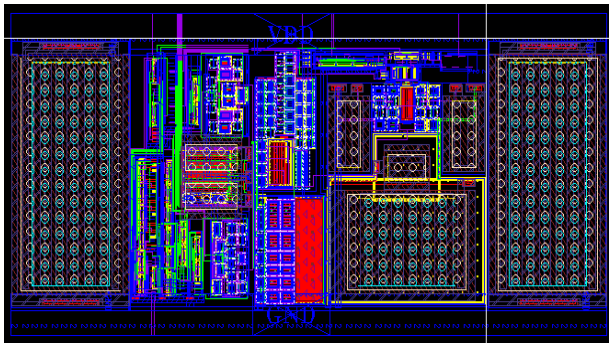
Principle of automatic VCO mode change



- Comparators check whether **voltage signal at PLL filter (Vcn)** is grater than **VDD-V** or lower than **V**.
  - If **Vcn > VDD-V** (VCO too slow) control logic starts count **REF** clocks. Then **mode register** is switched to faster mode.
  - If **Vcn < V** (VCO too fast) VCO **mode register** is switched to slower mode.
  - When **Vcn** voltage is between **VDD-V** and **V** the mode is not changed.

PLL prototypes in IBM 0.13µm

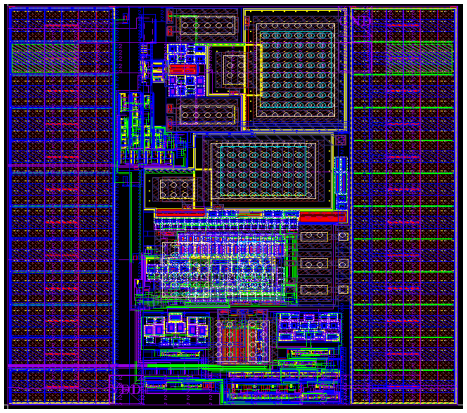
1st prototype



- Output frequency range 60 – 520MHz
- Low power consumption ~0.2mW @ 500MHz
- Low jitter ~ 1.5 ps (RMS)
- Low area 200x160 um
- Automatically changed VCO modes
- PLL divider by 8 or 10
- Used for 10-bit ADC serialization

Submitted in February 2012

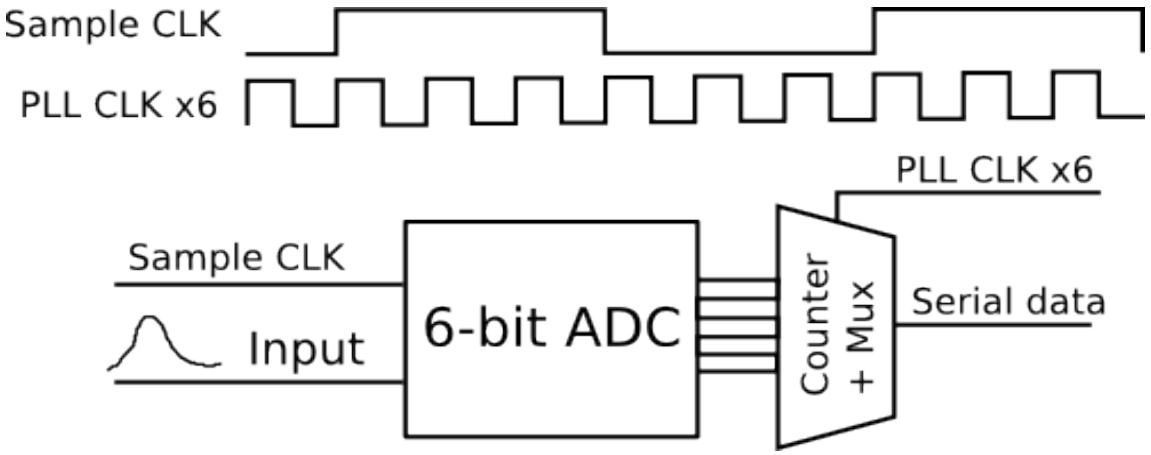
2nd prototype



- Output frequency range 8MHz - 3GHz
- Low power consumption ~1mW @ 3GHz
- Low jitter ~ 1 ps (RMS)
- Low area 300x300 um
- Automatically changed VCO modes
- PLL divider by 6, 8, 10 or 16
- Used for 6-bit ADC serialization

Submitted in May 2012

Serialization in 6-bit ADC for LHCb upgrade

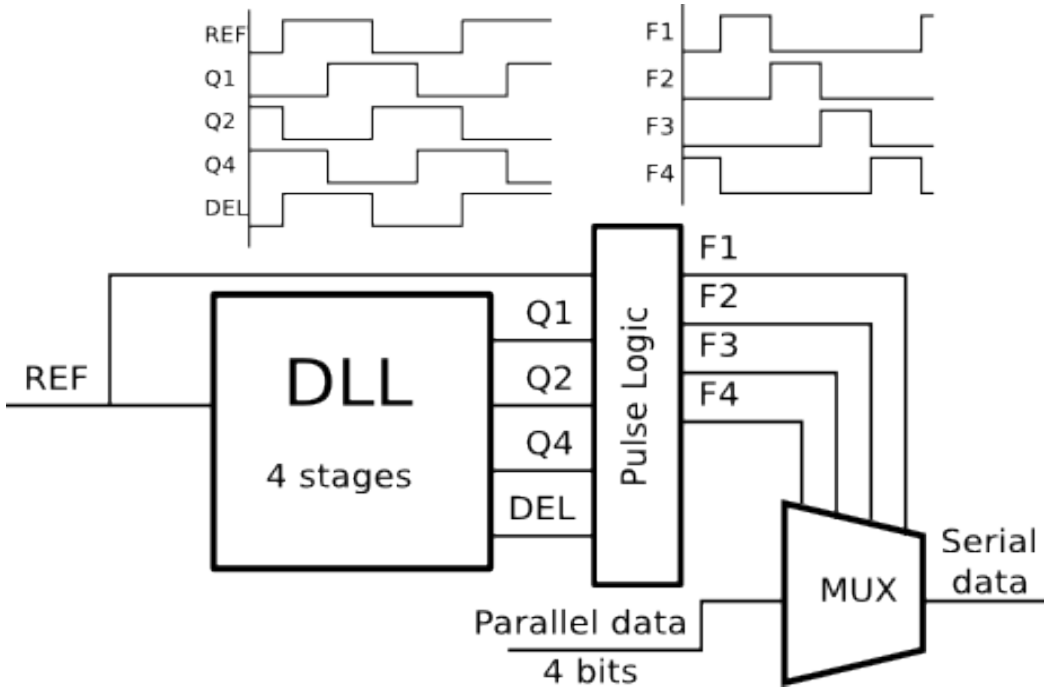


PLL used to multiply **Sample CLK** frequency by 6 (in this example)

- 6-bit ADC stores sample at the rising edge of **Sample CLK**
- 6 times faster **PLL CLK** (generated by 2nd PLL version) is sent to counter and multiplexer
- Parallel data from ADC is converted to **Serial data** output

Thank You for your attention

Data serialization using DLL



- DLL creates 4 waveforms (**Q1,Q2,Q3,DEL**) shifted by ¼ period of **REF** clock
- Phase difference between **REF** and **DEL** after synchronization is equal 2π

- Signals from DLL converted by **Pulse Logic** control multiplexer (MUX)
- Pulse signals **F1 – F4** are using to transform **Parallel data** bits to serial data. Width of this signals set bit width on **Serial data** output.