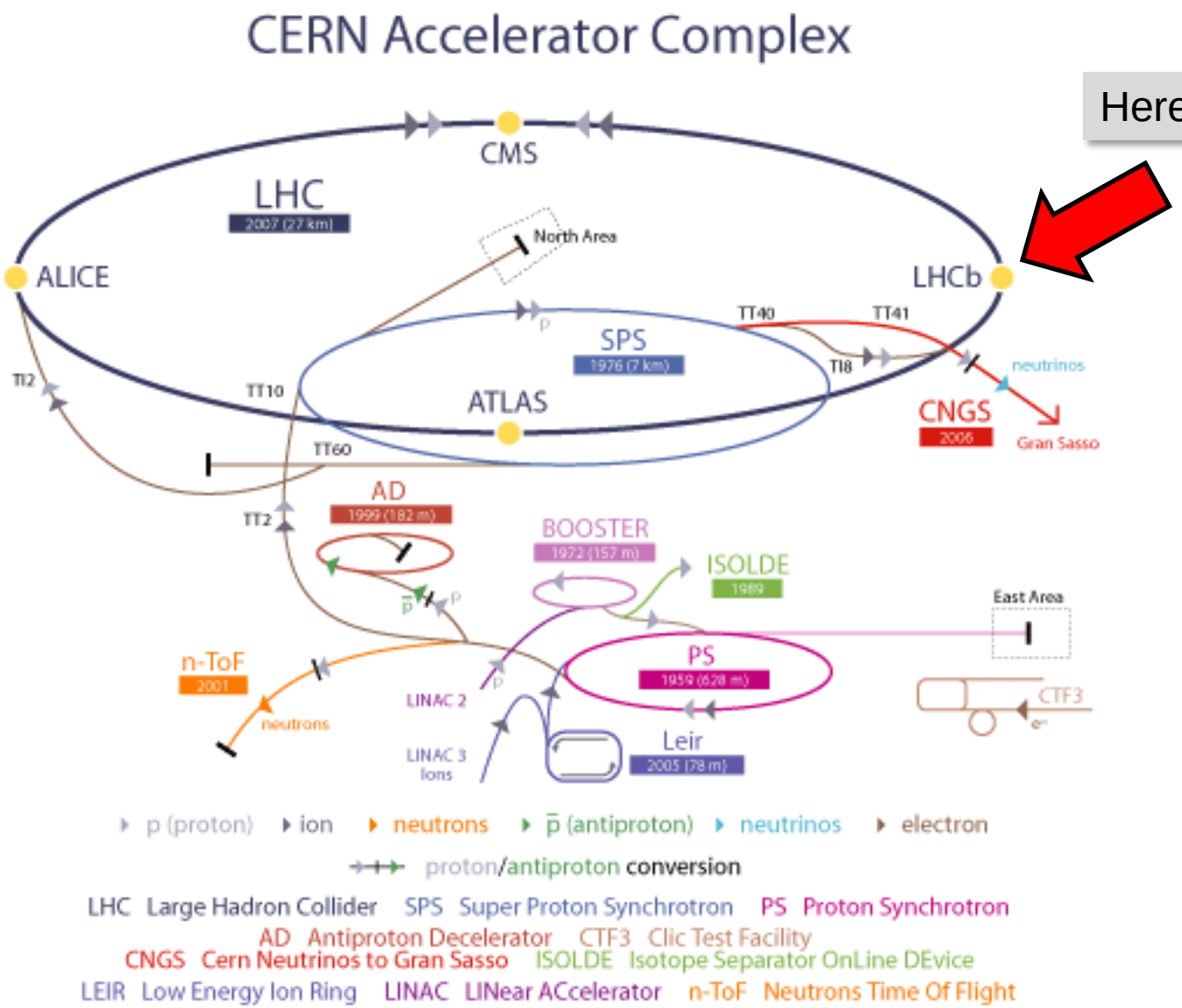
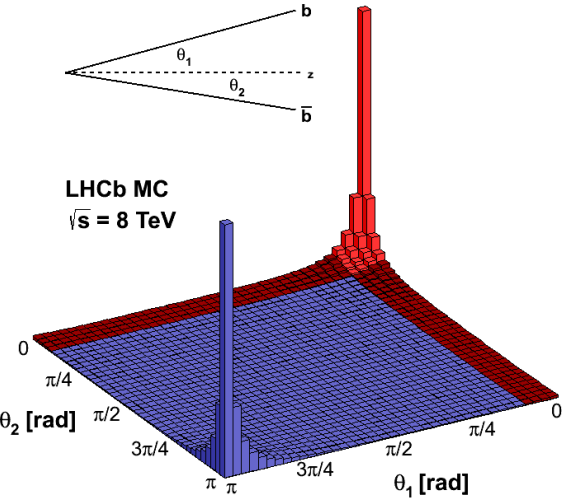
# Workshop on Common ASIC for the LHCb Upgrade

- A very brief introduction to the LHCb detector and upgrade

# LHCb at LHC

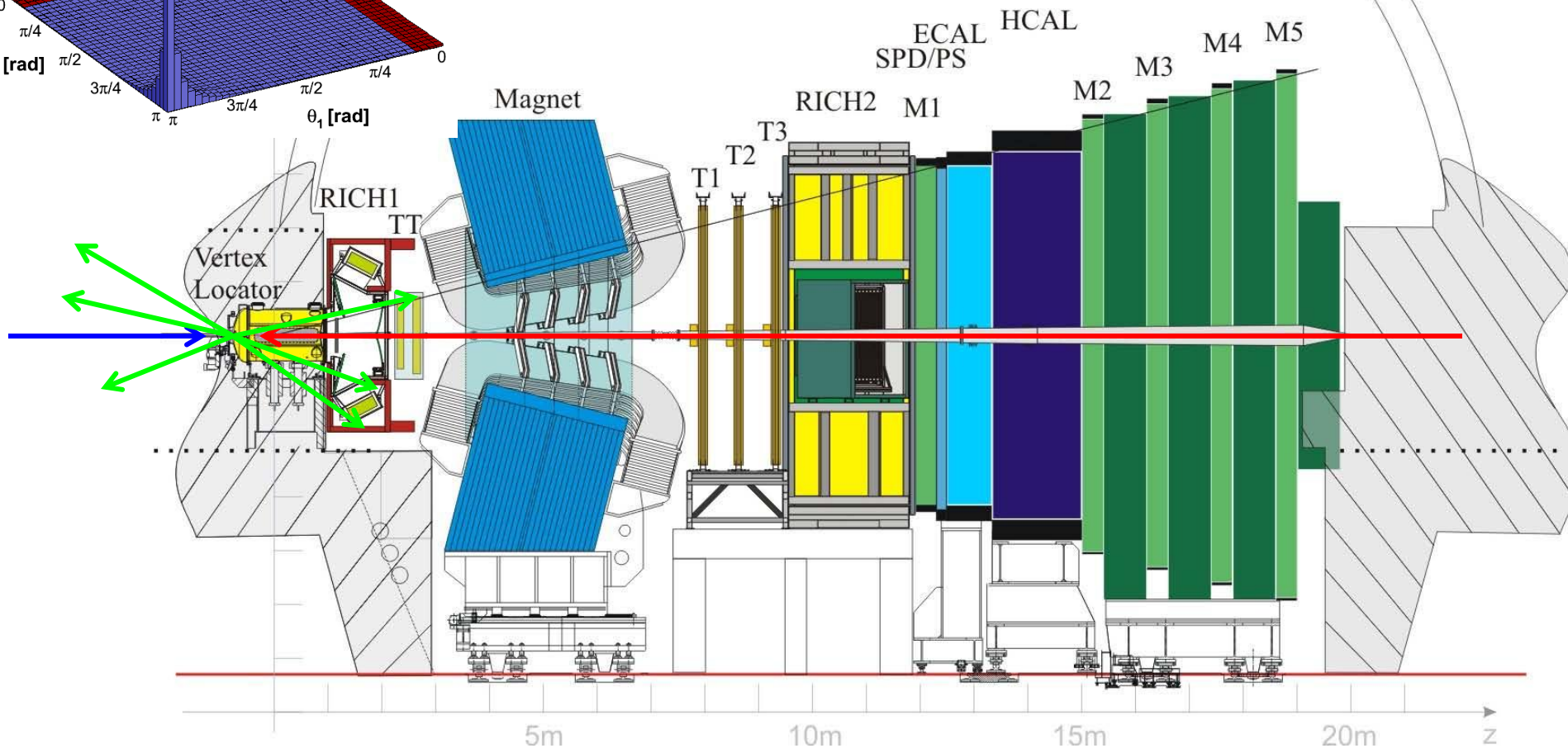

CERN Accelerator Complex
Here, at Point 8
CMS
LHC
2007 (27 km)
North Area
ALICE
LHCb
SPS
1976 (7 km)
TT40
TT41
TI8
neutrinos
CNGS
2006
Gran Sasso
TI2
TT10
ATLAS
TT60
AD
1999 (182 m)
TT2
BOOSTER
1972 (157 m)
ISOLDE
1989
East Area
n-ToF
2001
neutrons
LINAC 2
PS
1959 (628 m)
CTF3
LINAC 3
Ions
Leir
2005 (78 m)
p (proton)
ion
neutrons
p̄ (antiproton)
neutrinos
electron
proton/antiproton conversion
LHC Large Hadron Collider
SPS Super Proton Synchrotron
PS Proton Synchrotron
AD Antiproton Decelerator
CTF3 Clic Test Facility
CNGS Cern Neutrinos to Gran Sasso
ISOLDE Isotope Separator OnLine DEvice
LEIR Low Energy Ion Ring
LINAC LINear ACcelerator
n-ToF Neutrons Time Of Flight

# LHCb



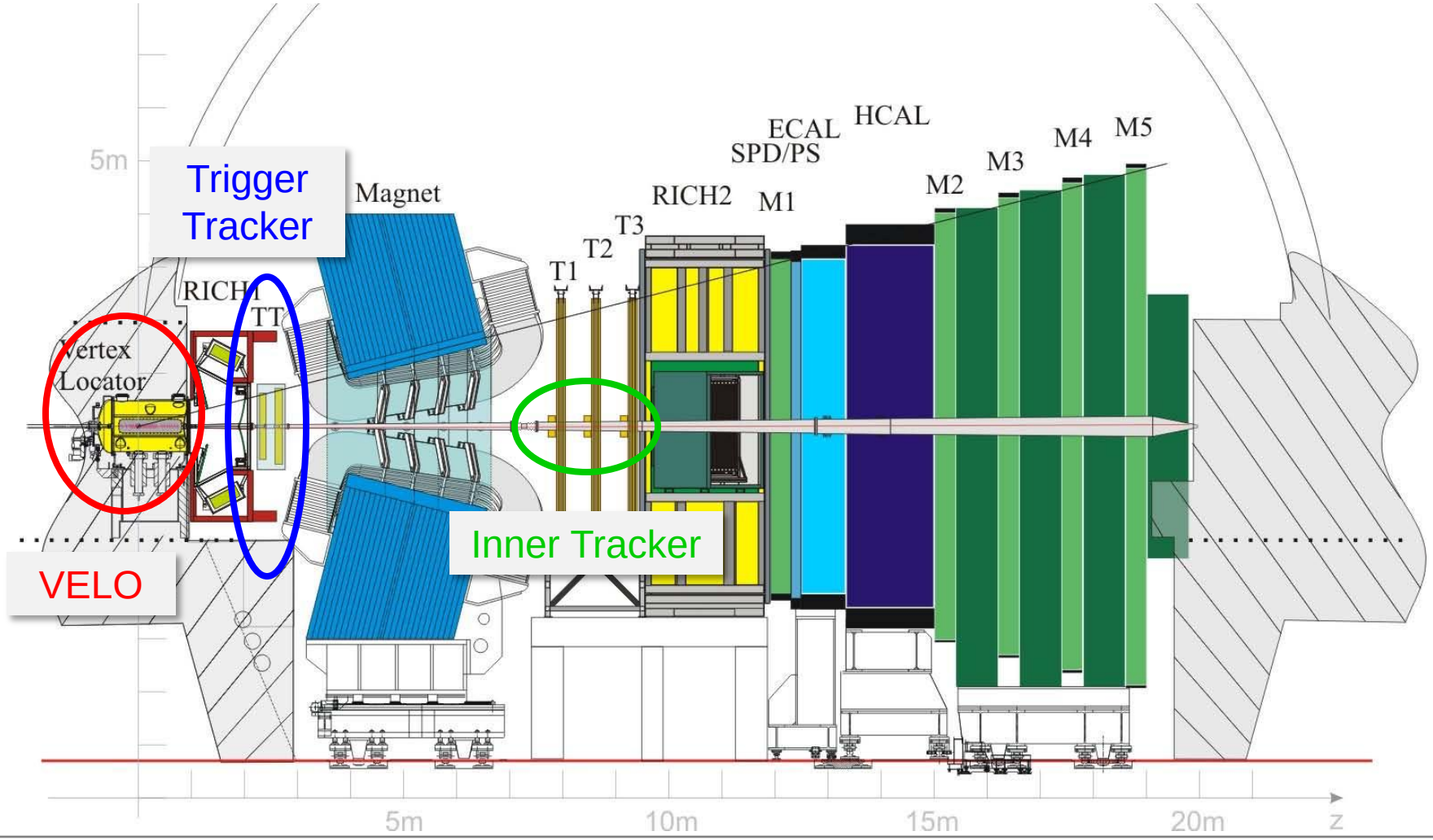

An LHC experiment for CP violation and rare decays in the B sector

(and much more, especially after the upgrade)

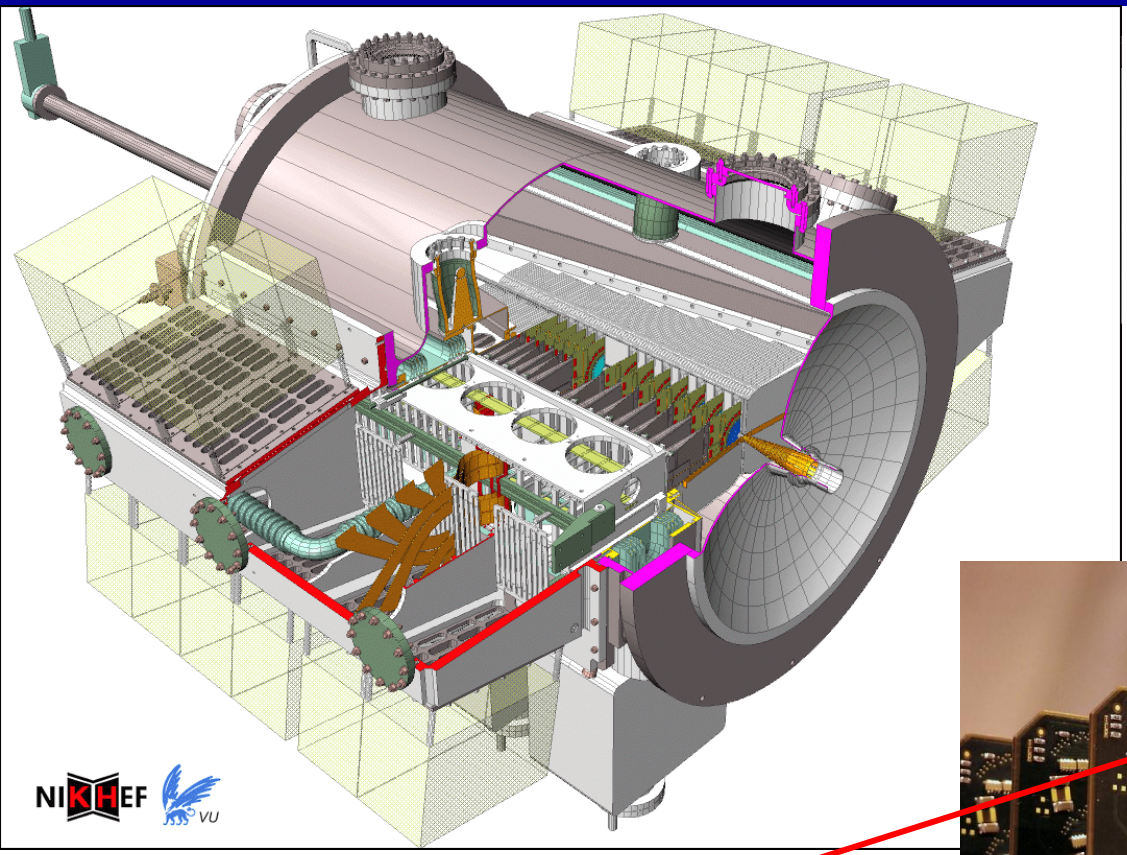


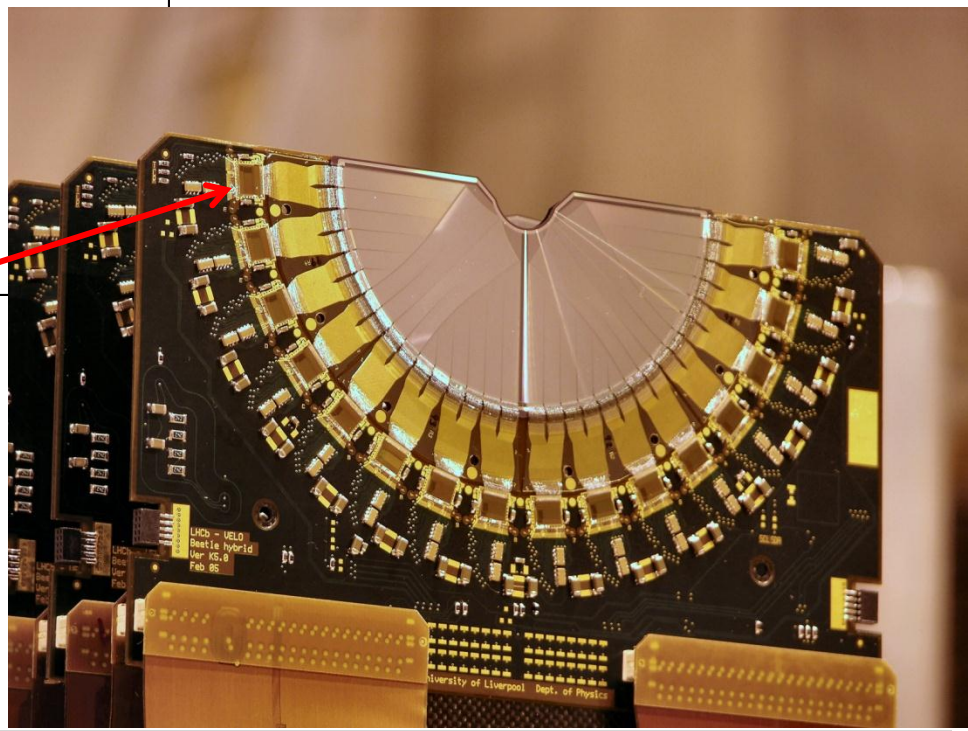
# LHCb Detector Upgrade

Subsystems for which silicon strips are considered



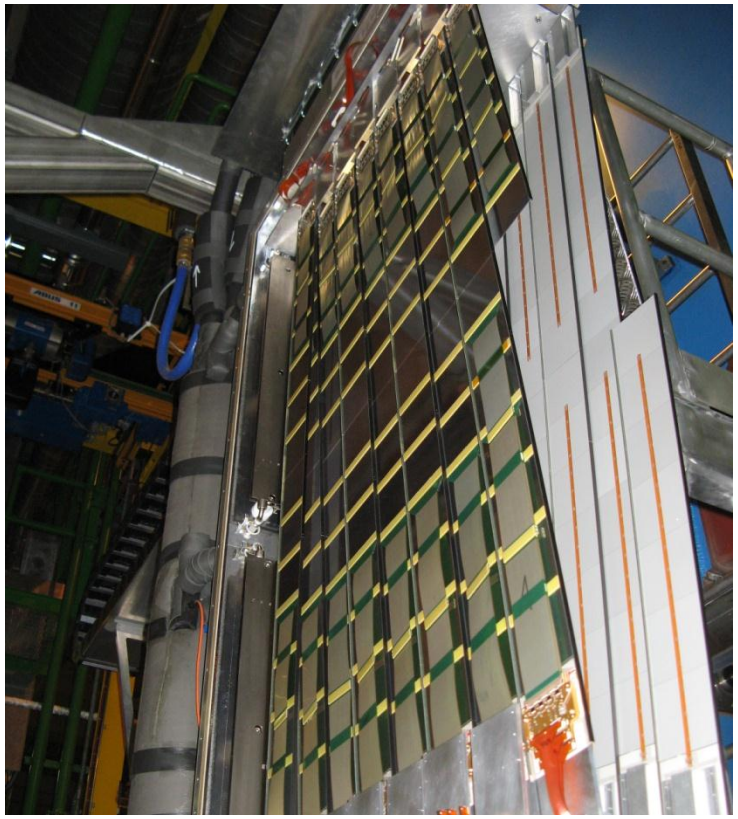
# VELO now

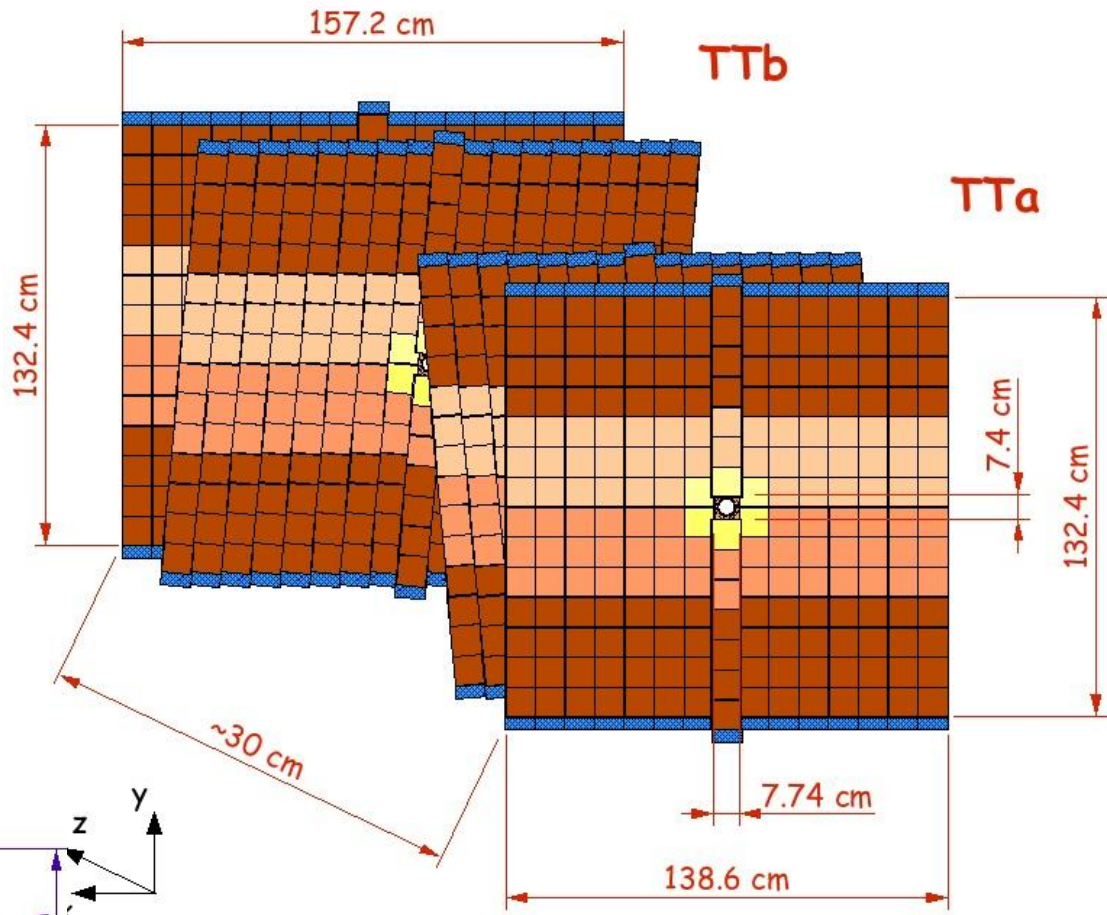


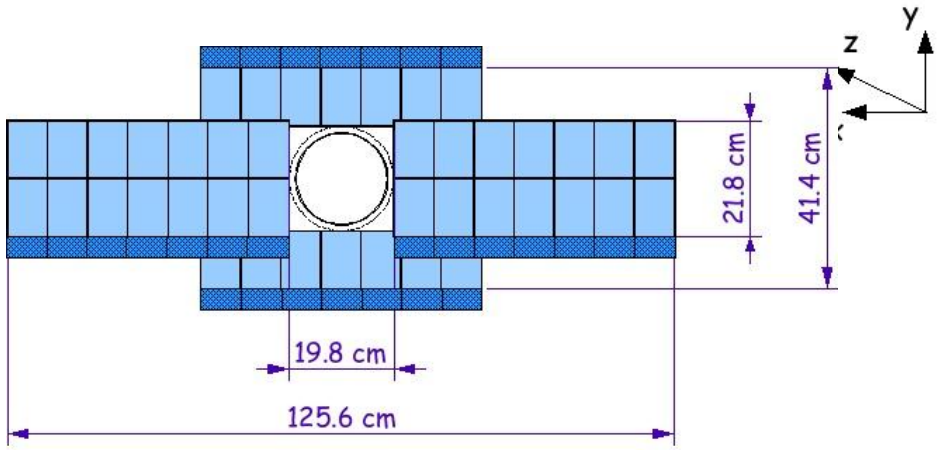




- Beetle chip

# TT an IT




157.2 cm
TTb
TTa
132.4 cm
7.4 cm
132.4 cm
~30 cm
7.74 cm
138.6 cm

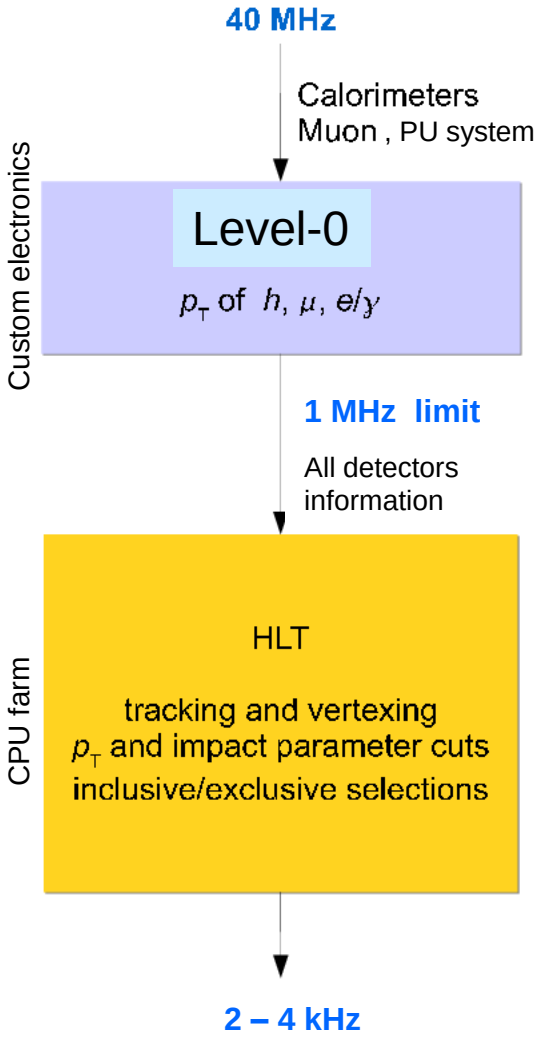

z
y
21.8 cm
41.4 cm
19.8 cm
125.6 cm

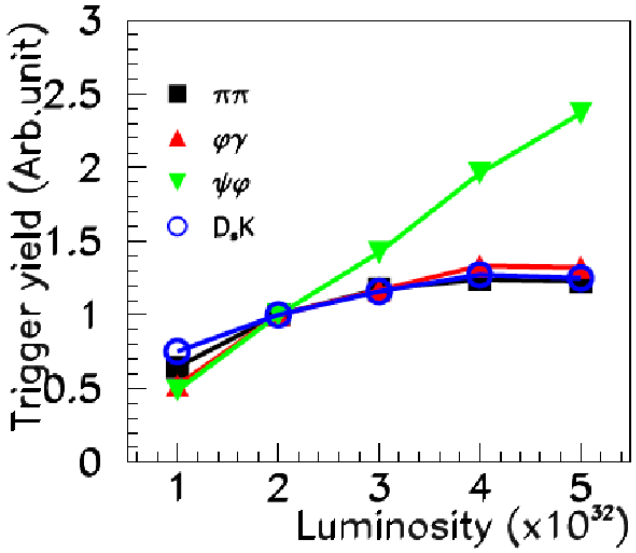
# Trigger overview

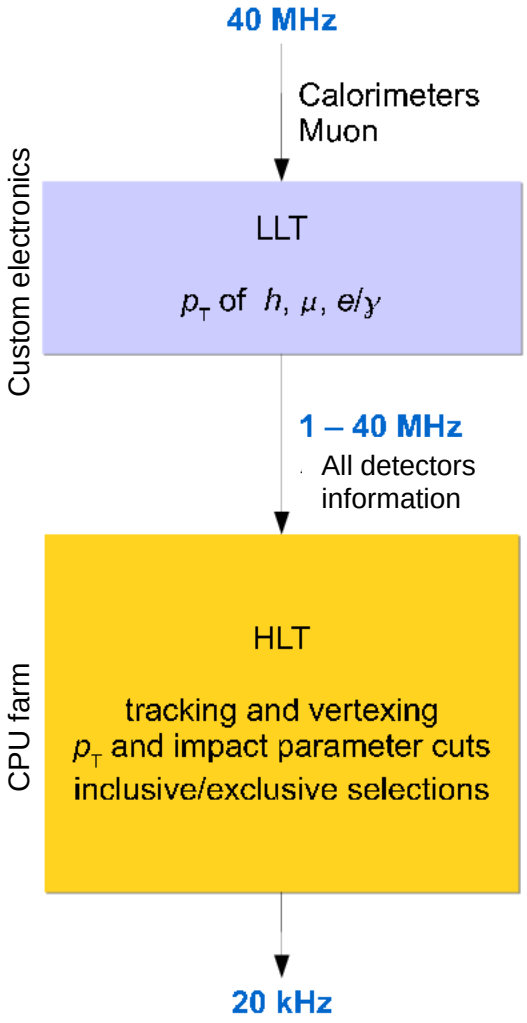
Current LHCb

not so Long Shutdown 2018

LHCb Upgrade



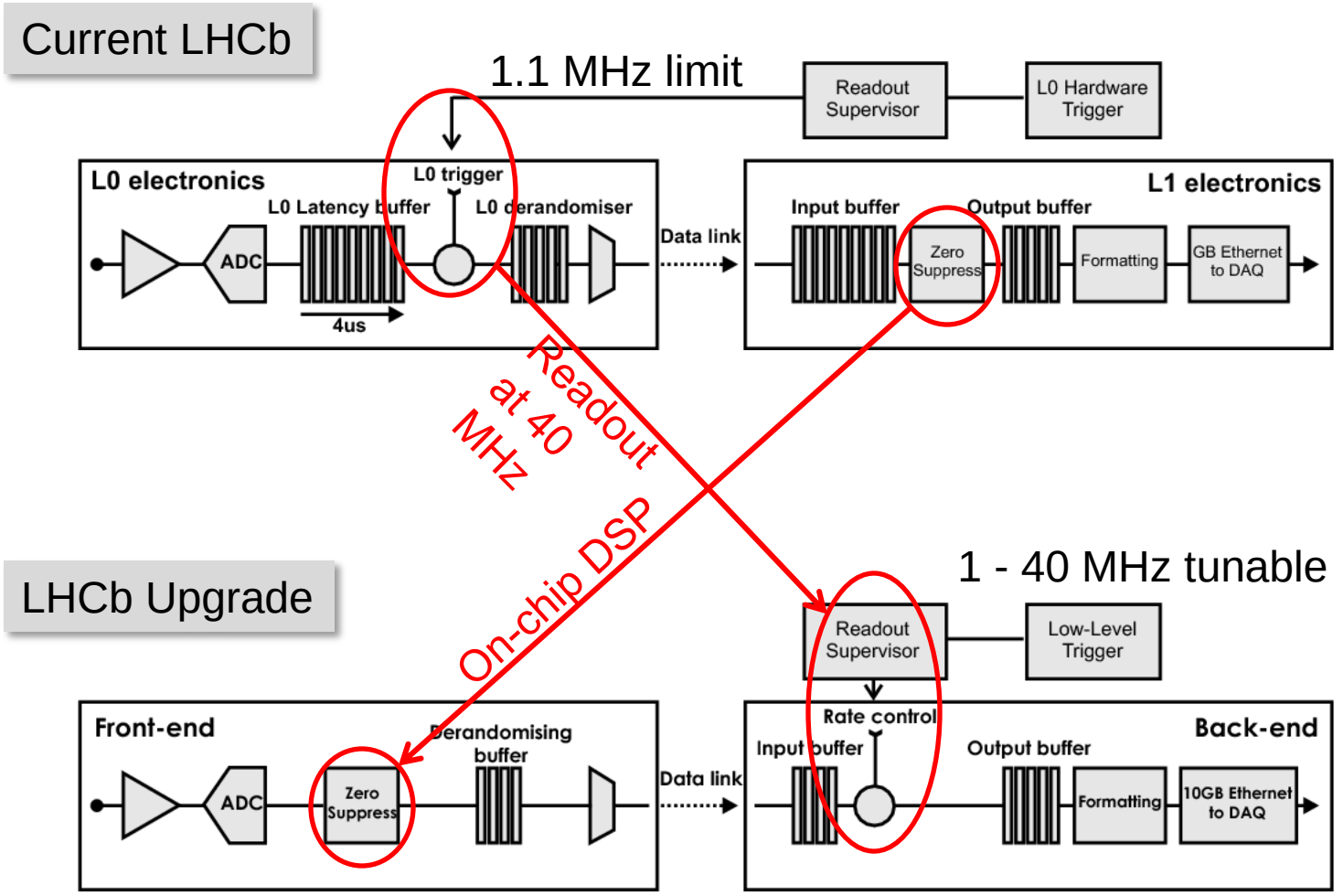




The 1 MHz limit being removed, we can crank up the luminosity to

**1 – 2 x $10^{33}$ Hz/cm$^2$**

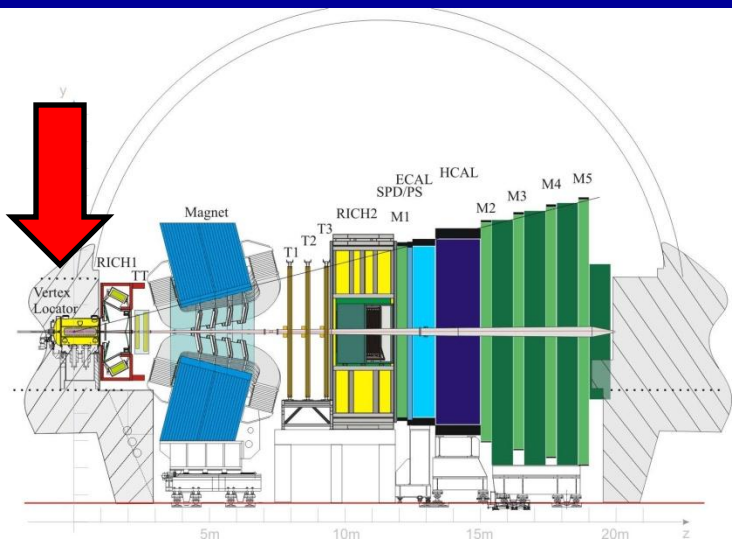
⇒ Compared to 2012 annual yields, we gain a factor ~ 10 / 20 for muonic / hadronic channels

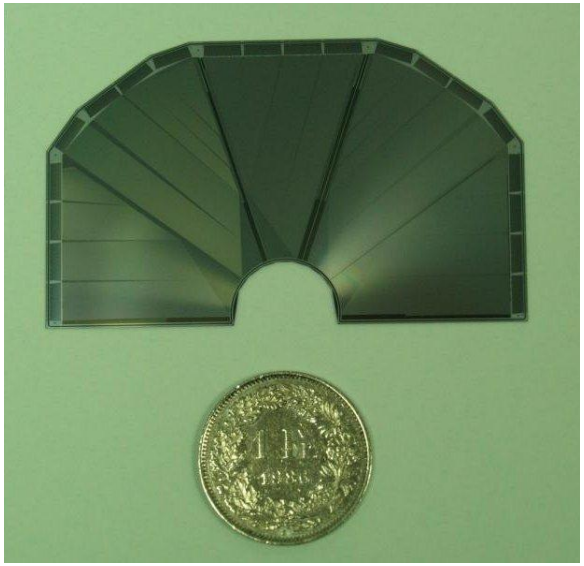
# Change in readout electronics



# VELO upgrade

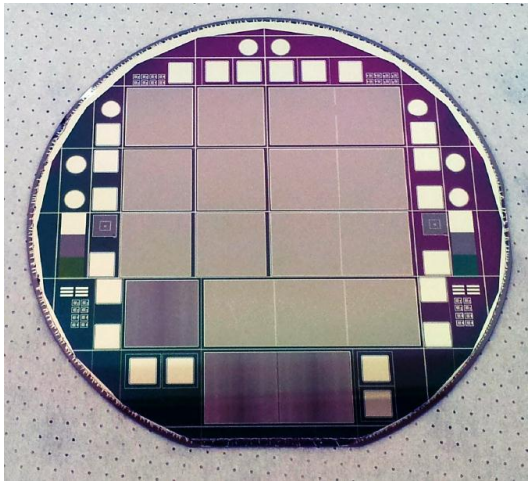
- More luminosity, more radiation
  - Must withstand up to ~ 8 x $10^{15}$ $n_{eq}/cm^2$ ( ~370 Mrad), highly non-uniform
- New (“stronger”) cooling
  - Studying microchannel, TPG, diamond substrate
- No degradation in performance!
  - Material budget, occupancy
  - Aim at 200 um, n-in-p, 25um min pitch
- Strip sensor development in progress
- Prototypes just received



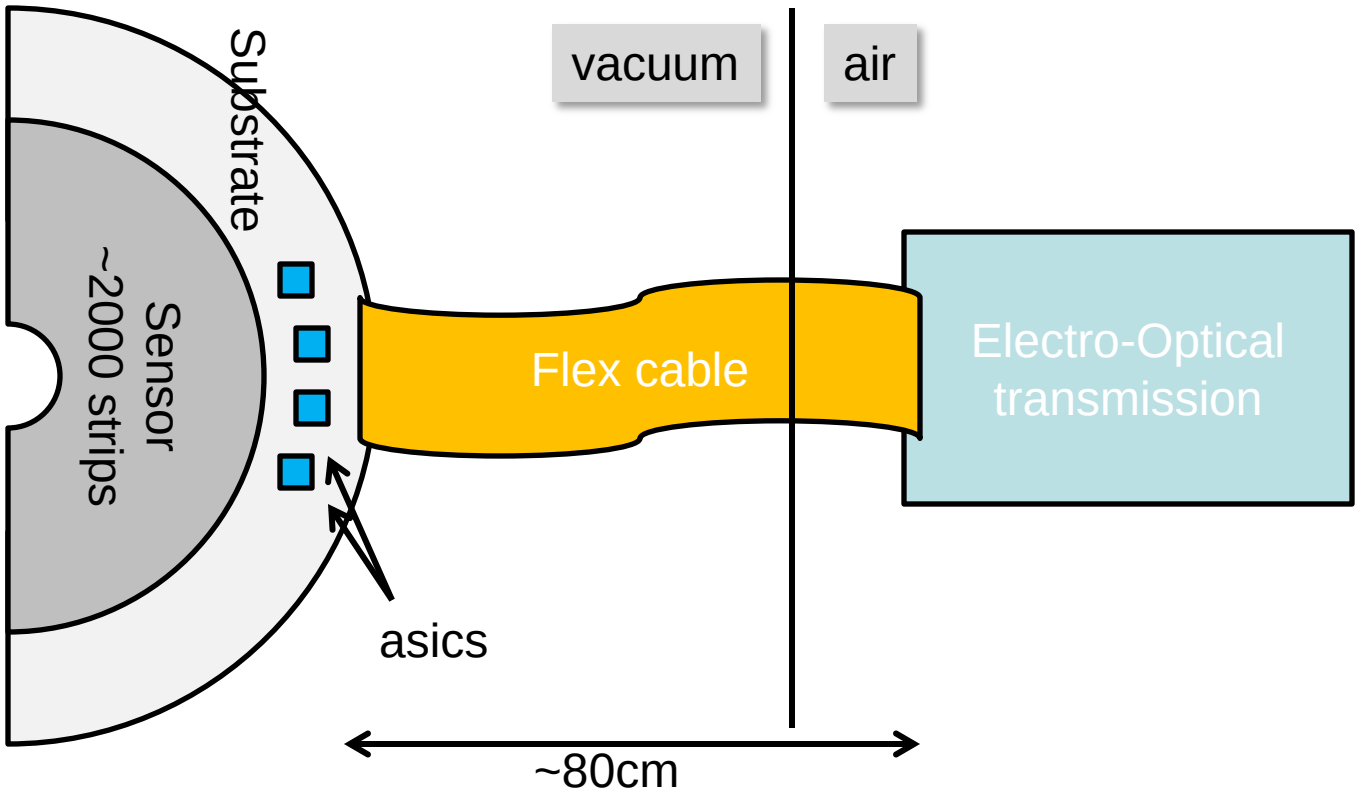
- Alternative: **Pixels**

  Choice to be made in first half of 2013



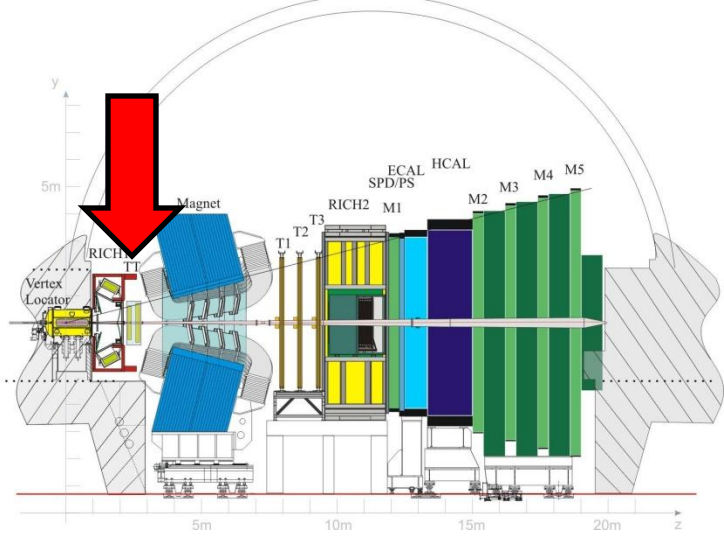
# VELO module design in powerpoint…

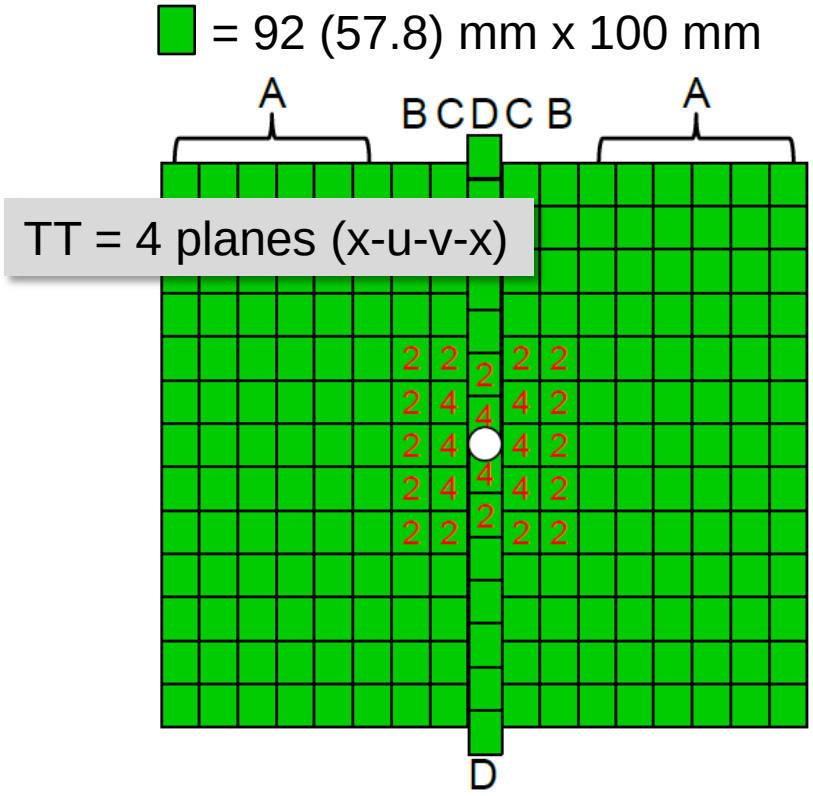
- FE chips directly bonded to the sensor, no pitch adapter
- Cooling provided to substrate
- Digital data sent out via a flex cable to outside the vacuum
- Electro-optical transmitters in air



# Trigger Tracker upgrade

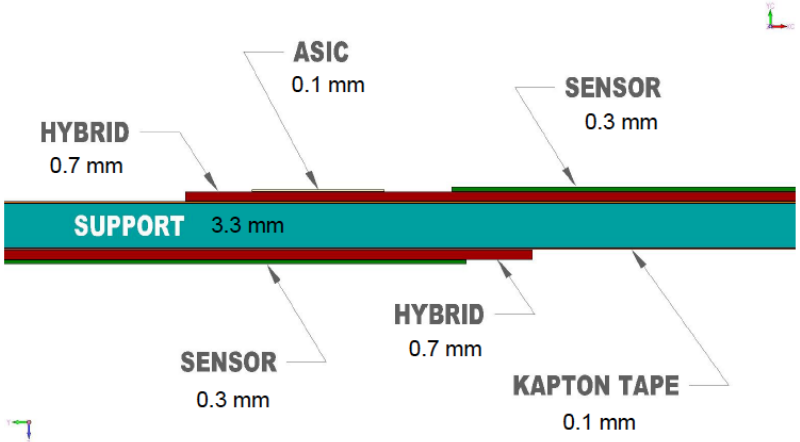
- Importance
  - Trigger (fast *p* measurement, VELO+TT)
  - Long lived particles (e.g. $K_S$) rec'tion
  - TT+T tracks to improve *p* resolution and reduce ghost rates
- Redesign completely
- Radiation in inner region similar to VELO before upgrade (~ few x $10^{14}$ $n_{eq}/cm^2$ )
- Improve on acceptance coverage
  - Remove gaps between sensors
  - Come closer to beam pipe
- Challenge: reduce material
  - Light  mechanics, convective cooling ?
- Sensors: (under study)
  - both n-in-p and p-in-n being considered
  - Pitch 178 um for outer region, less for inner
  - Sectorisation in inner region (grouping in outermost ?)



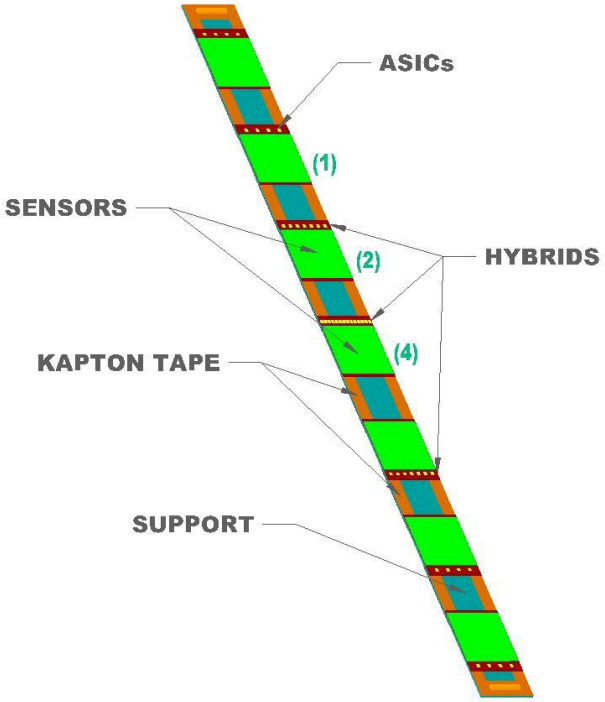



# TT: “stave design”

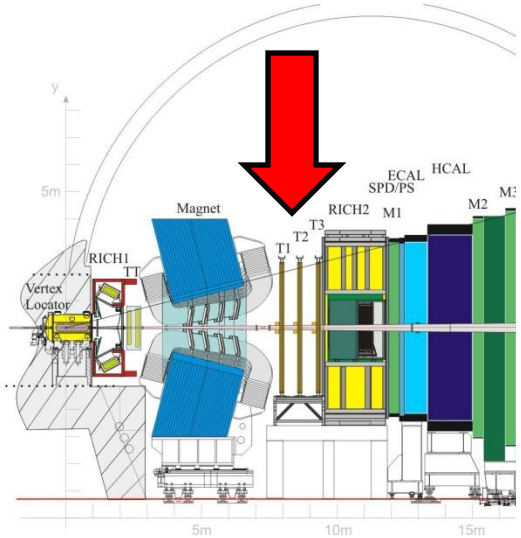
- Design inspired from ATLAS staves (see P. Allport et al, NIM A 636 (2011) S90–S96)
  - ASICs are mounted on hybdrids directly on the sensors
  - Sensors can have 1, 2 or 4 rows of strips (10, 5 or 2.5cm)
- Prototype sensor to be procured this summer
- Mockup stave being built
  - Model in ANSYS for thermal modelling
  - Build  a mockup in summer




$X_0$ = 1.511% (average per plane, including overlaps in x and y)
This number contains cooling assumptions that are yet to be minimized.



# Tracker stations



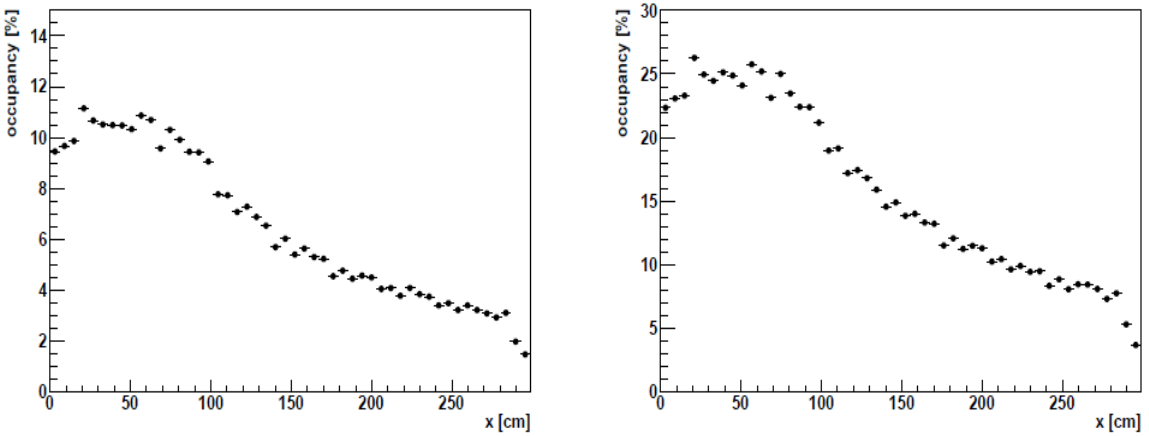




Figure 6.7: Occupancy distribution using MC for $b\bar{b}$ events *vs* the $x$-coordinate in the OT detector with the current detector for a luminosity of (left) $\mathcal{L} = 2 \times 10^{32}\text{cm}^{-2}\text{s}^{-1}$, (right) $\mathcal{L} = 10^{33}\text{cm}^{-2}\text{s}^{-1}$.

- Occupancy in inner regions of Outer Tracker will be too high at ~2e33 => the “hole” size must be increased

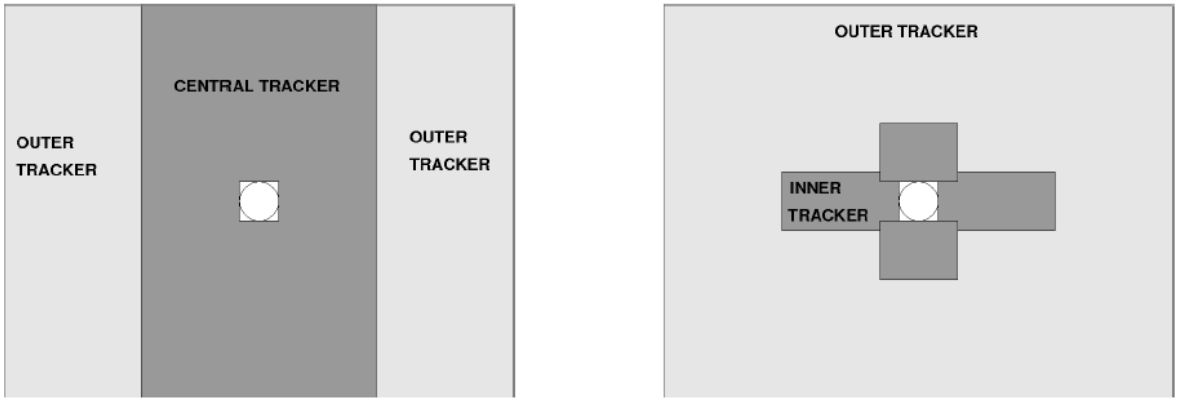



Figure 1: Schematic layouts of the two options being studied for the upgrade of the LHCb tracking stations (not to scale). Left: OT straw tubes (light grey area) with scintillating-fibre CT (dark grey area). Right: OT straw tubes (light grey area) with IT made of microstrip silicon sensors (dark grey area). The central hole is for the beam pipe.

- Two solutions being studied

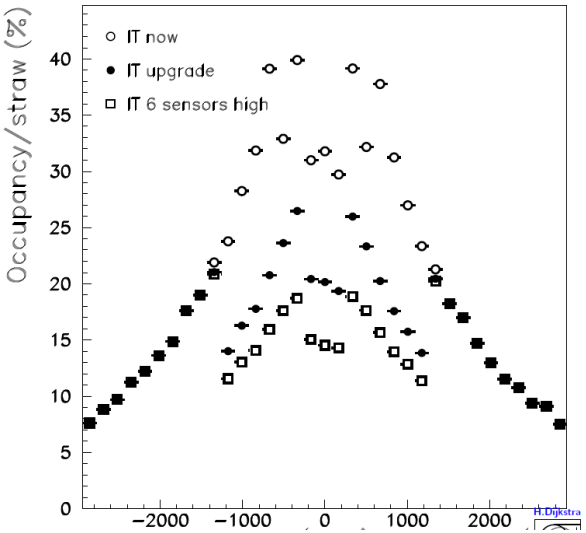
# Inner Tracker upgrade

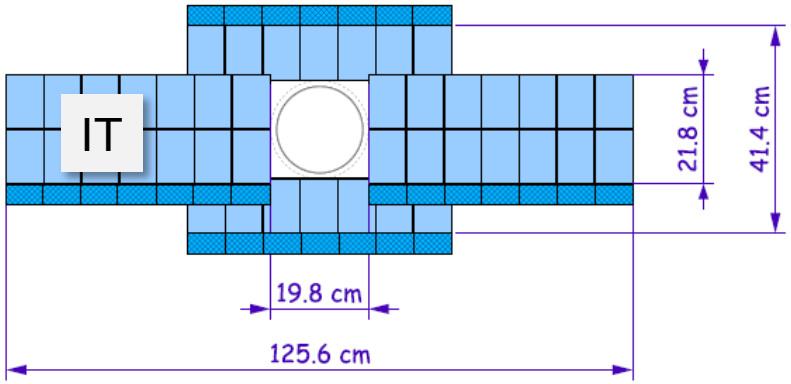
- Increase size + decrease mass of IT to cure the OT occupancy problem

Incl-B, minimal upgrade, i.e.

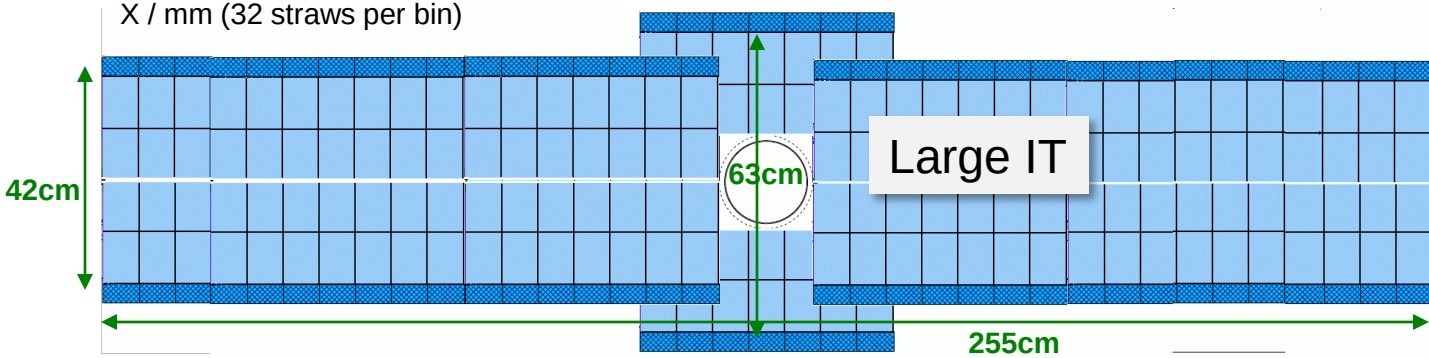
- Beam-support: halved
- IT behind OT
- xdsts: Upgrade/XDST/00005533/
- $L = 20 \times 10^{32}$
- 4→6 sensor high: few % reduction.

Note: present IT X/X0.



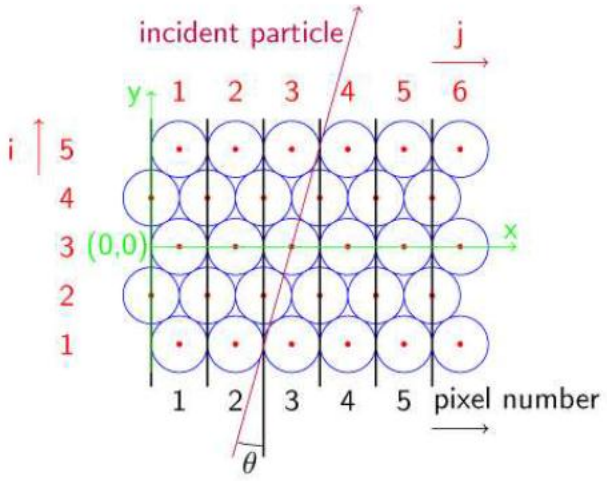




Challenges:
- Mass reduction
- Cost




- From 126x22(41) cm to 255x42(63) cm
- Increase number of sensors/layer by nearly factor 4, ×3.3 for 10 layers.
- "$\eta$" coverage: IT/(IT+OT)= 33% → 54%

# SciFi R&D



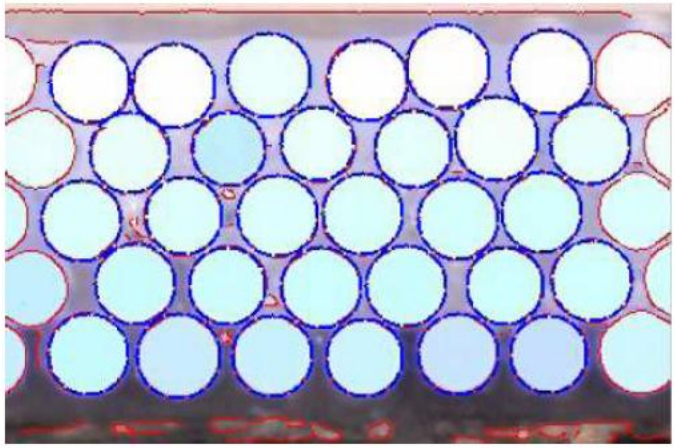
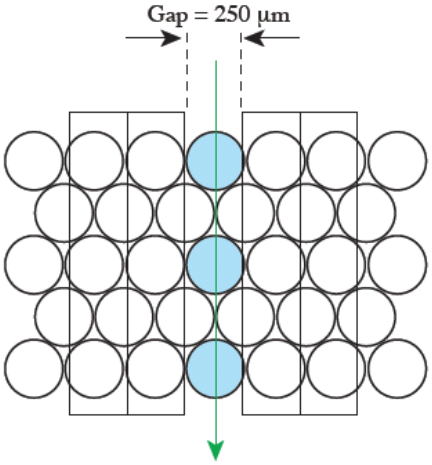
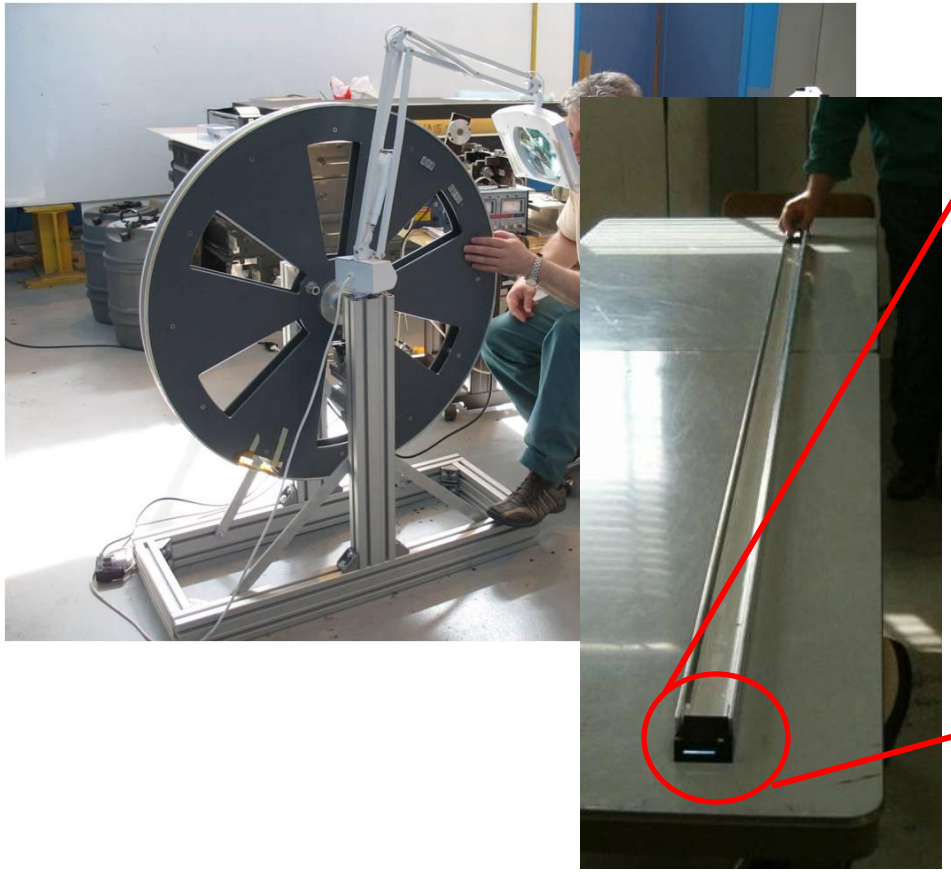



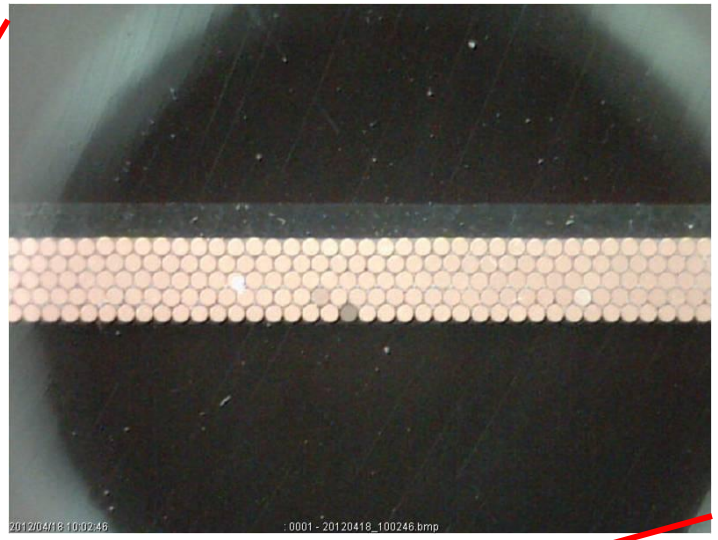
Figure 6.27: Left: ideal configuration of 5 layers of fibres. Right: picture of a portion of a fibre tracker prototype built for the PEBS experiment, seen from one end. The contour of each fibre was drawn by a pattern recognition program which is used to measure the alignment precision of each fibre with respect to its nominal position.

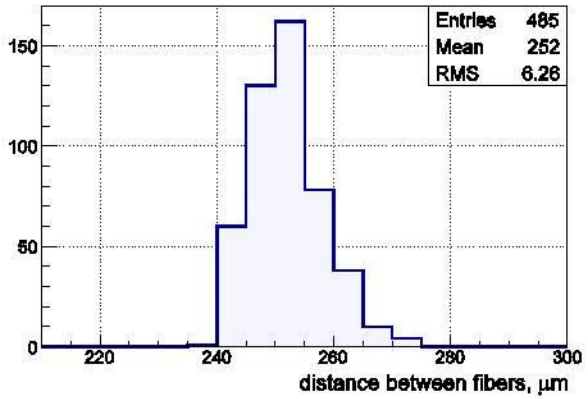
- SciFi module
  - 2.5m-long module
  - 5 fibre layer
  - 0.25 um fibres
- Fibres read out by 128-channel SiPM
- Front-end electronics to be designed



# Prototype module



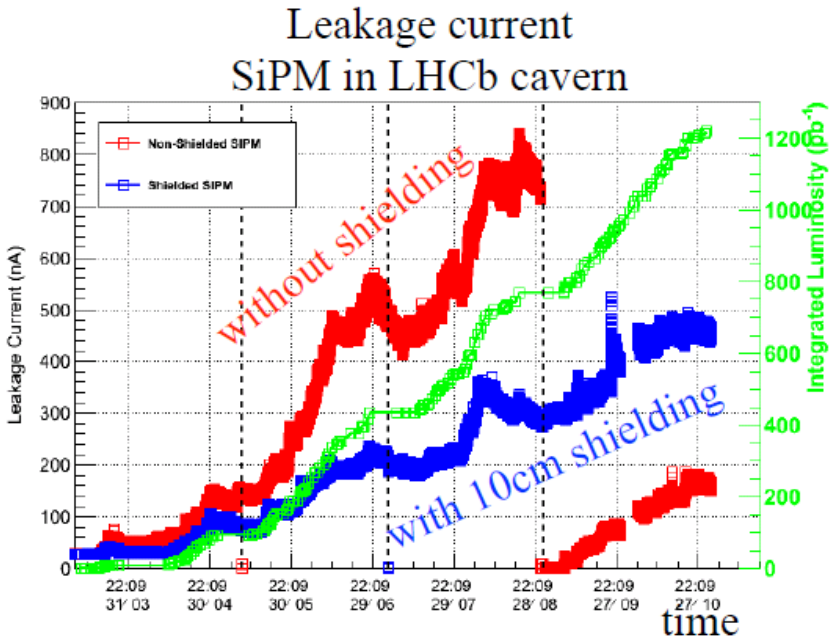




# SciFi challenge: SiPM and fibre radiation hardness

SiPM:

- Will require cooling




Fibres:

- Attenuation vs irradiation:
  is it viable ?

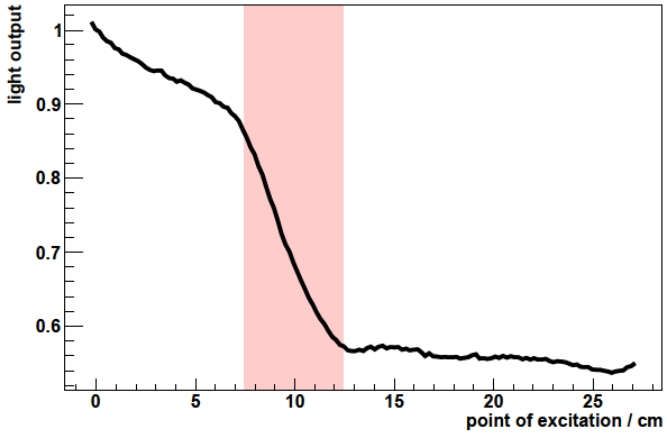
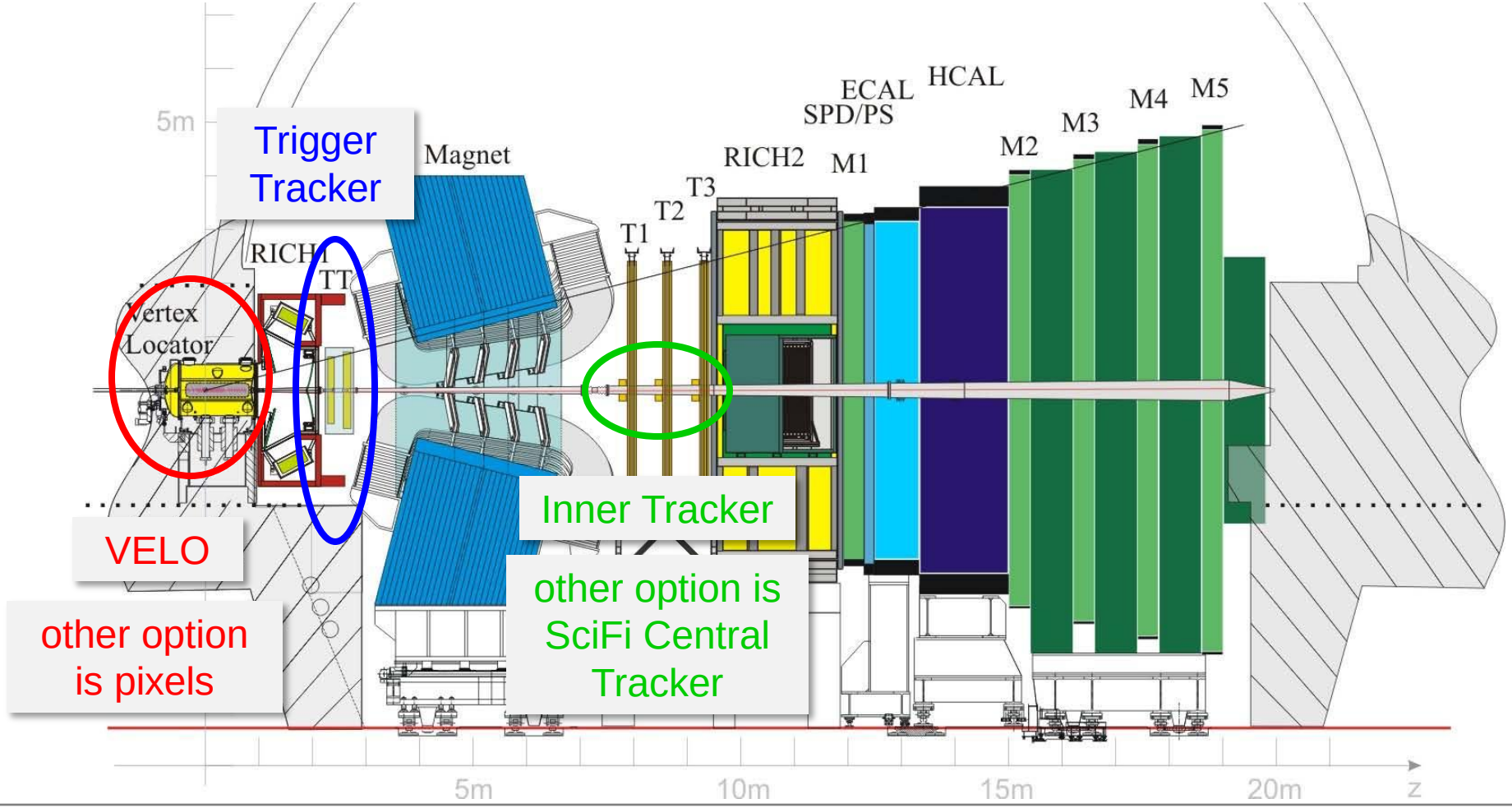



Figure 6.28: The light output of a scintillating fibre as a function of the distance between the point of excitation and the end of the fibre where the light yield is measured. The fibre was irradiated with a dose of $10^5$ Gy in the marked area.

# Silicon strip options in LHCb Upgrade

Approximately:

- **VELO:** ~ 20 asic/sensor * 100 sensors = **~2000 asics**
- **TT :** ~ 4 asic/sensor * 250 sensors/layer * 4 layers = **~4000 asics**
- **IT:** ~ 3 asic/ladder * 82 ladders/layer * 10 layers = **~2500 asics**



# LHCb Upgrade somatosensorial homunculus


**The Si-strip ASIC will be vital for the LHCb upgrade**

# Organization of this meeting

Many thanks to Marek and Tomasz

- Collaboration matter (Thu morning)
- Technical matter (rest of the time)

# Collaboration matter

- Review R&D + production schedule with spending profile
- Resources, expertise, activities in various institutes
  - Sharing and coordinating
- Identify people who will do design and/or testing for LHCb strip ASIC
- Synergy with other applications (SiPM, …?)
- Financing: what strategy ? funding options
- Organization of activities, regular meetings, and reviews
- Define contact persons (in Krakow and in the Velo, TT , IT/CT and other participating institutes)

# Technical matter

- Organize discussions by topic: FE, ADC, DSP, Interfaces
- Core functionality of the software platform
- Monitoring and trending
- Info needed for system design (eg power budget!)
- Strategy for shaper + spillover
- Differences between VELO/IT/TT sensors (and SiPM ?)
- Single vs multiple chip version ?
  - if multiple, how do we manage versions ? (submissions/planning issues)
- Compare 128/256ch, advantages/disadvantages
- Test boards. Who specifies/designs/produces them ?
- Expand specs with more details
- Compare with ATLAS upgrade strip chip design
- ADC part: look at architecture in detail, overlap with SciFi tracker (CT)
- Define missing blocks of chip
  - e.g. PLL, DACs, power (Vreg?), data interface, slow-control interface, band-gap
- What blocks can be borrowed from elsewhere?
- Digital block: Define strategy (specs, tools, input data.....)
- Prototyping in FPGA? (serial interface between ADC and FPGA?)
- Who does what ?

# Outcome of this meeting

Ideally, the minimal outcome of this strip ASIC workshop should be

- A list of technical questions and who will address them
- A scheme for collaborative work, with a list of roles, names and dates of meetings/reviews.
- A list of "living" (i.e. versionable) documents and a name of person responsible for each
  - technical specs, user guide, test reports, …
  - schedule/milestones, resources, spending profile, ...

And of course: we also need a contest to find a **name** for this chip